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Understanding Embedded - FPGAs (Field Programmable Gate Array)

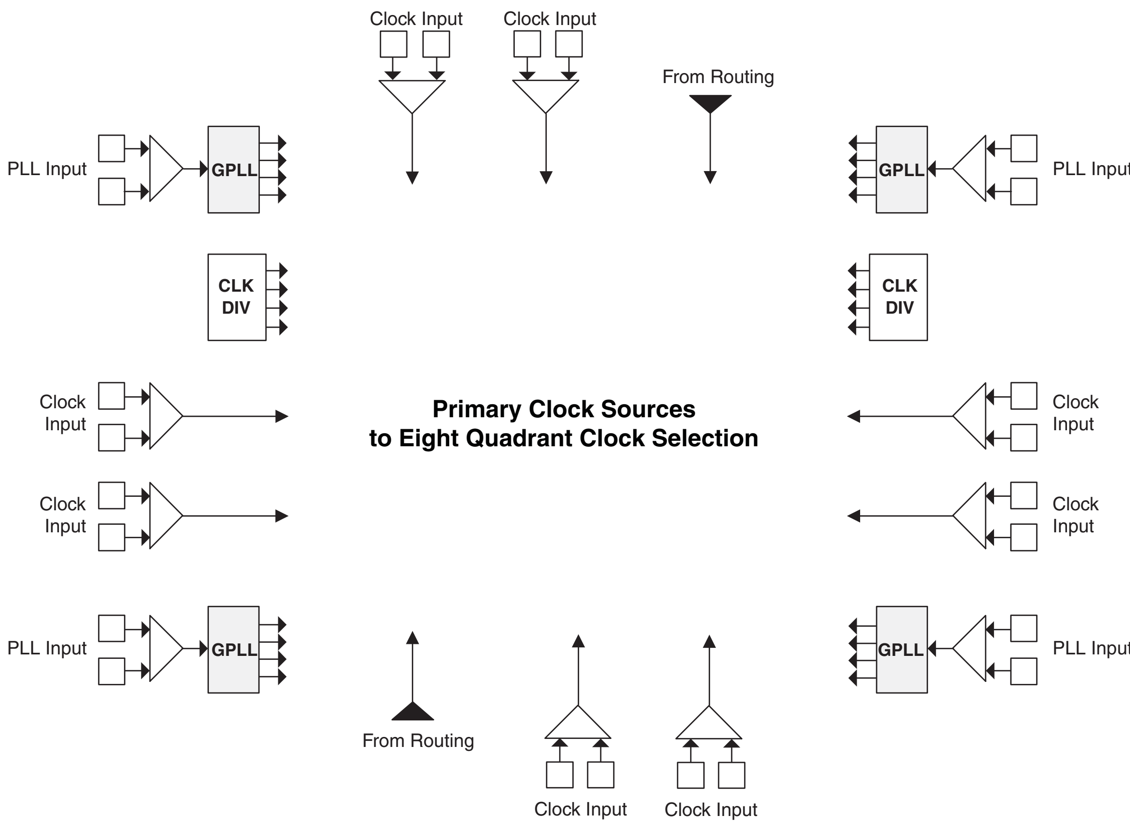
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	625
Number of Logic Elements/Cells	5000
Total RAM Bits	169984
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-5e-7tn144c

Figure 2-6. Primary Clock Sources for XP2-17



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.

Secondary Clock/Control Sources

LatticeXP2 devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-7 shows the secondary clock sources.

Figure 2-7. Secondary Clock Sources

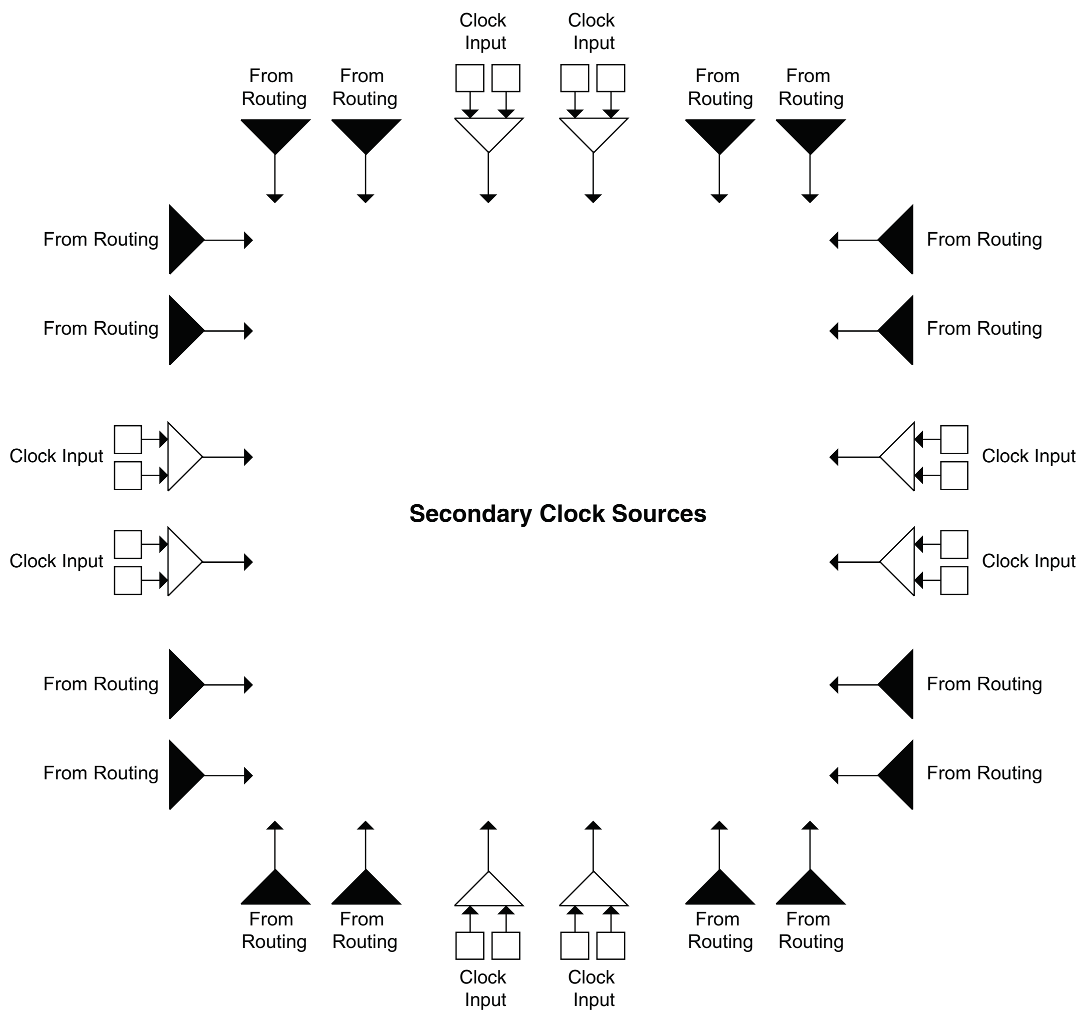
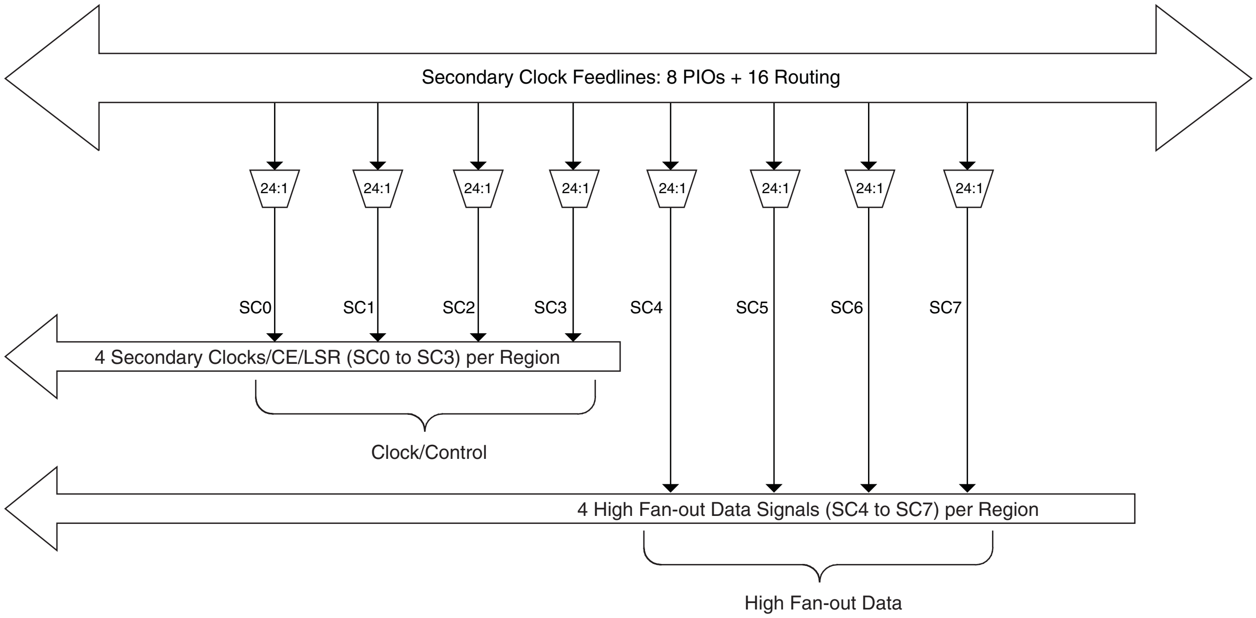


Figure 2-12. Secondary Clock Selection

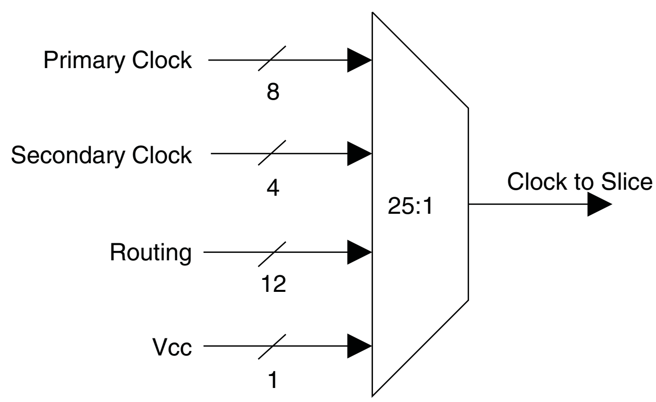


Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-13. Slice0 through Slice2 Clock Selection



sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

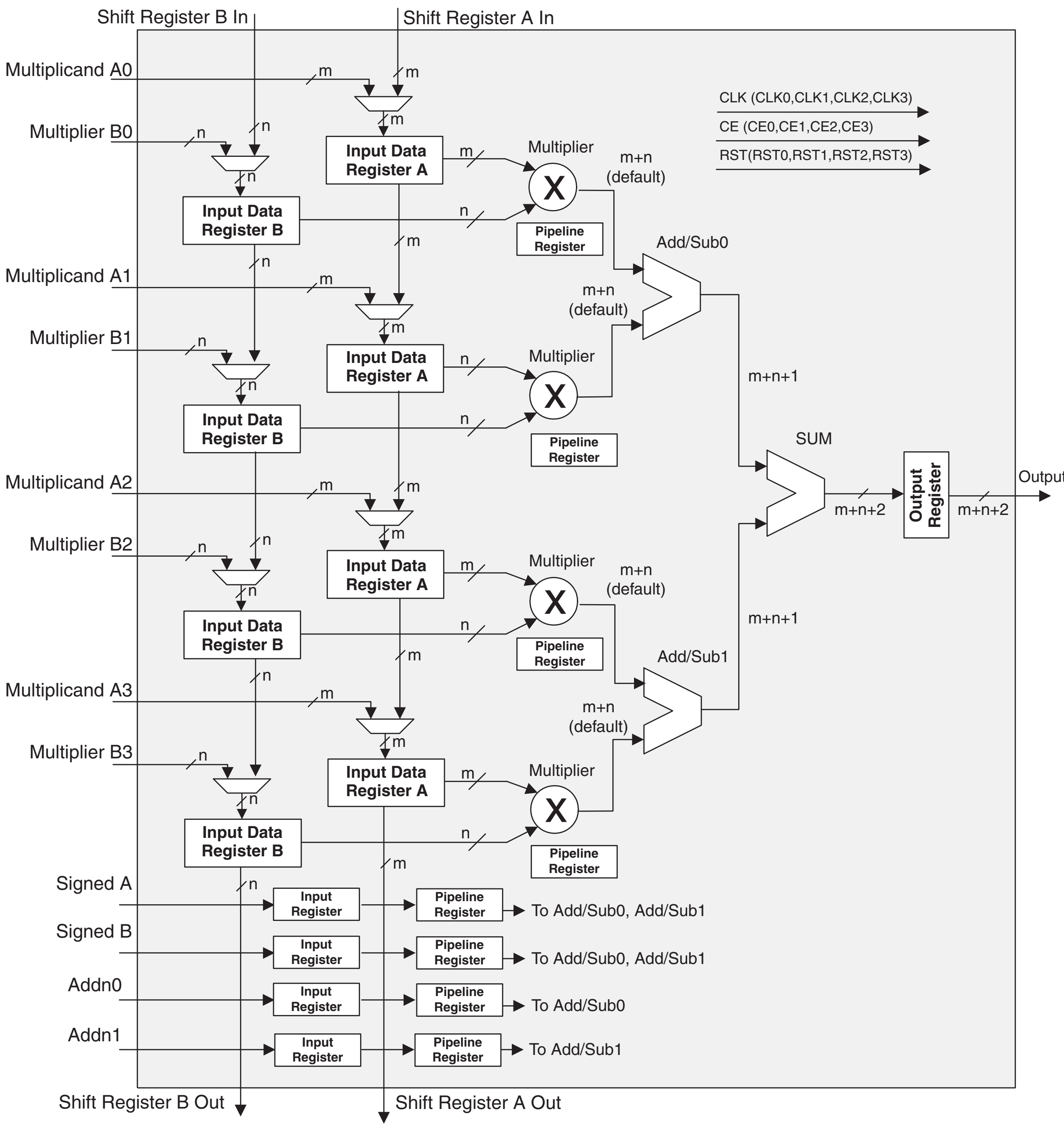
FlashBAK EBR Content Storage

All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.

MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly, CE and RST are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports other widths, in addition to x9, x18 and x36 widths, of signed and unsigned multipliers. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-7 provides an example of this.

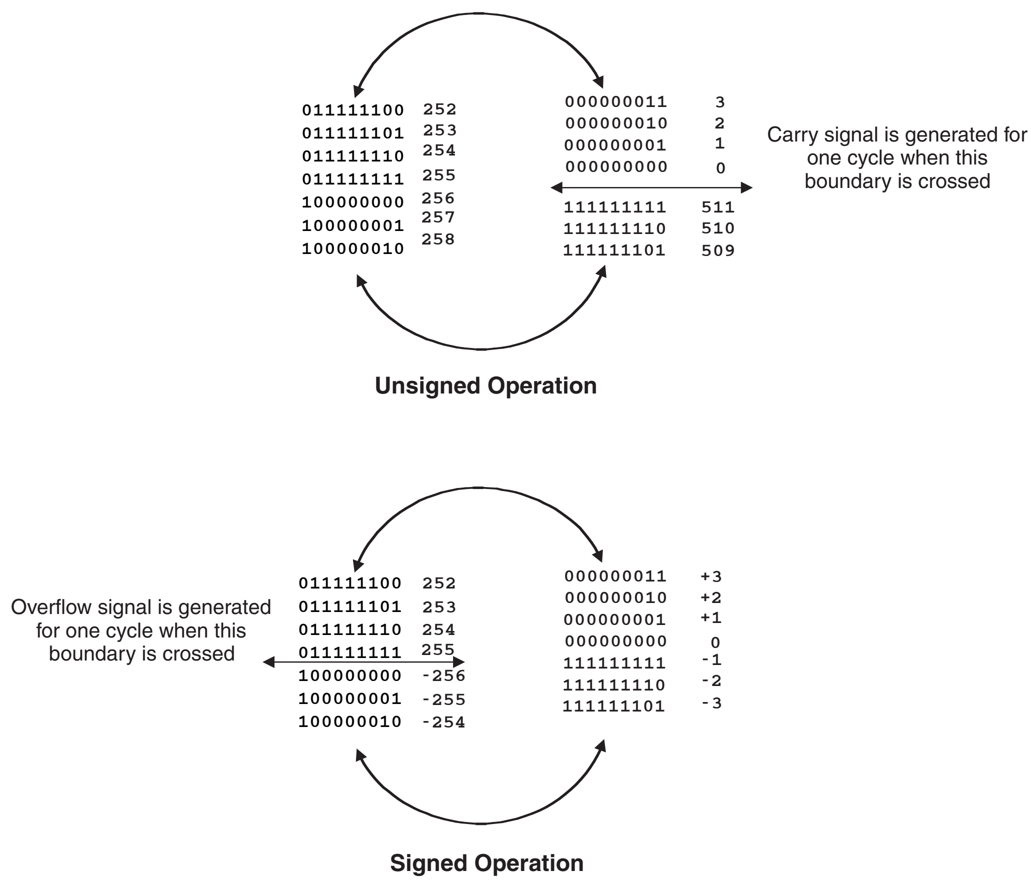
Table 2-7. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	000000000000000101	0101	000000101	000000000000000101
-6	N/A	N/A	N/A	1010	111111010	111111111111111010

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. "Roll-over" occurs and an overflow signal is indicated when any of the following is true: two unsigned numbers are added and the result is a smaller number than the accumulator, two positive numbers are added with a negative sum or two negative numbers are added with a positive sum. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions for the overflow signal for signed and unsigned operands are listed in Figure 2-24.

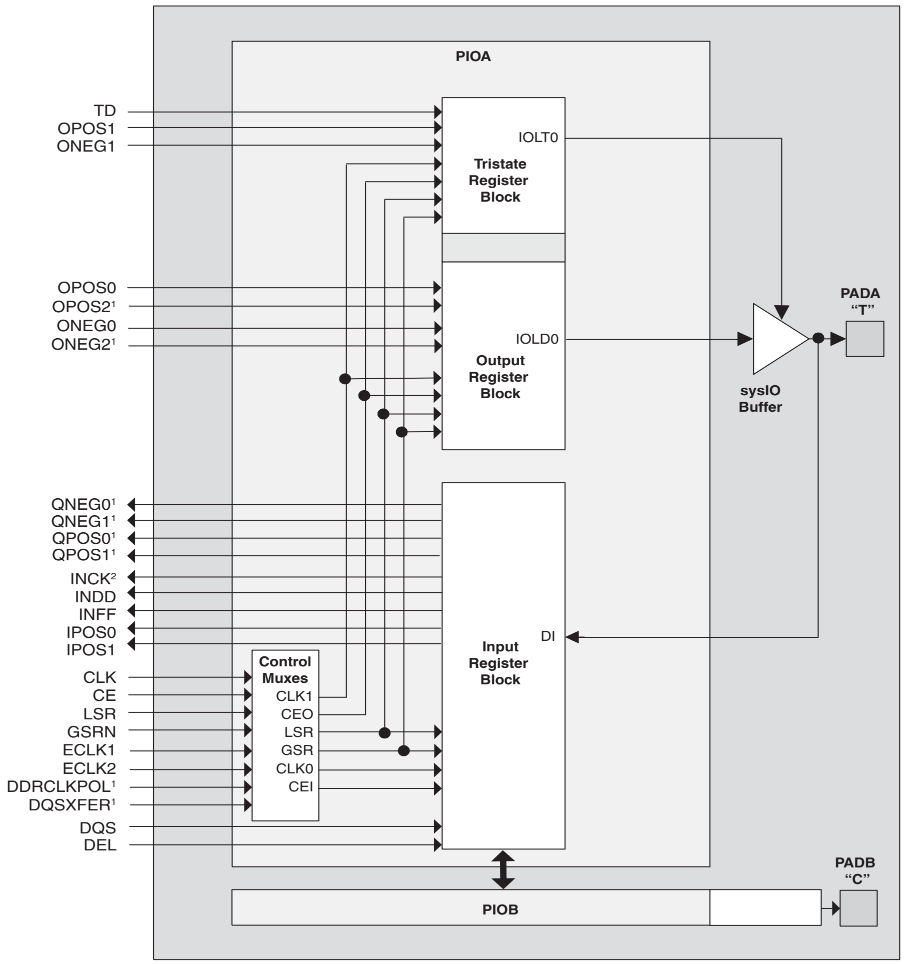
Figure 2-24. Accumulator Overflow/Underflow



Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-25. PIC Diagram



1. Signals are available on left/right/bottom edges only.
2. Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-25. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-27 shows the Tristate Register Block with the Output Block

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock signal is selected from general purpose routing, ECLK1, ECLK2 or a DQS signal (from the programmable DQS pin) and is provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

PICs have additional circuitry to allow implementation of high speed source synchronous and DDR memory interfaces.

PICs have registered elements that support DDR memory interfaces. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the top and bottom are designed for memories that support 18 bits of data. One of every 16 PIOs on the left and right and one of every 18 PIOs on the top and bottom contain delay elements to facilitate the generation of DQS signals. The DQS signals feed the DQS buses which span the set of 16 or 18 PIOs. Figure 2-28 and Figure 2-29 show the DQS pin assignments in each set of PIOs.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For additional information on using DDR memory support please see TN1138, LatticeXP2 High Speed I/O Interface.

Table 2-13. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL33 Class I, II	N/A	3.3
SSTL25 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL33, Class I, II	N/A	3.3
Differential SSTL25, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS[1, 2]	N/A	2.5
MLVDS[1]	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5
LVCMOS33D[1]	4mA, 8mA, 12mA, 16mA, 20mA	3.3

1. Emulated with external resistors.
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in

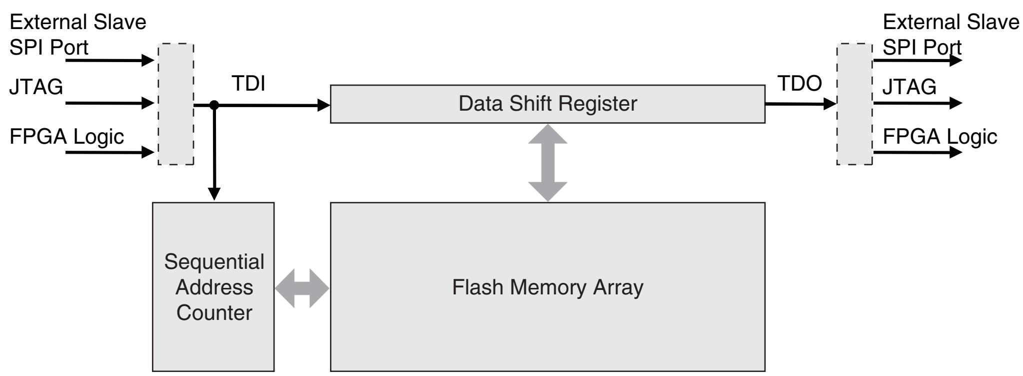
1. Unlocked
2. Key Locked – Presenting the key through the programming interface allows the device to be unlocked.
3. Permanently Locked – The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is independent of the Flash used for device configuration and given its use for general-purpose storage functions is always accessible regardless of the device security settings. For more information, see TN1137, LatticeXP2 Memory Usage Guide and TN1141, LatticeXP2 sysCONFIG Usage Guide.

Figure 2-34. Serial TAG Memory Diagram



Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. **Decryption Support**
   LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.
2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.
3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the

original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, LatticeXP2 Dual Boot Feature.

For more information on device configuration, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide.

On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.
2. During configuration, users select a different CCLK frequency.
3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

Table 2-14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode

CCLK/Oscillator (MHz)
2.5[1]
3.1[2]
4.3
5.4
6.9
8.1
9.2
10
13
15
20
26
32
40
54
80[3]
163[3]

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical[5]	Units
I_{CC}	Core Power Supply Current	XP2-5	14	mA
		XP2-8	18	mA
		XP2-17	24	mA
		XP2-30	35	mA
		XP2-40	45	mA
I_{CCAUX}	Auxiliary Power Supply Current[6]	XP2-5	15	mA
		XP2-8	15	mA
		XP2-17	15	mA
		XP2-30	16	mA
		XP2-40	16	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I_{CCIO}	Bank Power Supply Current (per bank)		2	mA
I_{CCJ}	V_{CCJ} Power Supply Current		0.25	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 25°C, power supplies at nominal voltage.
6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

Programming and Erase Flash Supply Current[1, 2, 3, 4, 5]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply)[6]	Units
I_{CC}	Core Power Supply Current	XP2-5	17	mA
		XP2-8	21	mA
		XP2-17	28	mA
		XP2-30	36	mA
		XP2-40	50	mA
I_{CCAUX}	Auxiliary Power Supply Current[7]	XP2-5	64	mA
		XP2-8	66	mA
		XP2-17	83	mA
		XP2-30	87	mA
		XP2-40	88	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I_{CCIO}	Bank Power Supply Current (per Bank)		5	mA
I_{CCJ}	V_{CCJ} Power Supply Current[8]		14	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz (excludes dynamic power from FPGA operation).
4. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
5. Bypass or decoupling capacitor across the supply.
6. T_J = 25°C, power supplies at nominal voltage.
7. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.
8. When programming via JTAG.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

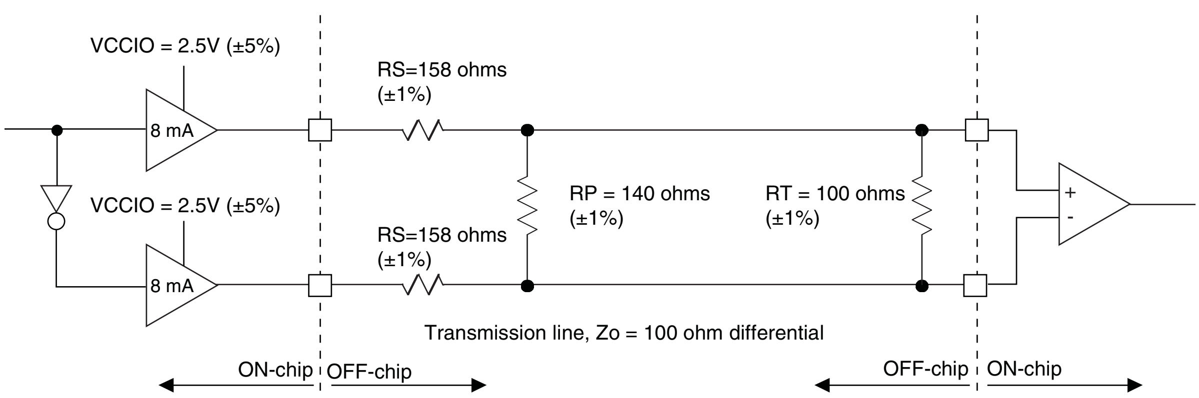


Table 3-1. LVDS25E DC Conditions

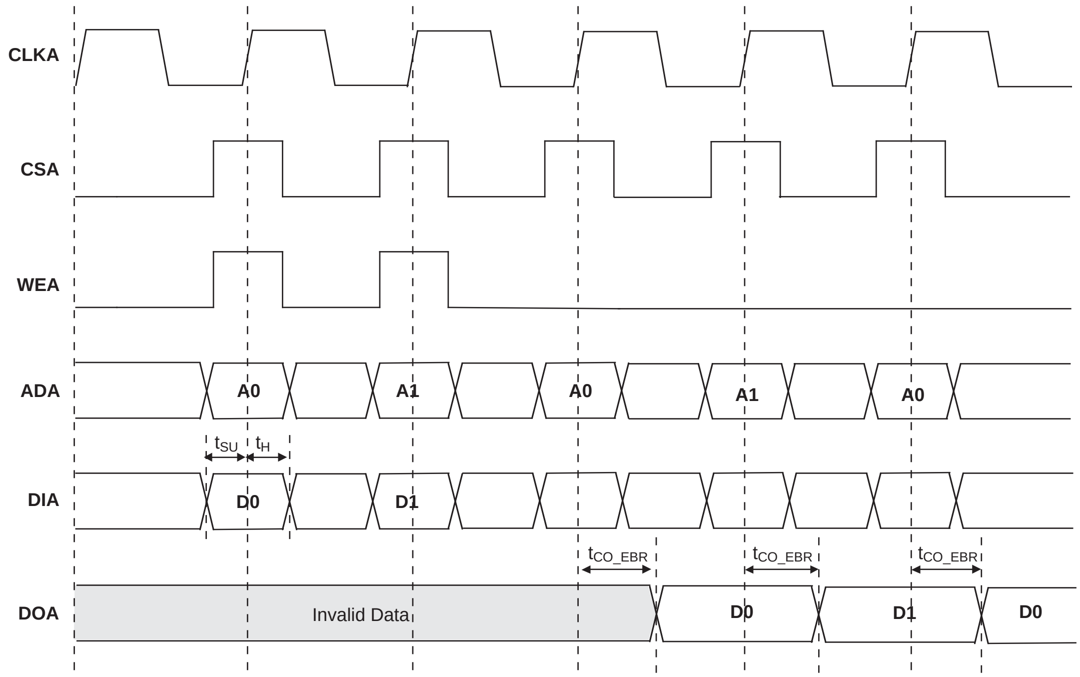
Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	158	Ω
R_P	Driver Parallel Resistor (+/-1%)	140	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage (after R_P)	1.43	V
V_{OL}	Output Low Voltage (after R_P)	1.07	V
V_{OD}	Output Differential Voltage (After R_P)	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

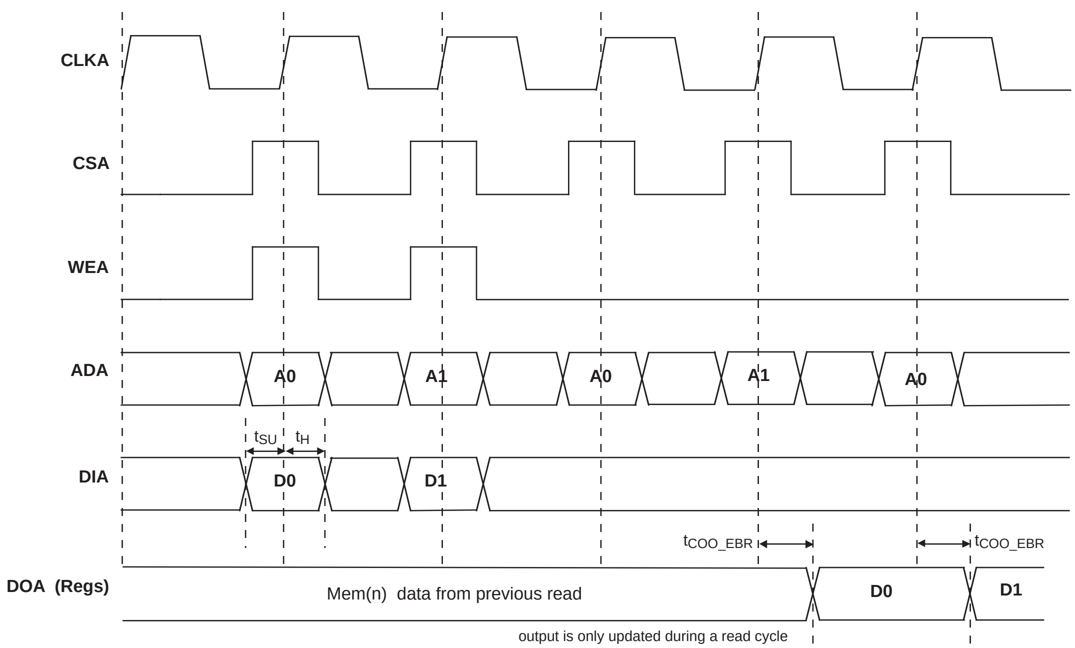
EBR Timing Diagrams

Figure 3-6. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-7. Read/Write Mode with Input and Output Registers



LatticeXP2 Family Timing Adders[1, 2, 3, 4] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTL33_4mA	LVTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

Pin Information Summary (Cont.)

Pin Type		XP2-5				XP2-8				XP2-17			XP2-30			XP2-40	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28	52	28	52	70	52	70
	Bank1	4	6	18	18	4	6	18	22	18	22	36	22	36	54	36	70
	Bank2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26	36	26	38	54	38	70
	Bank5	14	18	20	24	14	18	20	24	20	24	52	24	53	70	53	70
	Bank6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found under “Data Sheets” on the LatticeXP2 product page of the Lattice website a www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice Thermal Management document to find the device/package specific thermal values.

For Further Information

- TN1139, Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484I	1.2V	-5	fpBGA	484	IND	40
LFXP2-40E-6F484I	1.2V	-6	fpBGA	484	IND	40
LFXP2-40E-5F672I	1.2V	-5	fpBGA	672	IND	40
LFXP2-40E-6F672I	1.2V	-6	fpBGA	672	IND	40

Date	Version	Section	Change Summary
April 2008 (cont.)	01.4 (cont.)	DC and Switching Characteristics (cont.)	Updated Flash Download Time (From On-Chip Flash to SRAM) Table
			Updated Flash Program Time Table
			Updated Flash Erase Time Table
			Updated FlashBAK (from EBR to Flash) Table
			Updated Hot Socketing Specifications Table footnotes
		Pinout Information	Updated Signal Descriptions Table
June 2008	01.5	Architecture	Removed Read-Before-Write sysMEM EBR mode.
			Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Pinout Information	Updated DDR Banks Bonding Out per I/O Bank section of Pin Information Summary Table.
August 2008	01.6	—	Data sheet status changed from preliminary to final.
		Architecture	Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed “8W” specification from Hot Socketing Specifications table.
			Removed "8W" footnote from DC Electrical Characteristics table.
			Updated Register-to-Register Performance table.
		Ordering Information	Removed “8W” option from Part Number Description.
			Removed XP2-17 “8W” OPNs.
April 2011	01.7	DC and Switching Characteristics	Recommended Operating Conditions table, added footnote 5.
			On-Chip Flash Memory Specifications table, added footnote 1.
			BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms.
			sysCONFIG Port Timing Specifications table, added footnote 1 for t_{DINIT}.
January 2012	01.8	Multiple	Added support for Lattice Diamond design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary information.
May 2013	01.9	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			Added information regarding SED support.
		DC and Switching Characteristics	Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table.
		Ordering Information	Updated topside mark in Ordering Information diagram.
March 2014	02.0	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Added information on POR signal deactivation.
August 2014	02.1	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.
September 2014	2.2	DC and Switching Characteristics	Updated Switching Test Conditions section. Re-linked missing figure.