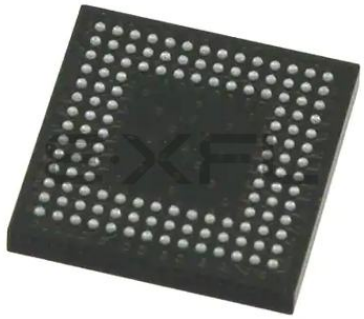


**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

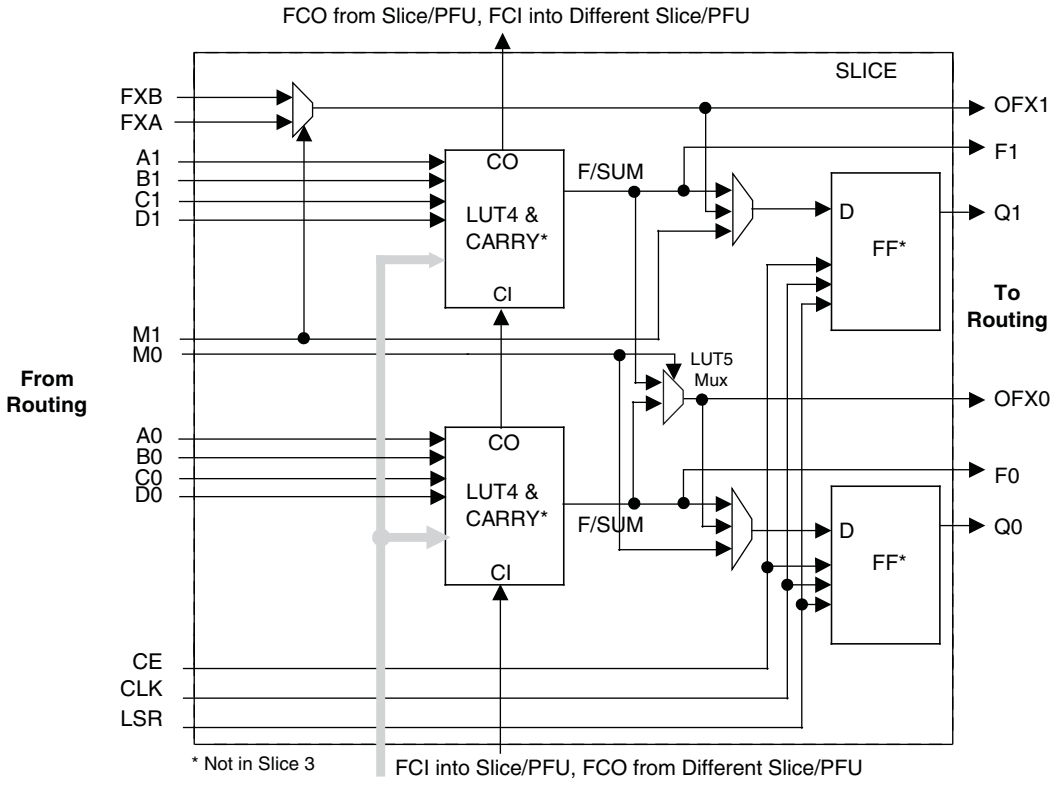
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1000 |
| Number of Logic Elements/Cells | 8000 |
| Total RAM Bits | 226304 |
| Number of I/O | 86 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 132-LFBGA, CSPBGA |
| Supplier Device Package | 132-CSBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-6m132c |

*Figure 2-3. Slice Diagram*




For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

*Table 2-2. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCI | Fast Carry-In[1] |
| Input | Inter-slice signal | FXA | Intermediate signal to generate LUT6 and LUT7 |
| Input | Inter-slice signal | FXB | Intermediate signal to generate LUT6 and LUT7 |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | Slice 2 of each PFU is the fast carry chain output[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

*Figure 2-4. General Purpose PLL (GPLL) Diagram*

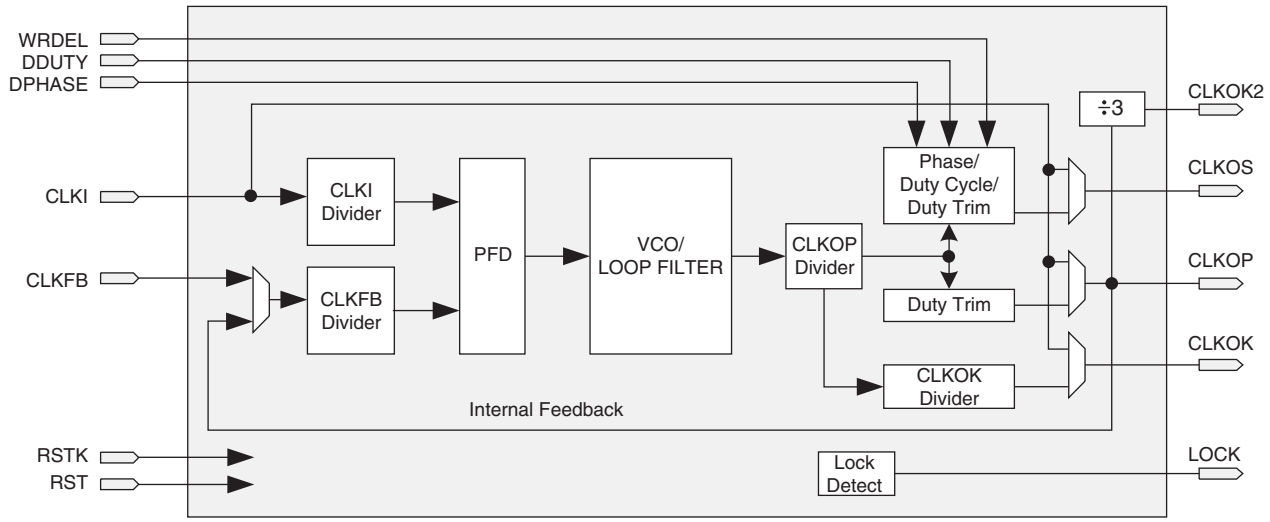



Table 2-4 provides a description of the signals in the GPLL blocks.

*Table 2-4. GPLL Block Signal Descriptions*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | "1" to reset PLL counters, VCO, charge pumps and M-dividers |
| RSTK | I | "1" to reset K-divider |
| DPHASE [3:0] | I | DPA Phase Adjust input |
| DDDUTY [3:0] | I | DPA Duty Cycle Select input |
| WRDEL | I | DPA Fine Delay Adjust input |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (no phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| CLKOK2 | O | PLL output to clock tree (CLKOP divided by 3) |
| LOCK | O | "1" indicates PLL LOCK to CLKI |

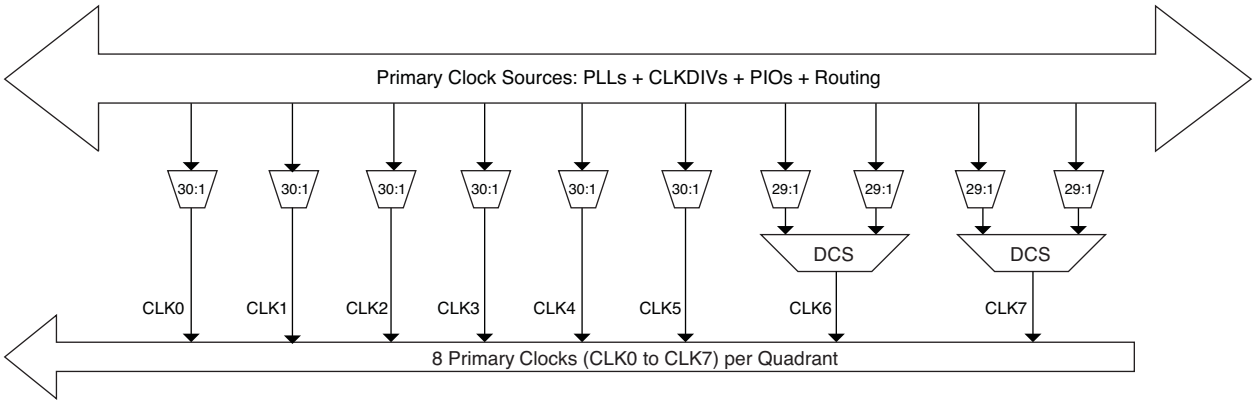
## Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.

## Primary Clock Routing

The clock routing structure in LatticeXP2 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-9 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

***Figure 2-9. Per Quadrant Primary Clock Selection***

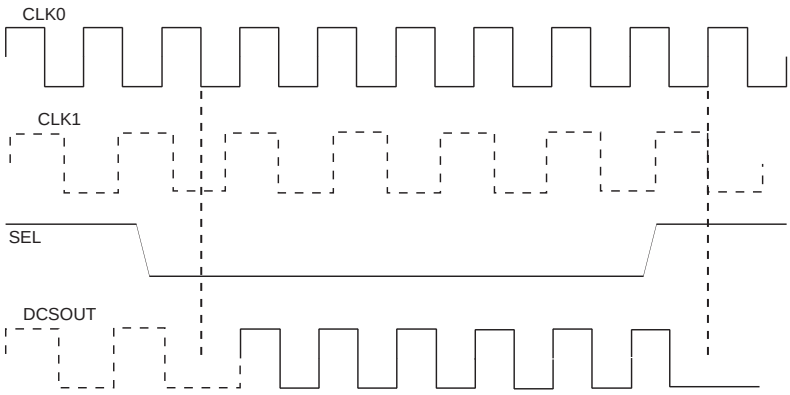



## Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-9).

Figure 2-10 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.

***Figure 2-10. DCS Waveforms***



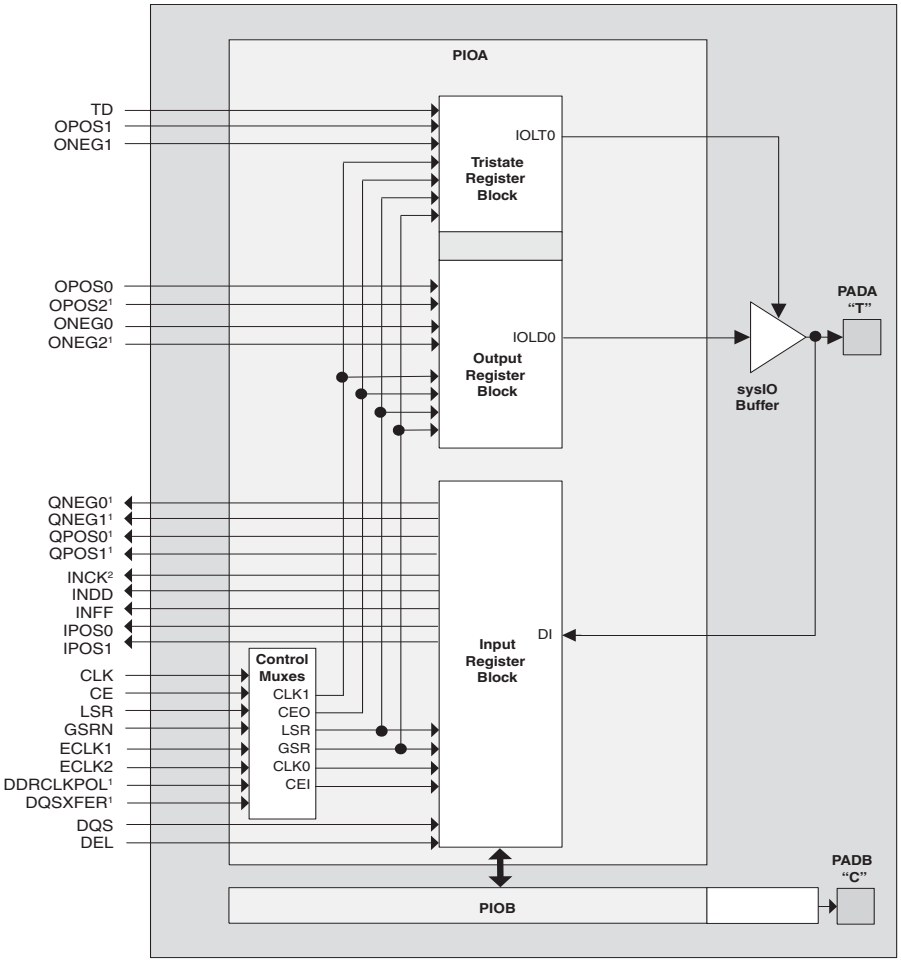

## Secondary Clock/Control Routing

Secondary clocks in the LatticeXP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR rows, DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-11 shows this special vertical routing channel and the eight secondary clock regions for the LatticeXP2-40.

## Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

***Figure 2-25. PIC Diagram***




1. Signals are available on left/right/bottom edges only.
2. Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

### Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-27 shows the Tristate Register Block with the Output Block

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

### Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock signal is selected from general purpose routing, ECLK1, ECLK2 or a DQS signal (from the programmable DQS pin) and is provided to the input register block. The clock can optionally be inverted.

## DDR Memory Support

PICs have additional circuitry to allow implementation of high speed source synchronous and DDR memory interfaces.

PICs have registered elements that support DDR memory interfaces. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the top and bottom are designed for memories that support 18 bits of data. One of every 16 PIOs on the left and right and one of every 18 PIOs on the top and bottom contain delay elements to facilitate the generation of DQS signals. The DQS signals feed the DQS buses which span the set of 16 or 18 PIOs. Figure 2-28 and Figure 2-29 show the DQS pin assignments in each set of PIOs.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For additional information on using DDR memory support please see TN1138, LatticeXP2 High Speed I/O Interface.

*Figure 2-28. DQS Input Routing (Left and Right)*

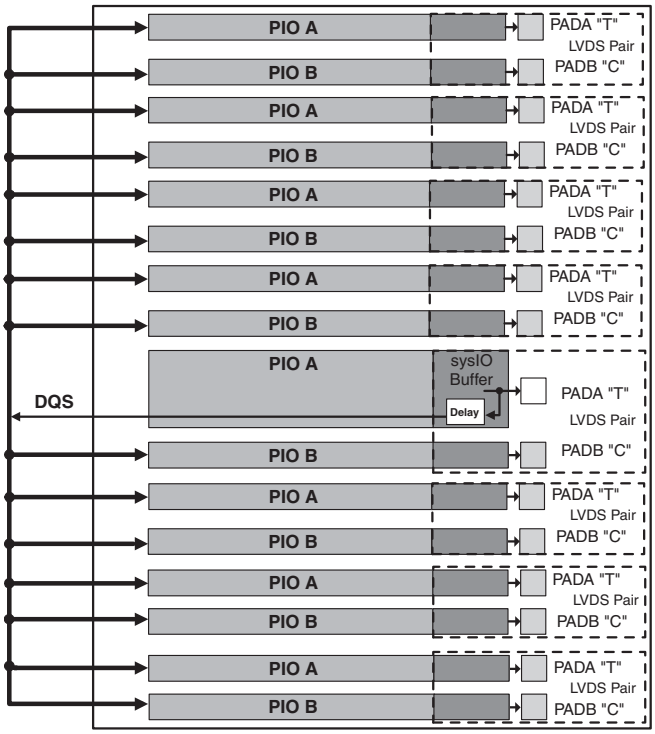



*Figure 2-29. DQS Input Routing (Top and Bottom)*

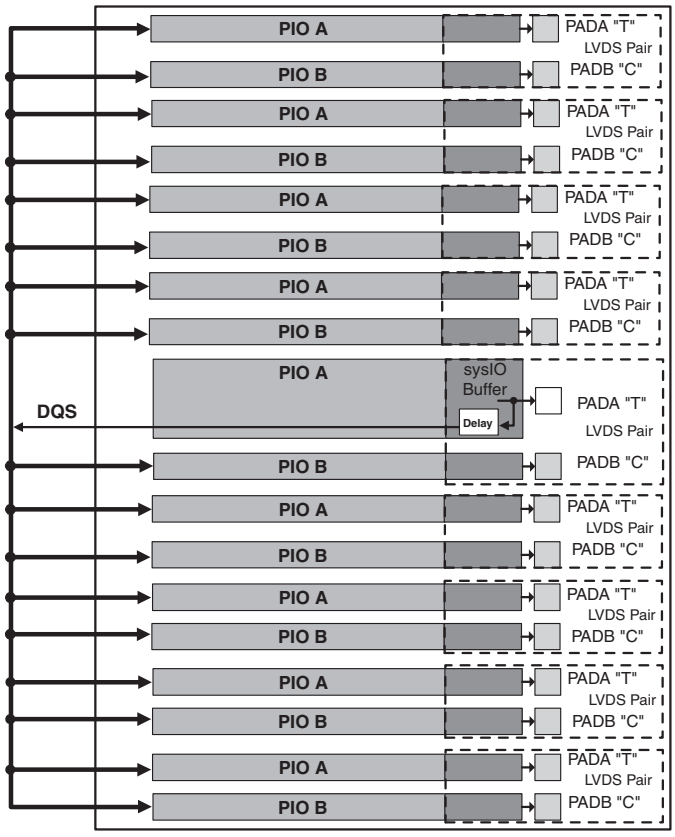
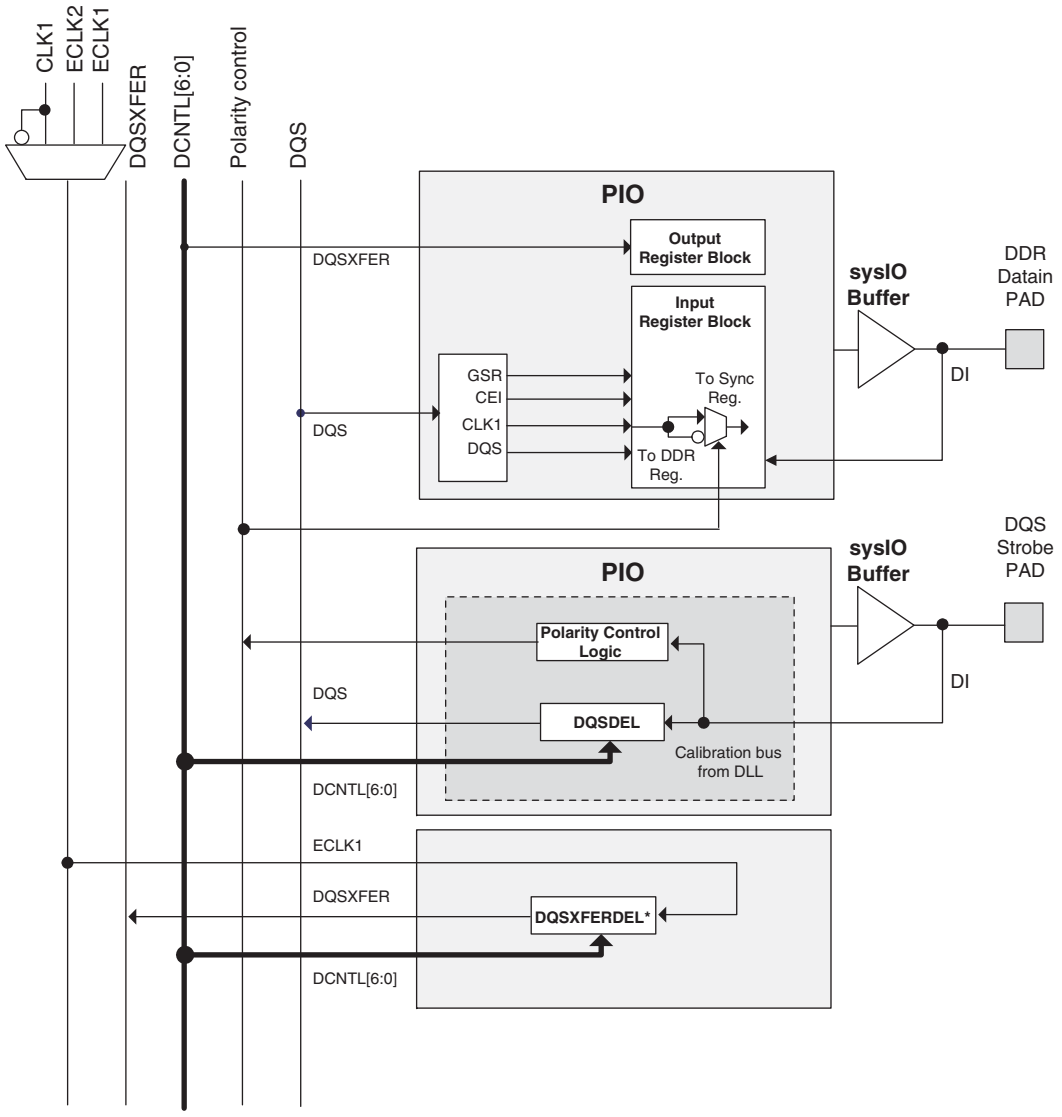


*Figure 2-31. DQS Local Bus*




*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

## Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

*Table 2-13. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Nom.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA 16mA, 20mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA, 16mA, 20mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA, 16mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA 16mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA, 6mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II | N/A | 1.8 |
| HSTL15 Class I | N/A | 1.5 |
| SSTL33 Class I, II | N/A | 3.3 |
| SSTL25 Class I, II | N/A | 2.5 |
| SSTL18 Class I, II | N/A | 1.8 |
| **Differential Interfaces** | | |
| Differential SSTL33, Class I, II | N/A | 3.3 |
| Differential SSTL25, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL15, Class I | N/A | 1.5 |
| LVDS[1, 2] | N/A | 2.5 |
| MLVDS[1] | N/A | 2.5 |
| BLVDS[1] | N/A | 2.5 |
| LVPECL[1] | N/A | 3.3 |
| RSDS[1] | N/A | 2.5 |
| LVCMOS33D[1] | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |

1. Emulated with external resistors.
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

## Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

# IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in

## Hot Socketing Specifications[1, 2, 3, 4]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{DK}$ | Input or I/O Leakage Current | $0 \le V_{IN} \le V_{IH}$ (MAX.) | — | — | +/-1 | mA |

1. Insensitive to sequence of $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$. However, assumes monotonic rise/fall rates for $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
4. LVCMOS and LVTTL only.

## ESD Performance

Please refer to the LatticeXP2 Product Family Qualification Summary for complete qualification data, including ESD performance.

## DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1] | Input or I/O Low Leakage | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 10 | µA |
| | | $V_{CCIO} \le V_{IN} \le V_{IH}$ (MAX) | — | — | 150 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{CCIO}$ | 30 | — | 210 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 210 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 6 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25ºC, f = 1.0 MHz.

## Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typical[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | XP2-5 | 14 | mA |
| | | XP2-8 | 18 | mA |
| | | XP2-17 | 24 | mA |
| | | XP2-30 | 35 | mA |
| | | XP2-40 | 45 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current[6] | XP2-5 | 15 | mA |
| | | XP2-8 | 15 | mA |
| | | XP2-17 | 15 | mA |
| | | XP2-30 | 16 | mA |
| | | XP2-40 | 16 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current (per PLL) | | 0.1 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (per bank) | | 2 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply Current | | 0.25 | mA |

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 25°C, power supplies at nominal voltage.
6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of $I_{CCAUX}$ and $I_{CCPLL}$. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

## Programming and Erase Flash Supply Current[1, 2, 3, 4, 5]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typical (25°C, Max. Supply)[6] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | XP2-5 | 17 | mA |
| | | XP2-8 | 21 | mA |
| | | XP2-17 | 28 | mA |
| | | XP2-30 | 36 | mA |
| | | XP2-40 | 50 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current[7] | XP2-5 | 64 | mA |
| | | XP2-8 | 66 | mA |
| | | XP2-17 | 83 | mA |
| | | XP2-30 | 87 | mA |
| | | XP2-40 | 88 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current (per PLL) | | 0.1 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (per Bank) | | 5 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply Current[8] | | 14 | mA |

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0 MHz (excludes dynamic power from FPGA operation).
4. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
5. Bypass or decoupling capacitor across the supply.
6. $T_J$ = 25°C, power supplies at nominal voltage.
7. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of $I_{CCAUX}$ and $I_{CCPLL}$. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.
8. When programming via JTAG.

# Typical Building Block Function Performance[1]

## Pin-to-Pin Performance (LVCMOS25 12mA Drive)

| Function | -7 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit Decoder | 4.4 | ns |
| 32-bit Decoder | 5.2 | ns |
| 64-bit Decoder | 5.6 | ns |
| 4:1 MUX | 3.7 | ns |
| 8:1 MUX | 3.9 | ns |
| 16:1 MUX | 4.3 | ns |
| 32:1 MUX | 4.5 | ns |

## Register-to-Register Performance

| Function | -7 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit Decoder | 521 | MHz |
| 32-bit Decoder | 537 | MHz |
| 64-bit Decoder | 484 | MHz |
| 4:1 MUX | 744 | MHz |
| 8:1 MUX | 678 | MHz |
| 16:1 MUX | 616 | MHz |
| 32:1 MUX | 529 | MHz |
| 8-bit Adder | 570 | MHz |
| 16-bit Adder | 507 | MHz |
| 64-bit Adder | 293 | MHz |
| 16-bit Counter | 541 | MHz |
| 32-bit Counter | 440 | MHz |
| 64-bit Counter | 321 | MHz |
| 64-bit Accumulator | 261 | MHz |
| **Embedded Memory Functions** | | |
| 512x36 Single Port RAM, EBR Output Registers | 315 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers) | 315 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers) | 231 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (One PFU) | 760 | MHz |
| 32x2 Pseudo-Dual Port RAM | 455 | MHz |
| 64x1 Pseudo-Dual Port RAM | 351 | MHz |
| **DSP Functions** | | |
| 18x18 Multiplier (All Registers) | 342 | MHz |
| 9x9 Multiplier (All Registers) | 342 | MHz |
| 36x36 Multiply (All Registers) | 330 | MHz |
| 18x18 Multiply/Accumulate (Input and Output Registers) | 218 | MHz |
| 18x18 Multiply-Add/Sub-Sum (All Registers) | 292 | MHz |

# LatticeXP2 External Switching Characteristics (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HE}$ | Clock to Data Hold - PIO Input Register | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $f_{MAX\_IOE}$ | Clock Frequency of I/O and PFU Register | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| **General I/O Pin Parameters (using Primary Clock with PLL)**[1] | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | XP2-5 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-8 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-17 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-30 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-40 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | XP2-5 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-8 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-17 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | XP2-5 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-8 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-17 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-8 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-17 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-30 | 2.00 | — | 2.20 | — | 2.40 | — | ns |
| | | XP2-40 | 2.00 | — | 2.20 | — | 2.40 | — | ns |

## LatticeXP2 External Switching Characteristics (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| **DDR[2] and DDR2[3] I/O Pin Parameters** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | XP2 | — | 0.29 | — | 0.29 | — | 0.29 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | XP2 | 0.71 | — | 0.71 | — | 0.71 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | XP2 | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | XP2 | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR}$ | DDR Clock Frequency | XP2 | 95 | 200 | 95 | 166 | 95 | 133 | MHz |
| $f_{MAX\_DDR2}$ | DDR Clock Frequency | XP2 | 133 | 200 | 133 | 200 | 133 | 166 | MHz |
| **Primary Clock** | | | | | | | | | |
| $f_{MAX\_PRI}$ | Frequency for Primary Clock Tree | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | XP2 | 1 | — | 1 | — | 1 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Bank | XP2 | — | 160 | — | 160 | — | 160 | ps |
| **Edge Clock (ECLK1 and ECLK2)** | | | | | | | | | |
| $f_{MAX\_ECLK}$ | Frequency for Edge Clock | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| $t_{W\_ECLK}$ | Clock Pulse Width for Edge Clock | XP2 | 1 | — | 1 | — | 1 | — | ns |
| $t_{SKEW\_ECLK}$ | Edge Clock Skew Within an Edge of the Device | XP2 | — | 130 | — | 130 | — | 130 | ps |

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25.
3. DDR2 timing numbers based on SSTL18.

## LatticeXP2 Family Timing Adders[1, 2, 3, 4] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -7 | -6 | -5 | Units |
|---|---|---|---|---|---|
| HSTL15_I | HSTL_15 class I 4mA drive | 0.32 | 0.69 | 1.06 | ns |
| HSTL15D_I | Differential HSTL 15 class I 4mA drive | 0.32 | 0.69 | 1.06 | ns |
| SSTL33_I | SSTL_3 class I | -0.25 | 0.05 | 0.35 | ns |
| SSTL33_II | SSTL_3 class II | -0.31 | -0.02 | 0.27 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.25 | 0.05 | 0.35 | ns |
| SSTL33D_II | Differential SSTL_3 class II | -0.31 | -0.02 | 0.27 | ns |
| SSTL25_I | SSTL_2 class I 8mA drive | -0.25 | 0.02 | 0.30 | ns |
| SSTL25_II | SSTL_2 class II 16mA drive | -0.28 | 0.00 | 0.28 | ns |
| SSTL25D_I | Differential SSTL_2 class I 8mA drive | -0.25 | 0.02 | 0.30 | ns |
| SSTL25D_II | Differential SSTL_2 class II 16mA drive | -0.28 | 0.00 | 0.28 | ns |
| SSTL18_I | SSTL_1.8 class I | -0.17 | 0.13 | 0.43 | ns |
| SSTL18_II | SSTL_1.8 class II 8mA drive | -0.18 | 0.12 | 0.42 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | -0.17 | 0.13 | 0.43 | ns |
| SSTL18D_II | Differential SSTL_1.8 class II 8mA drive | -0.18 | 0.12 | 0.42 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | -0.37 | -0.05 | 0.26 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | -0.45 | -0.18 | 0.10 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | -0.52 | -0.24 | 0.04 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | -0.43 | -0.14 | 0.14 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | -0.46 | -0.18 | 0.09 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive, fast slew rate | -0.37 | -0.05 | 0.26 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive, fast slew rate | -0.45 | -0.18 | 0.10 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive, fast slew rate | -0.52 | -0.24 | 0.04 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive, fast slew rate | -0.43 | -0.14 | 0.14 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive, fast slew rate | -0.46 | -0.18 | 0.09 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive, fast slew rate | -0.42 | -0.15 | 0.13 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive, fast slew rate | -0.48 | -0.21 | 0.05 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive, fast slew rate | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive, fast slew rate | -0.45 | -0.18 | 0.08 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive, fast slew rate | -0.49 | -0.22 | 0.04 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive, fast slew rate | -0.46 | -0.18 | 0.10 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive, fast slew rate | -0.52 | -0.25 | 0.02 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive, fast slew rate | -0.56 | -0.30 | -0.03 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive, fast slew rate | -0.50 | -0.24 | 0.03 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive, fast slew rate | -0.45 | -0.17 | 0.11 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive, fast slew rate | -0.53 | -0.26 | 0.00 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive, fast slew rate | -0.46 | -0.19 | 0.08 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive, fast slew rate | -0.55 | -0.29 | -0.02 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive, slow slew rate | 0.98 | 1.41 | 1.84 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive, slow slew rate | 0.74 | 1.16 | 1.58 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive, slow slew rate | 0.56 | 0.97 | 1.38 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive, slow slew rate | 0.77 | 1.19 | 1.61 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive, slow slew rate | 0.57 | 0.98 | 1.40 | ns |

## Flash Download Time (from On-Chip Flash to SRAM)

**Over Recommended Operating Conditions**

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{REFRESH}$ | PROGRAMN Low-to-High. Transition to Done High. | XP2-5 | — | 1.8 | 2.1 | ms |
| | | XP2-8 | — | 1.9 | 2.3 | ms |
| | | XP2-17 | — | 1.7 | 2.0 | ms |
| | | XP2-30 | — | 2.0 | 2.1 | ms |
| | | XP2-40 | — | 2.0 | 2.3 | ms |
| | Power-up refresh when PROGRAMN is pulled up to $V_{CC}$ ($V_{CC}$=$V_{CC}$ Min) | XP2-5 | — | 1.8 | 2.1 | ms |
| | | XP2-8 | — | 1.9 | 2.3 | ms |
| | | XP2-17 | — | 1.7 | 2.0 | ms |
| | | XP2-30 | — | 2.0 | 2.1 | ms |
| | | XP2-40 | — | 2.0 | 2.3 | ms |

## Flash Program Time

**Over Recommended Operating Conditions**

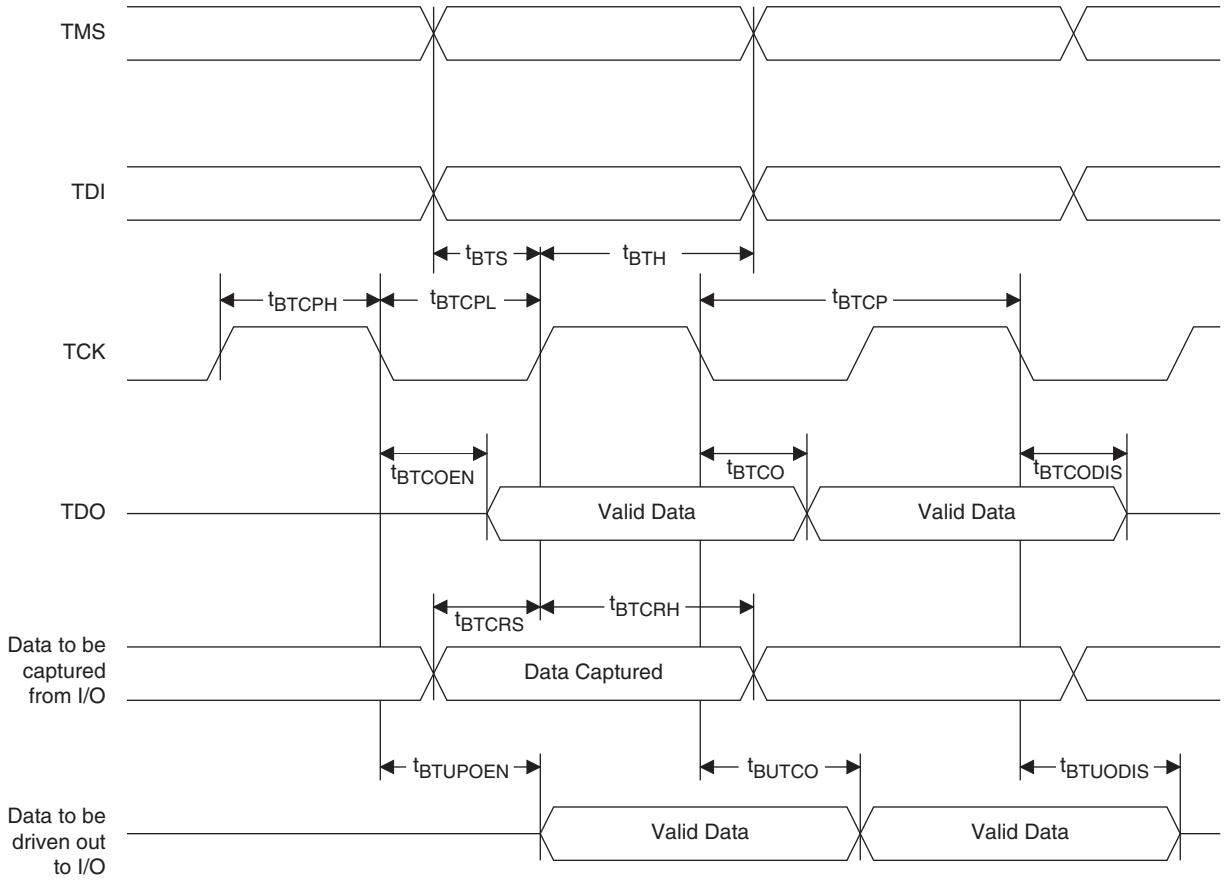
| Device | Flash Density | | Program Time Typ. | Units |
|---|---|---|---|---|
| XP2-5 | 1.2M | TAG | 1.0 | ms |
| | | Main Array | 1.1 | s |
| XP2-8 | 2.0M | TAG | 1.0 | ms |
| | | Main Array | 1.4 | s |
| XP2-17 | 3.6M | TAG | 1.0 | ms |
| | | Main Array | 1.8 | s |
| XP2-30 | 6.0M | TAG | 2.0 | ms |
| | | Main Array | 3.0 | s |
| XP2-40 | 8.0M | TAG | 2.0 | ms |
| | | Main Array | 4.0 | s |

## Flash Erase Time

**Over Recommended Operating Conditions**

| Device | Flash Density | | Erase Time Typ. | Units |
|---|---|---|---|---|
| XP2-5 | 1.2M | TAG | 1.0 | s |
| | | Main Array | 3.0 | s |
| XP2-8 | 2.0M | TAG | 1.0 | s |
| | | Main Array | 4.0 | s |
| XP2-17 | 3.6M | TAG | 1.0 | s |
| | | Main Array | 5.0 | s |
| XP2-30 | 6.0M | TAG | 2.0 | s |
| | | Main Array | 7.0 | s |
| XP2-40 | 8.0M | TAG | 2.0 | s |
| | | Main Array | 9.0 | s |

*Figure 3-10. JTAG Port Timing Waveforms*



## PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO Within PIC | DDR Strobe (DQS) and Data (DQ) Pins |
|---|---|---|
| **For Left and Right Edges of the Device** | | |
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |
| **For Top and Bottom Edges of the Device** | | |
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |
| P[Edge] [n+4] | A | DQ |
| | B | DQ |

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-30E-5FTN256C | 1.2V | -5 | Lead-Free ftBGA | 256 | COM | 30 |
| LFXP2-30E-6FTN256C | 1.2V | -6 | Lead-Free ftBGA | 256 | COM | 30 |
| LFXP2-30E-7FTN256C | 1.2V | -7 | Lead-Free ftBGA | 256 | COM | 30 |
| LFXP2-30E-5FN484C | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 30 |
| LFXP2-30E-6FN484C | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 30 |
| LFXP2-30E-7FN484C | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 30 |
| LFXP2-30E-5FN672C | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 30 |
| LFXP2-30E-6FN672C | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 30 |
| LFXP2-30E-7FN672C | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 30 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-40E-5FN484C | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 40 |
| LFXP2-40E-6FN484C | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 40 |
| LFXP2-40E-7FN484C | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 40 |
| LFXP2-40E-5FN672C | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 40 |
| LFXP2-40E-6FN672C | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 40 |
| LFXP2-40E-7FN672C | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 40 |

**Industrial**

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-5E-5MN132I | 1.2V | -5 | Lead-Free csBGA | 132 | IND | 5 |
| LFXP2-5E-6MN132I | 1.2V | -6 | Lead-Free csBGA | 132 | IND | 5 |
| LFXP2-5E-5TN144I | 1.2V | -5 | Lead-Free TQFP | 144 | IND | 5 |
| LFXP2-5E-6TN144I | 1.2V | -6 | Lead-Free TQFP | 144 | IND | 5 |
| LFXP2-5E-5QN208I | 1.2V | -5 | Lead-Free PQFP | 208 | IND | 5 |
| LFXP2-5E-6QN208I | 1.2V | -6 | Lead-Free PQFP | 208 | IND | 5 |
| LFXP2-5E-5FTN256I | 1.2V | -5 | Lead-Free ftBGA | 256 | IND | 5 |
| LFXP2-5E-6FTN256I | 1.2V | -6 | Lead-Free ftBGA | 256 | IND | 5 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-8E-5MN132I | 1.2V | -5 | Lead-Free csBGA | 132 | IND | 8 |
| LFXP2-8E-6MN132I | 1.2V | -6 | Lead-Free csBGA | 132 | IND | 8 |
| LFXP2-8E-5TN144I | 1.2V | -5 | Lead-Free TQFP | 144 | IND | 8 |
| LFXP2-8E-6TN144I | 1.2V | -6 | Lead-Free TQFP | 144 | IND | 8 |
| LFXP2-8E-5QN208I | 1.2V | -5 | Lead-Free PQFP | 208 | IND | 8 |
| LFXP2-8E-6QN208I | 1.2V | -6 | Lead-Free PQFP | 208 | IND | 8 |
| LFXP2-8E-5FTN256I | 1.2V | -5 | Lead-Free ftBGA | 256 | IND | 8 |
| LFXP2-8E-6FTN256I | 1.2V | -6 | Lead-Free ftBGA | 256 | IND | 8 |

## Conventional Packaging

**Commercial**

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-5E-5M132C | 1.2V | -5 | csBGA | 132 | COM | 5 |
| LFXP2-5E-6M132C | 1.2V | -6 | csBGA | 132 | COM | 5 |
| LFXP2-5E-7M132C | 1.2V | -7 | csBGA | 132 | COM | 5 |
| LFXP2-5E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 5 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-8E-5M132C | 1.2V | -5 | csBGA | 132 | COM | 8 |
| LFXP2-8E-6M132C | 1.2V | -6 | csBGA | 132 | COM | 8 |
| LFXP2-8E-7M132C | 1.2V | -7 | csBGA | 132 | COM | 8 |
| LFXP2-8E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 8 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-17E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-5F484C | 1.2V | -5 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-6F484C | 1.2V | -6 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-7F484C | 1.2V | -7 | fpBGA | 484 | COM | 17 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-30E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-5F484C | 1.2V | -5 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-6F484C | 1.2V | -6 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-7F484C | 1.2V | -7 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-5F672C | 1.2V | -5 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-6F672C | 1.2V | -6 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-7F672C | 1.2V | -7 | fpBGA | 672 | COM | 30 |