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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

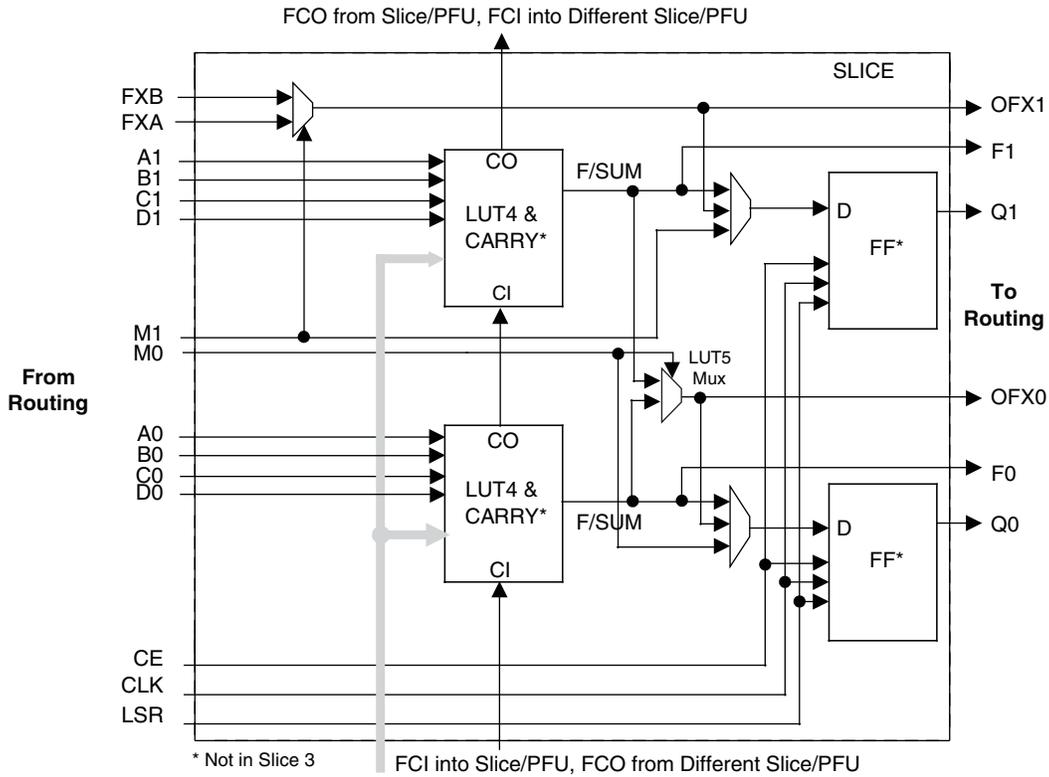
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	86
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-6m132i

Figure 2-3. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
- WAD [A:D] is a 4bit address from slice 1 LUT input

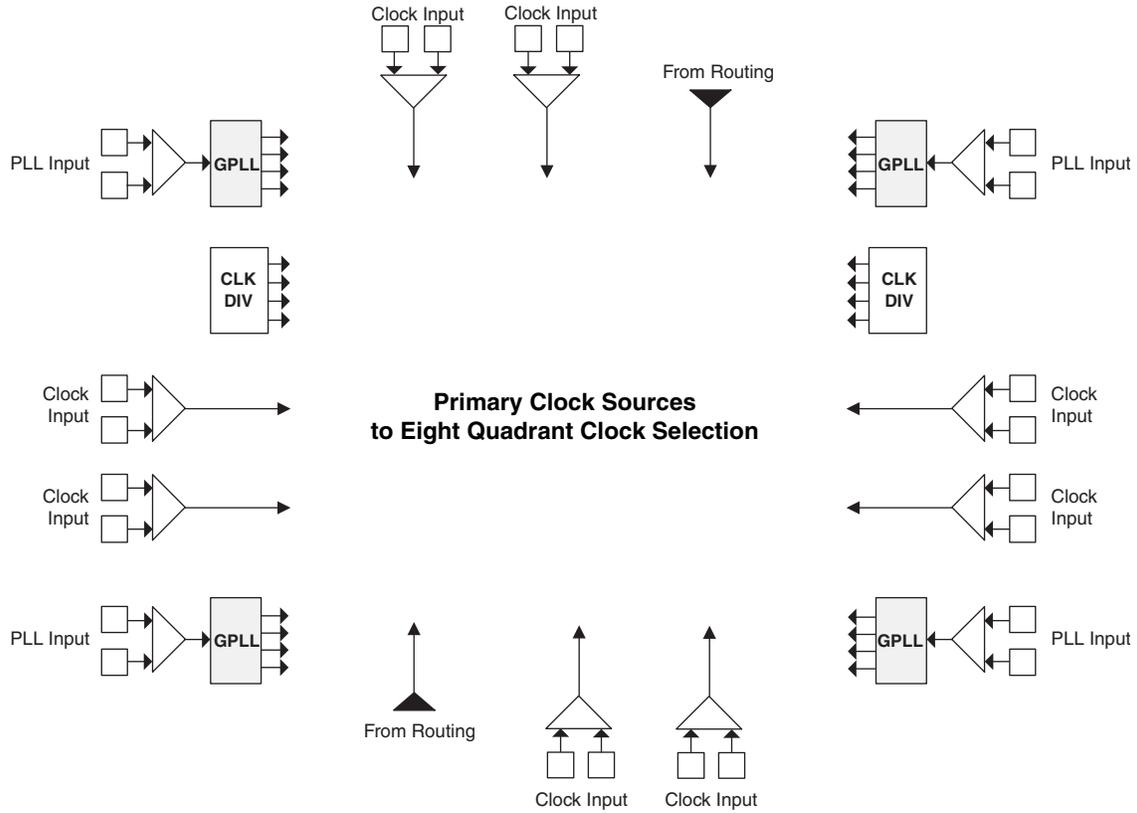
Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-In ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

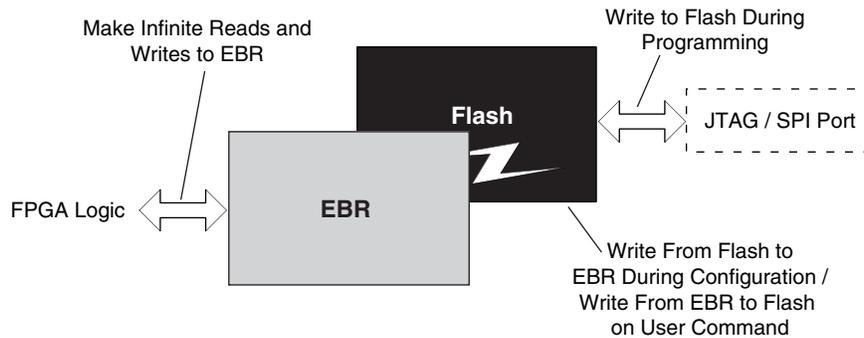
2. Requires two PFUs.

Figure 2-6. Primary Clock Sources for XP2-17



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.

Figure 2-16. FlashBAK Technology



Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

Figure 2-17. Memory Core Reset

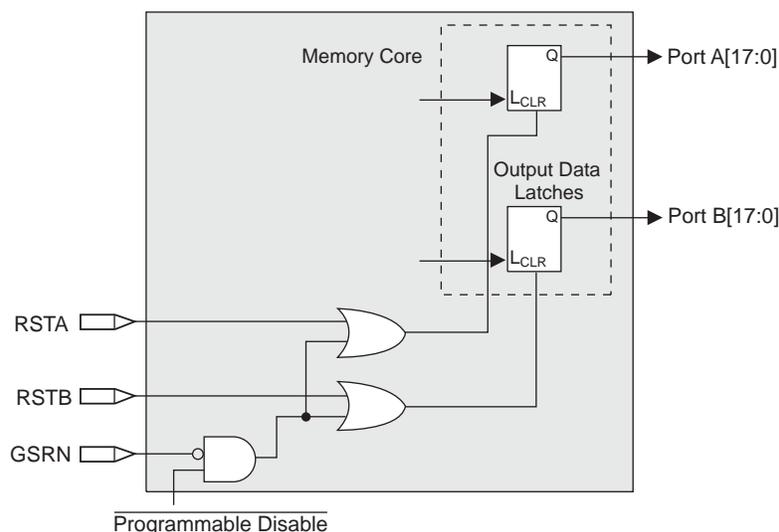
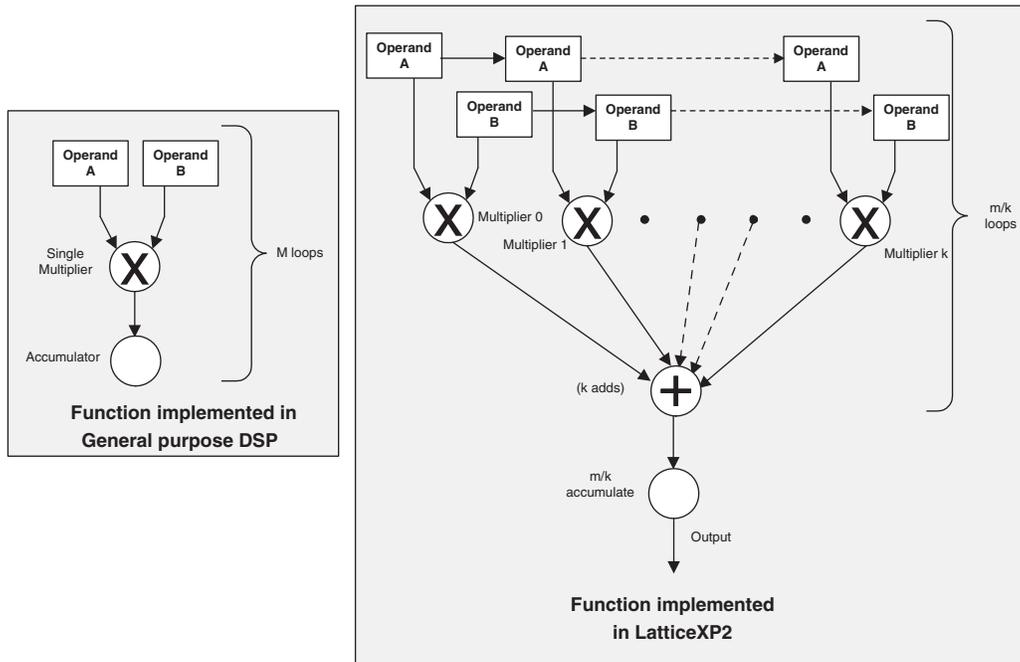


Figure 2-19. Comparison of General DSP and LatticeXP2 Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeXP2 family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeXP2 family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-6 shows the capabilities of the block.

Table 2-6. Maximum Number of Elements in a Block

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	—
MULTADDSUB	4	2	—
MULTADDSUBSUM	2	1	—

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting 'dynamic operation' the following operations are possible:

register. Similarly, CE and RST are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports other widths, in addition to x9, x18 and x36 widths, of signed and unsigned multipliers. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-7 provides an example of this.

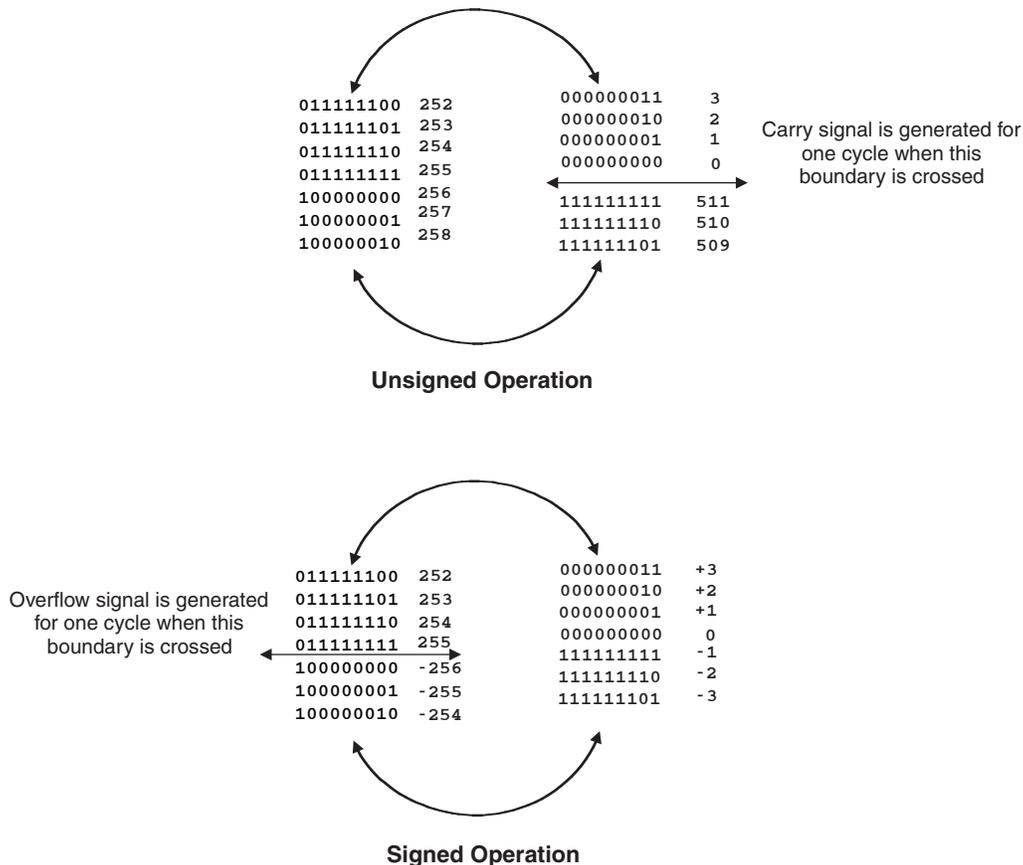
Table 2-7. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	0000000000000000101	0101	000000101	0000000000000000101
-6	N/A	N/A	N/A	1010	11111010	111111111111111010

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. "Roll-over" occurs and an overflow signal is indicated when any of the following is true: two unsigned numbers are added and the result is a smaller number than the accumulator, two positive numbers are added with a negative sum or two negative numbers are added with a positive sum. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions for the overflow signal for signed and unsigned operands are listed in Figure 2-24.

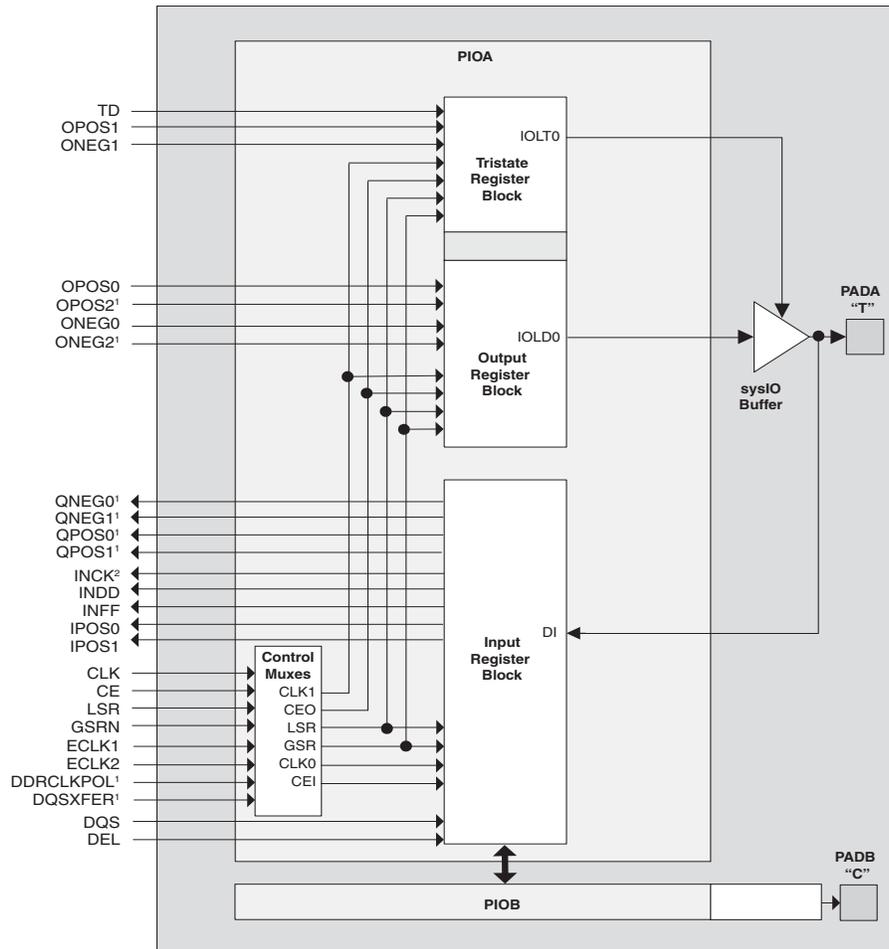
Figure 2-24. Accumulator Overflow/Underflow



Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-25. PIC Diagram



1. Signals are available on left/right/bottom edges only.
2. Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-25. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

Table 2-11. PIO Signal List

Name	Type	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

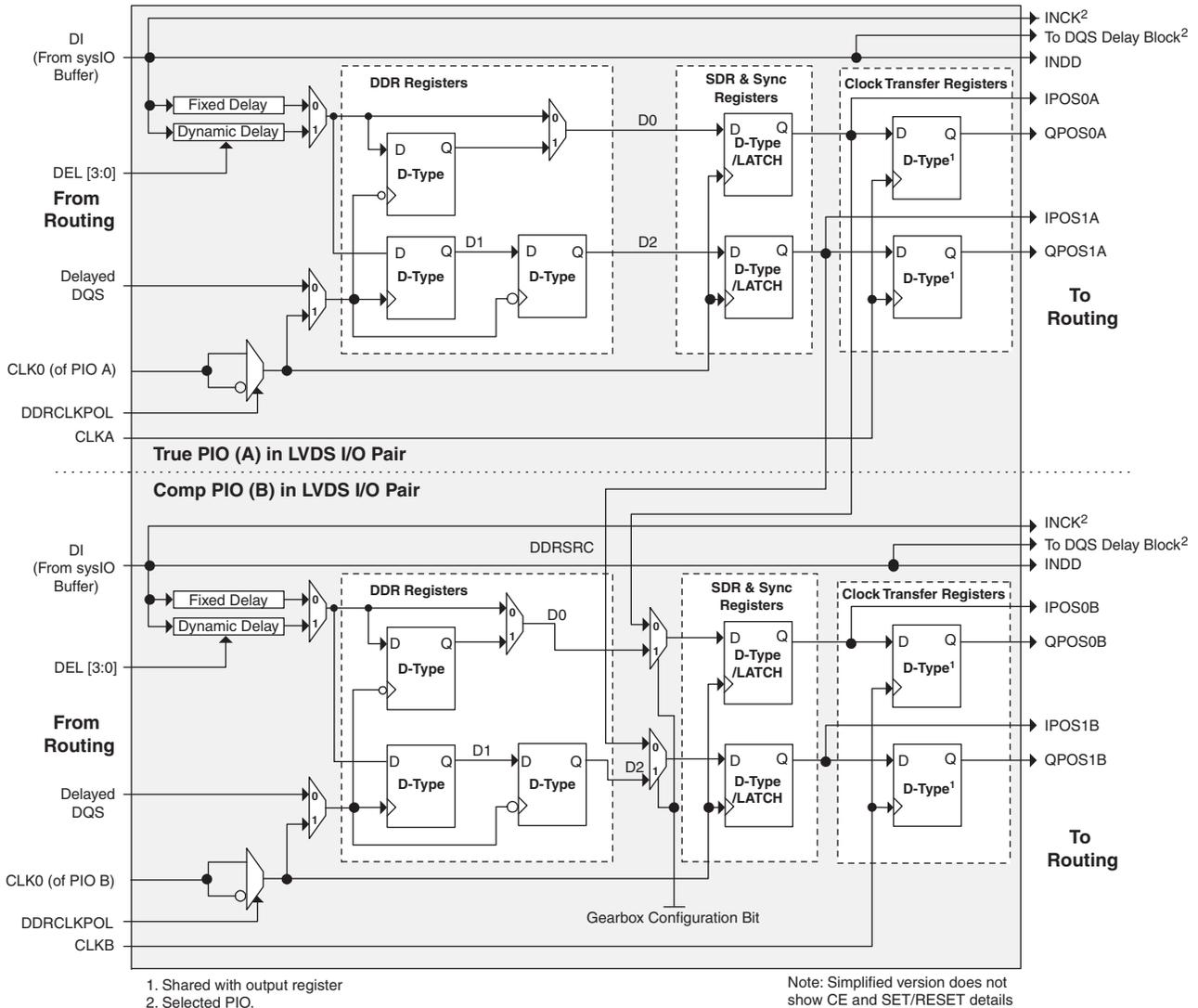
Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, [LatticeXP2 High Speed I/O Interface](#).

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Block



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. Figure 2-27 shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-27

Hot Socketing Specifications^{1, 2, 3, 4}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH} (MAX.)$	—	—	+/-1	mA

1. Insensitive to sequence of V_{CC} , V_{CCAUX} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} and V_{CCIO} .
2. $0 \leq V_{CC} \leq V_{CC} (MAX)$, $0 \leq V_{CCIO} \leq V_{CCIO} (MAX)$ or $0 \leq V_{CCAUX} \leq V_{CCAUX} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .
4. LVCMOS and LVTTTL only.

ESD Performance

Please refer to the [LatticeXP2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL} , I_{IH}^1	Input or I/O Low Leakage	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	10	μA
		$V_{CCIO} \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{CCIO}$	30	—	210	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-150	μA
V_{BHT}	Bus Hold Trip Points		$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = 1.2V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	8	—	pf
C2	Dedicated Input Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = 1.2V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, $f = 1.0$ MHz.

sysIO Recommended Operating Conditions

Over Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS33 ²	3.135	3.3	3.465	—	—	—
LVC MOS25 ²	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 ²	1.14	1.2	1.26	—	—	—
LV TTL33 ²	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL18_I ² , SSTL18_II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I ² , SSTL25_II ²	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I ² , SSTL33_II ²	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I ²	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I ² , HSTL18_II ²	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25 ²	2.375	2.5	2.625	—	—	—
MLVDS25 ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1,2}	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1,2}	2.375	2.5	2.625	—	—	—
RSDS ^{1,2}	2.375	2.5	2.625	—	—	—
SSTL18D_I ² , SSTL18D_II ²	1.71	1.8	1.89	—	—	—
SSTL25D_I ² , SSTL25D_II ²	2.375	2.5	2.625	—	—	—
SSTL33D_I ² , SSTL33D_II ²	3.135	3.3	3.465	—	—	—
HSTL15D_I ²	1.425	1.5	1.575	—	—	—
HSTL18D_I ² , HSTL18D_II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. Input on this standard does not depend on the value of V_{CCIO}.

Register-to-Register Performance (Continued)

Function	-7 Timing	Units
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	198	MHz
1024-pt FFT	221	MHz
8X8 Matrix Multiplication	196	MHz

- These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device, design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

LatticeXP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
DDR² and DDR³ I/O Pin Parameters									
t _{DVADQ}	Data Valid After DQS (DDR Read)	XP2	—	0.29	—	0.29	—	0.29	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	XP2	0.71	—	0.71	—	0.71	—	UI
t _{DQVBS}	Data Valid Before DQS	XP2	0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	XP2	0.25	—	0.25	—	0.25	—	UI
f _{MAX_DDR}	DDR Clock Frequency	XP2	95	200	95	166	95	133	MHz
f _{MAX_DDR2}	DDR Clock Frequency	XP2	133	200	133	200	133	166	MHz
Primary Clock									
f _{MAX_PRI}	Frequency for Primary Clock Tree	XP2	—	420	—	357	—	311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	XP2	1	—	1	—	1	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	XP2	—	160	—	160	—	160	ps
Edge Clock (ECLK1 and ECLK2)									
f _{MAX_ECLK}	Frequency for Edge Clock	XP2	—	420	—	357	—	311	MHz
t _{W_ECLK}	Clock Pulse Width for Edge Clock	XP2	1	—	1	—	1	—	ns
t _{SKEW_ECLK}	Edge Clock Skew Within an Edge of the Device	XP2	—	130	—	130	—	130	ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25.
3. DDR2 timing numbers based on SSTL18.

LatticeXP2 Internal Switching Characteristics¹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RST_PIO}	Asynchronous reset time for PFU Logic	—	0.386	—	0.419	—	0.452	ns
t _{DEL}	Dynamic Delay Step Size	0.035	0.035	0.035	0.035	0.035	0.035	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to Output from Address or Data	—	2.774	—	3.142	—	3.510	ns
t _{COO_EBR}	Clock (Write) to Output from EBR Output Register	—	0.360	—	0.408	—	0.456	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory (Write Clk)	-0.167	—	-0.198	—	-0.229	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory (Write Clk)	0.194	—	0.231	—	0.267	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory (Write Clk)	-0.117	—	-0.137	—	-0.157	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory (Write Clk)	0.157	—	0.182	—	0.207	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory (Write/Read Clk)	-0.135	—	-0.159	—	-0.182	—	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.158	—	0.186	—	0.214	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.144	—	0.160	—	0.176	—	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)	-0.097	—	-0.113	—	-0.129	—	ns
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchronous)	—	1.156	—	1.341	—	1.526	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.117	—	-0.137	—	-0.157	—	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.157	—	0.182	—	0.207	—	ns
t _{RSTREC_EBR}	Asynchronous reset recovery time for EBR	0.233	—	0.291	—	0.347	—	ns
t _{RST_EBR}	Asynchronous reset time for EBR	—	1.156	—	1.341	—	1.526	ns
PLL Parameters								
t _{RSTKREC_PLL}	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.000	—	1.000	—	1.000	—	ns
t _{RSTREC_PLL}	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only ²)	1.000	—	1.000	—	1.000	—	ns
DSP Block Timing								
t _{SUI_DSP}	Input Register Setup Time	0.135	—	0.151	—	0.166	—	ns
t _{HI_DSP}	Input Register Hold Time	0.021	—	-0.006	—	-0.031	—	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.505	—	2.784	—	3.064	—	ns

LatticeXP2 Family Timing Adders^{1, 2, 3, 4} (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTTL33_4mA	LVTTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTTL33_8mA	LVTTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTTL33_16mA	LVTTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

LatticeXP2 Family Timing Adders^{1, 2, 3, 4} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, slow slew rate	1.05	1.43	1.81	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, slow slew rate	0.78	1.15	1.52	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, slow slew rate	0.59	0.96	1.33	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, slow slew rate	0.81	1.18	1.55	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, slow slew rate	0.61	0.98	1.35	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, slow slew rate	1.01	1.38	1.75	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, slow slew rate	0.72	1.08	1.45	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, slow slew rate	0.53	0.90	1.26	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, slow slew rate	0.74	1.11	1.48	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, slow slew rate	0.96	1.33	1.71	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, slow slew rate	-0.53	-0.26	0.00	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, slow slew rate	0.90	1.27	1.65	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, slow slew rate	-0.55	-0.29	-0.02	ns
PCI33	3.3V PCI	-0.29	-0.01	0.26	ns

1. Timing Adders are characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. The base parameters used with these timing adders to calculate timing are listed in the LatticeXP2 Internal Switching Characteristics table under PIO Input/Output Timing.
5. These timing adders are measured with the recommended resistor values.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		10	—	435	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		10	—	435	MHz
f_{OUT2}	K-Divider Output Frequency	CLKOK	0.078	—	217.5	MHz
		CLKOK2	3.3	—	145	MHz
f_{VCO}	PLL VCO Frequency		435	—	870	MHz
f_{PFD}	Phase Detector Input Frequency		10	—	435	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t_{CPA}	Coarse Phase Adjust		-5	0	5	%
t_{PH} ⁴	Output Phase Accuracy		-5	0	5	%
t_{OPJIT} ¹	Output Clock Period Jitter	$f_{OUT} > 400$ MHz	—	—	±50	ps
		100 MHz $< f_{OUT} < 400$ MHz	—	—	±125	ps
		$f_{OUT} < 100$ MHz	—	—	0.025	UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±240	ps
t_{OPW}	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK} ²	PLL Lock-in Time	25 to 435 MHz	—	—	50	μs
		10 to 25 MHz	—	—	100	μs
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDL}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RSTKW}	Reset Signal Pulse Width (RSTK)		10	—	—	ns
t_{RSTW}	Reset Signal Pulse Width (RST)		500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.

FlashBAK Time (from EBR to Flash)

Over Recommended Operating Conditions

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	s
XP2-8	221K	1.5	s
XP2-17	276K	1.5	s
XP2-30	387K	2.0	s
XP2-40	885K	3.0	s

JTAG Port Timing Specifications

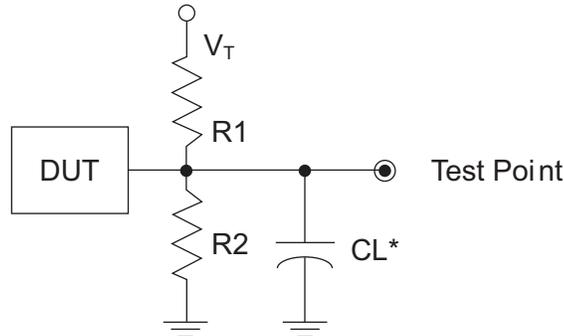
Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Switching Test Conditions

Figure 3-11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-11. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ		V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100		V _{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	30
LFXP2-30E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	30
LFXP2-30E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	30
LFXP2-30E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	30
LFXP2-30E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	30
LFXP2-30E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	30
LFXP2-30E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	30
LFXP2-30E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	30
LFXP2-30E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	40
LFXP2-40E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	40
LFXP2-40E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	40
LFXP2-40E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	40
LFXP2-40E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	40
LFXP2-40E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	40

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	5
LFXP2-5E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	5
LFXP2-5E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	5
LFXP2-5E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	5
LFXP2-5E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	5
LFXP2-5E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	5
LFXP2-5E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	5
LFXP2-5E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	8
LFXP2-8E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	8
LFXP2-8E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	8
LFXP2-8E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	8
LFXP2-8E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	8
LFXP2-8E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	8
LFXP2-8E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	8
LFXP2-8E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	8

For Further Information

A variety of technical notes for the LatticeXP2 FPGA family are available on the Lattice Semiconductor web site at www.latticesemi.com.

- TN1136, [LatticeXP2 sysIO Usage Guide](#)
- TN1137, [LatticeXP2 Memory Usage Guide](#)
- TN1138, [LatticeXP2 High Speed I/O Interface](#)
- TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#)
- TN1139, [Power Estimation and Management for LatticeXP2 Devices](#)
- TN1140, [LatticeXP2 sysDSP Usage Guide](#)
- TN1141, [LatticeXP2 sysCONFIG Usage Guide](#)
- TN1142, [LatticeXP2 Configuration Encryption and Security Usage Guide](#)
- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- TN1220, [LatticeXP2 Dual Boot Feature](#)
- TN1130, [LatticeXP2 Soft Error Detection \(SED\) Usage Guide](#)
- TN1143, [LatticeXP2 Hardware Checklist](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com