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## Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	86
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-6mn132c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-6mn132c</a>

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## Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-4. General Purpose PLL (GPLL) Diagram**

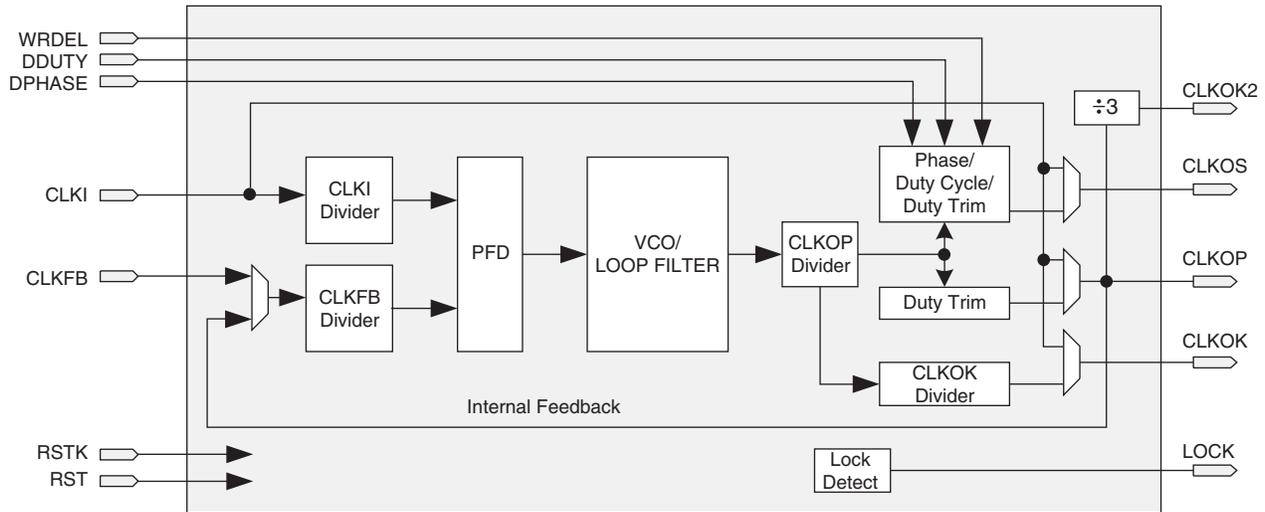


Table 2-4 provides a description of the signals in the GPLL blocks.

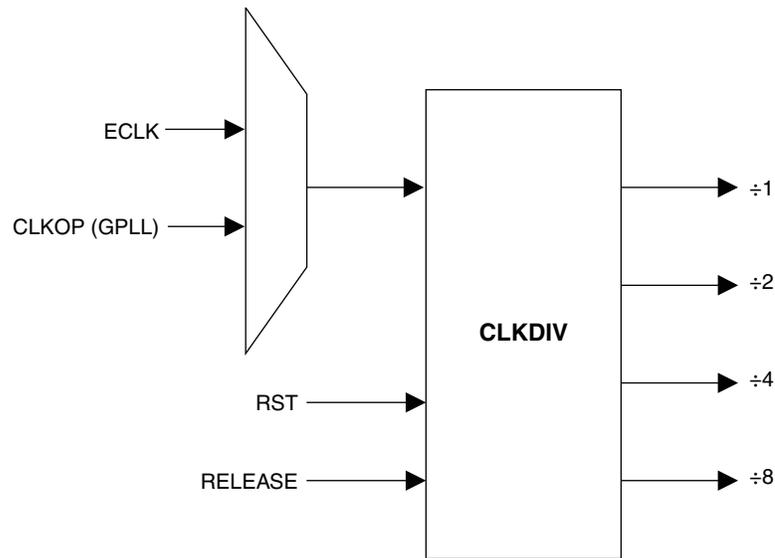
**Table 2-4. GPLL Block Signal Descriptions**

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI

## Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a  $\div 2$ ,  $\div 4$  or  $\div 8$  mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#). Figure 2-5 shows the clock divider connections.

Figure 2-5. Clock Divider Connections



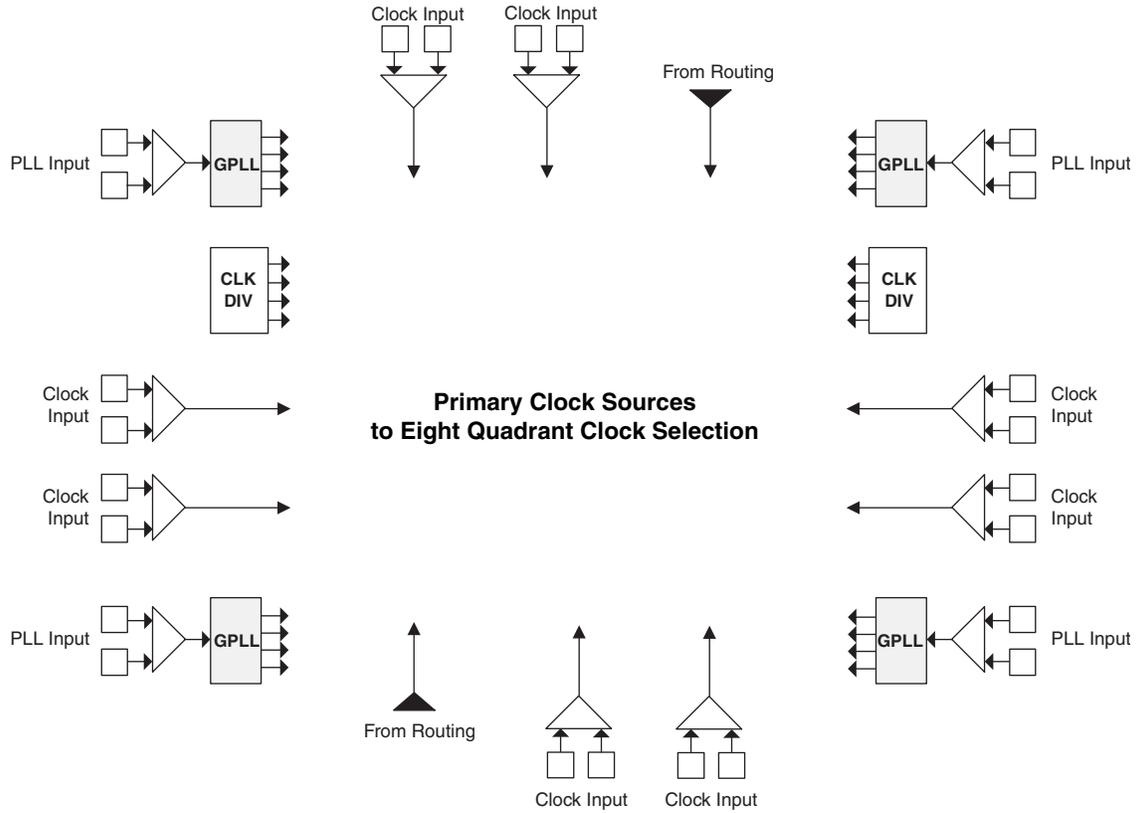
## Clock Distribution Network

LatticeXP2 devices have eight quadrant-based primary clocks and between six and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. The clock inputs are selected from external I/Os, the sysCLOCK PLLs, or routing. Clock inputs are fed throughout the chip via the primary, secondary and edge clock networks.

## Primary Clock Sources

LatticeXP2 devices derive primary clocks from four sources: PLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeXP2 devices have two to four sysCLOCK PLLs, located in the four corners of the device. There are eight dedicated clock inputs, two on each side of the device. Figure 2-6 shows the primary clock sources.

**Figure 2-6. Primary Clock Sources for XP2-17**



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.

LatticeXP2-30 and smaller devices have six secondary clock regions. All devices in the LatticeXP2 family have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-12 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

**Figure 2-11. Secondary Clock Regions XP2-40**

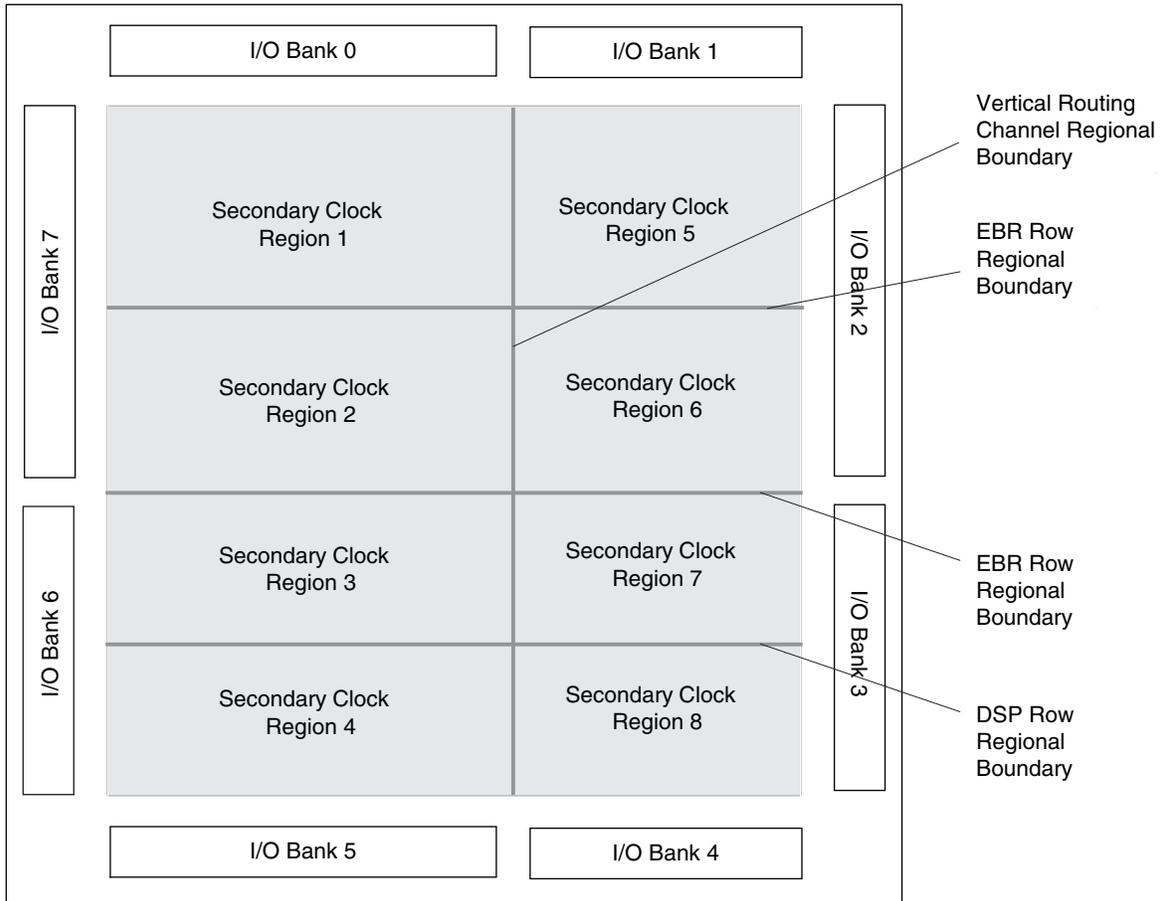
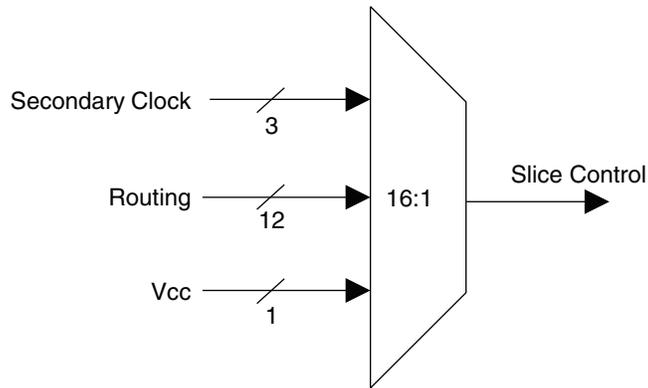


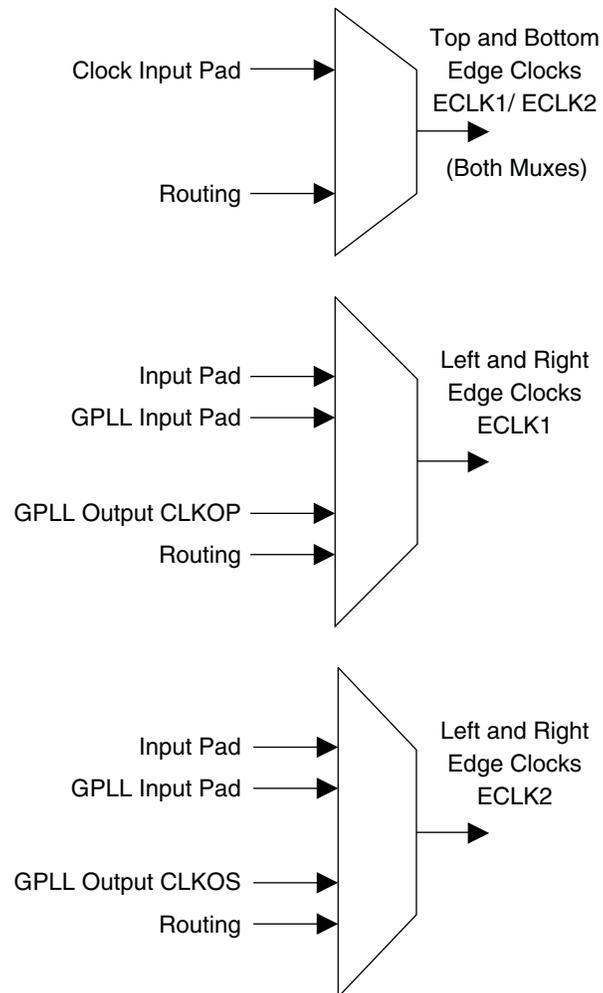
Figure 2-14. Slice0 through Slice2 Control Selection



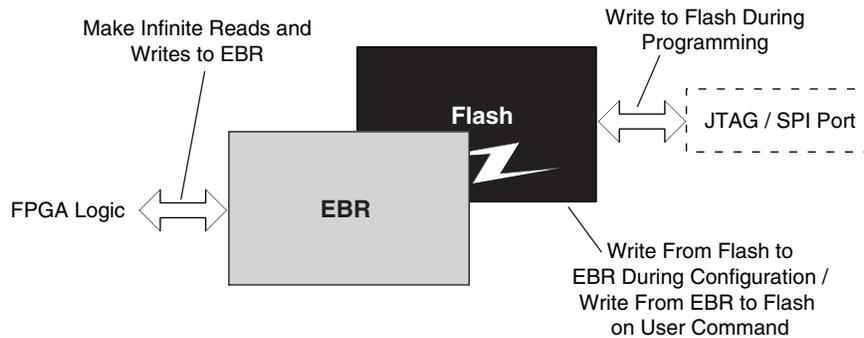
### Edge Clock Routing

LatticeXP2 devices have eight high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. Each device has two edge clocks per edge. Figure 2-15 shows the selection muxes for these clocks.

Figure 2-15. Edge Clock Mux Connections



**Figure 2-16. FlashBAK Technology**



## Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

## Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

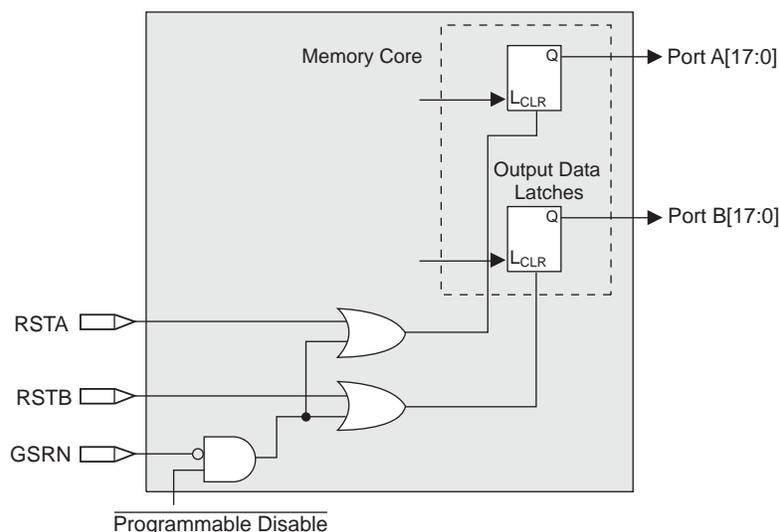
EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

**Figure 2-17. Memory Core Reset**



register. Similarly, CE and RST are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

### Signed and Unsigned with Different Widths

The DSP block supports other widths, in addition to x9, x18 and x36 widths, of signed and unsigned multipliers. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-7 provides an example of this.

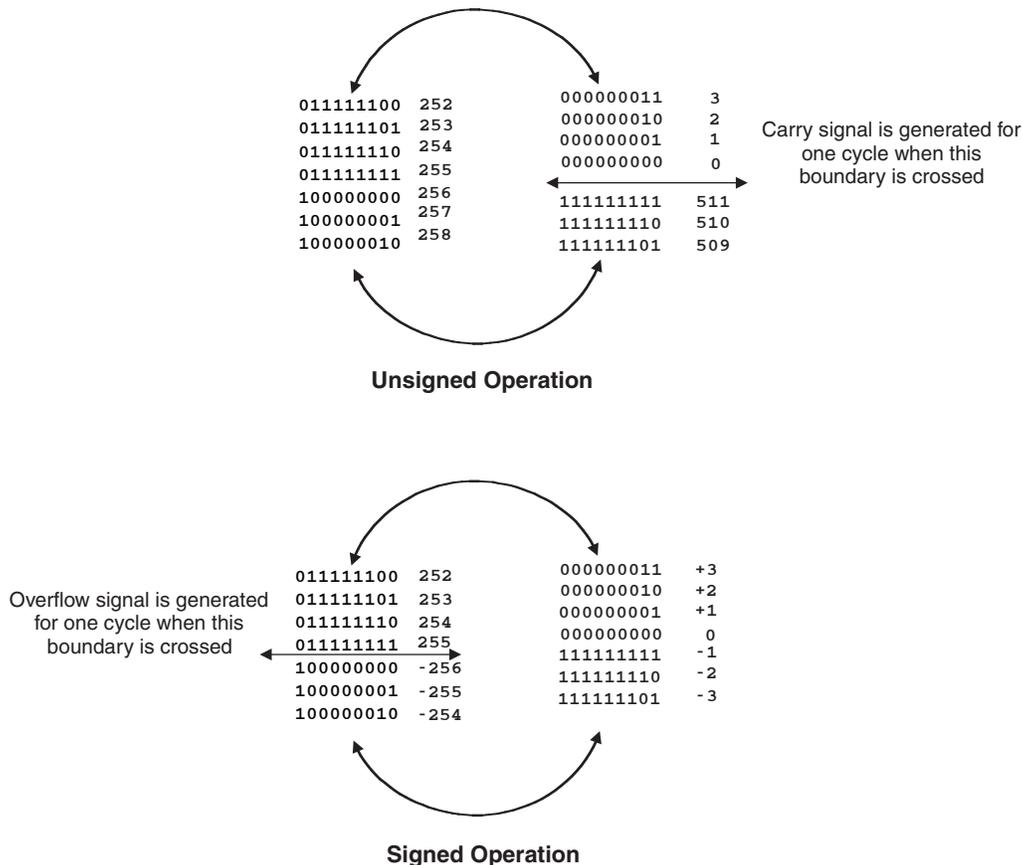
**Table 2-7. Sign Extension Example**

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	0000000000000000101	0101	000000101	0000000000000000101
-6	N/A	N/A	N/A	1010	11111010	111111111111111010

### OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. "Roll-over" occurs and an overflow signal is indicated when any of the following is true: two unsigned numbers are added and the result is a smaller number than the accumulator, two positive numbers are added with a negative sum or two negative numbers are added with a positive sum. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions for the overflow signal for signed and unsigned operands are listed in Figure 2-24.

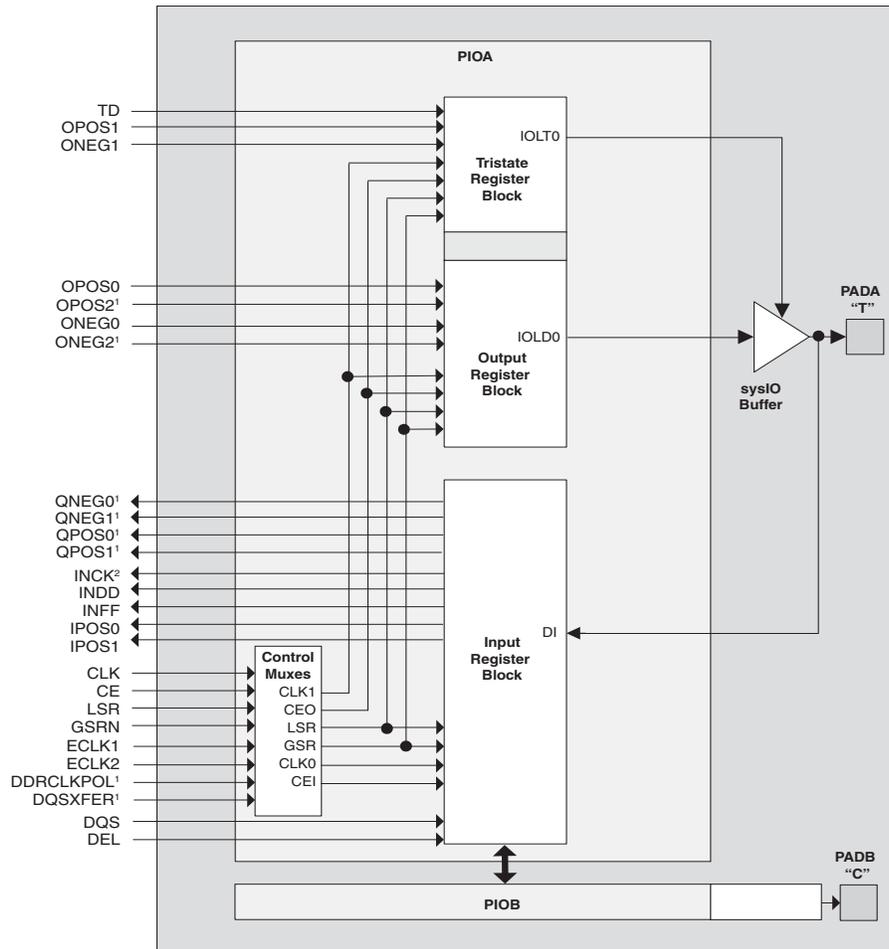
**Figure 2-24. Accumulator Overflow/Underflow**



## Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-25. PIC Diagram



1. Signals are available on left/right/bottom edges only.
2. Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-25. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

**Supply Current (Standby)<sup>1, 2, 3, 4</sup>**
**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typical <sup>5</sup>	Units
$I_{CC}$	Core Power Supply Current	XP2-5	14	mA
		XP2-8	18	mA
		XP2-17	24	mA
		XP2-30	35	mA
		XP2-40	45	mA
$I_{CCAUX}$	Auxiliary Power Supply Current <sup>6</sup>	XP2-5	15	mA
		XP2-8	15	mA
		XP2-17	15	mA
		XP2-30	16	mA
		XP2-40	16	mA
$I_{CCPLL}$	PLL Power Supply Current (per PLL)		0.1	mA
$I_{CCIO}$	Bank Power Supply Current (per bank)		2	mA
$I_{CCJ}$	$V_{CCJ}$ Power Supply Current		0.25	mA

1. For further information on supply current, please see TN1139, [Power Estimation and Management for LatticeXP2 Devices](#).
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the  $V_{CCIO}$  or GND.
3. Frequency 0 MHz.
4. Pattern represents a "blank" configuration data file.
5.  $T_J = 25^\circ\text{C}$ , power supplies at nominal voltage.
6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of  $I_{CCAUX}$  and  $I_{CCPLL}$ . For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

**Initialization Supply Current<sup>1, 2, 3, 4, 5</sup>**
**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typical (25°C, Max. Supply) <sup>6</sup>	Units
$I_{CC}$	Core Power Supply Current	XP2-5	20	mA
		XP2-8	21	mA
		XP2-17	44	mA
		XP2-30	58	mA
		XP2-40	62	mA
$I_{CCAUX}$	Auxiliary Power Supply Current <sup>7</sup>	XP2-5	67	mA
		XP2-8	74	mA
		XP2-17	112	mA
		XP2-30	124	mA
		XP2-40	130	mA
$I_{CCPLL}$	PLL Power Supply Current (per PLL)		1.8	mA
$I_{CCIO}$	Bank Power Supply Current (per Bank)		6.4	mA
$I_{CCJ}$	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, please see TN1139, [Power Estimation and Management for LatticeXP2 Devices](#).

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the  $V_{CCIO}$  or GND.

3. Frequency 0 MHz.

4. Does not include additional current from bypass or decoupling capacitor across the supply.

5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

6.  $T_J = 25^\circ\text{C}$ , power supplies at nominal voltage.

7. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of  $I_{CCAUX}$  and  $I_{CCPLL}$ . For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

## sysIO Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}^1$ (mA)	$I_{OH}^1$ (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)		
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS18	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS15	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS12	-0.3	$0.35 V_{CC}$	$0.65 V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI33	-0.3	$0.3 V_{CCIO}$	$0.5 V_{CCIO}$	3.6	$0.1 V_{CCIO}$	$0.9 V_{CCIO}$	1.5	-0.5
SSTL33_I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL33_II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL25_I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
							12	-12
SSTL25_II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
							20	-20
SSTL18_I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
SSTL18_II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.28	$V_{CCIO} - 0.28$	8	-8
							11	-11
HSTL15_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
HSTL18_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
							12	-12
HSTL18_II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed  $n * 8mA$ , where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

## sysIO Differential Electrical Characteristics

### LVDS

#### Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}$ $V_{INM}$	Input Voltage		0	—	2.4	V
$V_{CM}$	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
$V_{THD}$	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
$I_{IN}$	Input Current	Power On or Power Off	—	—	+/-10	$\mu$ A
$V_{OH}$	Output High Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	—	1.38	1.60	V
$V_{OL}$	Output Low Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	0.9V	1.03	—	V
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM})$ , $R_T = 100$ Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Between High and Low		—	—	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2$ , $R_T = 100$ Ohm	1.125	1.20	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ Between H and L		—	—	50	mV
$I_{SA}$	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Ground	—	—	24	mA
$I_{SAB}$	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Each Other	—	—	12	mA

### Differential HSTL and SSTL

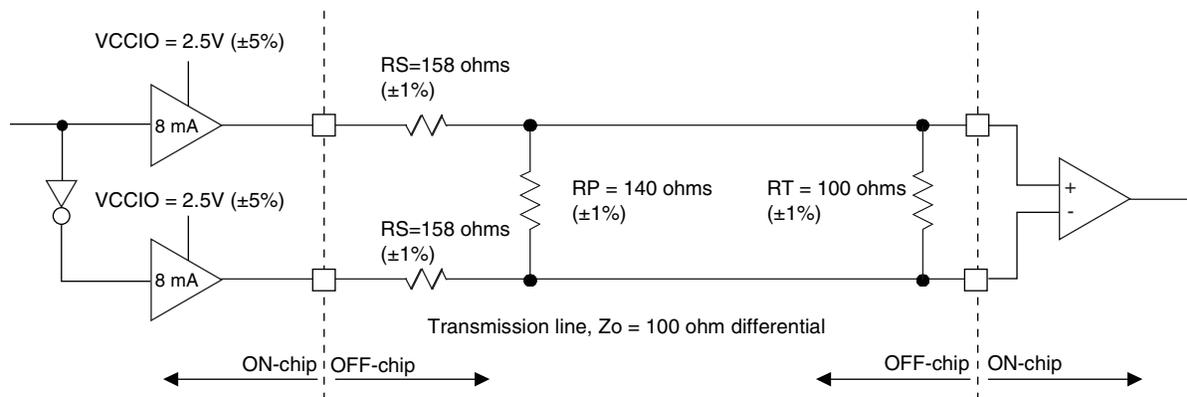
Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

### LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example



## LVPECL

The LatticeXP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

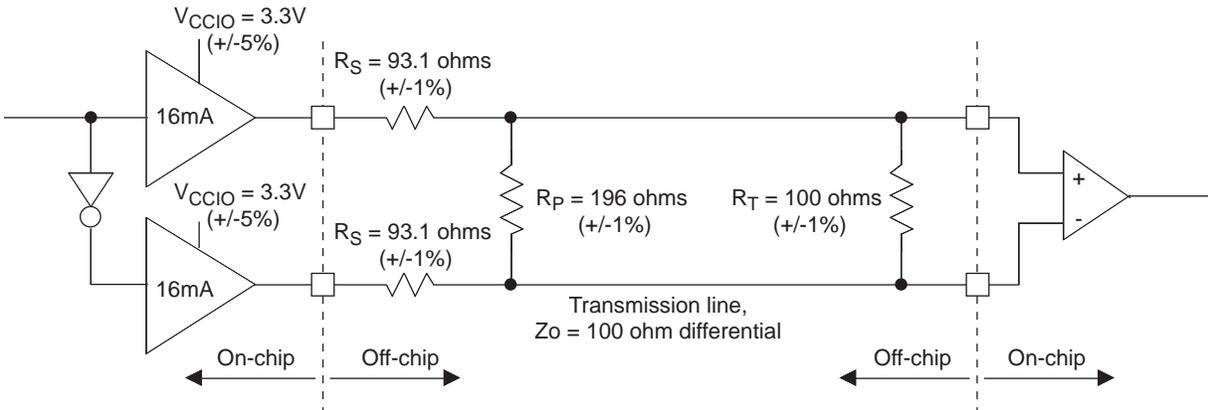


Table 3-3. LVPECL DC Conditions<sup>1</sup>

### Over Recommended Operating Conditions

Parameter	Description	Typical	Units
$V_{CCIO}$	Output Driver Supply (+/-5%)	3.30	V
$Z_{OUT}$	Driver Impedance	10	$\Omega$
$R_S$	Driver Series Resistor (+/-1%)	93	$\Omega$
$R_P$	Driver Parallel Resistor (+/-1%)	196	$\Omega$
$R_T$	Receiver Termination (+/-1%)	100	$\Omega$
$V_{OH}$	Output High Voltage (After $R_P$ )	2.05	V
$V_{OL}$	Output Low Voltage (After $R_P$ )	1.25	V
$V_{OD}$	Output Differential Voltage (After $R_P$ )	0.80	V
$V_{CM}$	Output Common Mode Voltage	1.65	V
$Z_{BACK}$	Back Impedance	100.5	$\Omega$
$I_{DC}$	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

**LatticeXP2 Family Timing Adders<sup>1, 2, 3, 4</sup> (Continued)**

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTTL33_4mA	LVTTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTTL33_8mA	LVTTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTTL33_16mA	LVTTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

## Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Units
t <sub>REFRESH</sub>	PROGRAMN Low-to-High. Transition to Done High.	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms
	Power-up refresh when PROGRAMN is pulled up to V <sub>CC</sub> (V <sub>CC</sub> =V <sub>CC</sub> Min)	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms

## Flash Program Time

Over Recommended Operating Conditions

Device	Flash Density		Program Time		Units
			Typ.		
XP2-5	1.2M	TAG	1.0		ms
		Main Array	1.1		s
XP2-8	2.0M	TAG	1.0		ms
		Main Array	1.4		s
XP2-17	3.6M	TAG	1.0		ms
		Main Array	1.8		s
XP2-30	6.0M	TAG	2.0		ms
		Main Array	3.0		s
XP2-40	8.0M	TAG	2.0		ms
		Main Array	4.0		s

## Flash Erase Time

Over Recommended Operating Conditions

Device	Flash Density		Erase Time		Units
			Typ.		
XP2-5	1.2M	TAG	1.0		s
		Main Array	3.0		s
XP2-8	2.0M	TAG	1.0		s
		Main Array	4.0		s
XP2-17	3.6M	TAG	1.0		s
		Main Array	5.0		s
XP2-30	6.0M	TAG	2.0		s
		Main Array	7.0		s
XP2-40	8.0M	TAG	2.0		s
		Main Array	9.0		s

### Signal Descriptions

Signal Name	I/O	Description
<b>General Purpose</b>		
P[Edge] [Row/Column Number*]_[A/B]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p>
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V <sub>CC</sub>	—	Power supply pins for core logic. Dedicated pins.
V <sub>CCAUX</sub>	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V <sub>CCPLL</sub>	—	PLL supply pins. csBGA, PQFP and TQFP packages only.
V <sub>CCIOx</sub>	—	Dedicated power supply pins for I/O bank x.
V <sub>REF1_x</sub> , V <sub>REF2_x</sub>	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V <sub>REF</sub> inputs. When not used, they may be used as I/O pins.
<b>PLL and Clock Functions</b> (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V <sub>CCPLL</sub>	—	Power supply pin for PLL: LLC, LRC, URC, ULC, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
<b>Test and Programming (Dedicated Pins)</b>		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.

## Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
<b>Configuration Pads (Used during sysCONFIG)</b>		
CFG[1:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN <sup>1</sup>	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI <sup>2</sup>	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI <sup>2</sup>	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN <sup>2</sup>	O	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V <sub>CC</sub> is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10k $\Omega$  is recommended.
2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

**Lead-Free Packaging**
**Commercial**

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17

## For Further Information

A variety of technical notes for the LatticeXP2 FPGA family are available on the Lattice Semiconductor web site at [www.latticesemi.com](http://www.latticesemi.com).

- TN1136, [LatticeXP2 sysIO Usage Guide](#)
- TN1137, [LatticeXP2 Memory Usage Guide](#)
- TN1138, [LatticeXP2 High Speed I/O Interface](#)
- TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#)
- TN1139, [Power Estimation and Management for LatticeXP2 Devices](#)
- TN1140, [LatticeXP2 sysDSP Usage Guide](#)
- TN1141, [LatticeXP2 sysCONFIG Usage Guide](#)
- TN1142, [LatticeXP2 Configuration Encryption and Security Usage Guide](#)
- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- TN1220, [LatticeXP2 Dual Boot Feature](#)
- TN1130, [LatticeXP2 Soft Error Detection \(SED\) Usage Guide](#)
- TN1143, [LatticeXP2 Hardware Checklist](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): [www.jedec.org](http://www.jedec.org)
- PCI: [www.pcisig.com](http://www.pcisig.com)