

Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-6tn144i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



LatticeXP2 Family Data Sheet Architecture

August 2014

Data Sheet DS1009

Architecture Overview

Each LatticeXP2 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and a row of sys-DSP[™] Digital Signal Processing blocks as shown in Figure 2-1.

On the left and right sides of the Programmable Functional Unit (PFU) array, there are Non-volatile Memory Blocks. In configuration mode the nonvolatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG[™] peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memory is not required, and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an "instant-on" capability that allows easy interfacing in many applications. LatticeXP2 devices can also transfer data from the sysMEM EBR blocks to the Non-volatile Memory Blocks at user request.

There are two kinds of logic blocks, the PFU and the PFU without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

LatticeXP2 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18Kbit memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeXP2 devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO buffers. The sysIO buffers of the LatticeXP2 devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as 7:1 LVDS interfaces, found in many display applications, and memory interfaces including DDR and DDR2.

The LatticeXP2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

Other blocks provided include PLLs and configuration functions. The LatticeXP2 architecture provides up to four General Purpose PLLs (GPLL) per device. The GPLL blocks are located in the corners of the device.

The configuration block that supports features such as configuration bit-stream de-encryption, transparent updates and dual boot support is located between banks two and three. Every device in the LatticeXP2 family supports a sysCONFIG port, muxed with bank seven I/Os, which supports serial device configuration. A JTAG port is provided between banks two and three.

This family also provides an on-chip oscillator. LatticeXP2 devices use 1.2V as their core voltage.

^{© 2014} Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Figure 2-4. General Purpose PLL (GPLL) Diagram



Table 2-4 provides a description of the signals in the GPLL blocks.

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	0	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	0	PLL output clock to clock tree (no phase shift)
CLKOK	0	PLL output to clock tree through secondary clock divider
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)
LOCK	0	"1" indicates PLL LOCK to CLKI

Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs and clock dividers as shown in Figure 2-8.

Figure 2-8. Edge Clock Sources



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.



sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

FlashBAK EBR Content Storage

All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.



Table 2-11. PIO Signal List

Name	Туре	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, LatticeXP2 High Speed I/O Interface.



The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.





Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. Figure 2-27 shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-27



shows the diagram using this gearbox function. For more information on this topic, see TN1138, <u>LatticeXP2 High</u> <u>Speed I/O Interface</u>.







Figure 2-28. DQS Input Routing (Left and Right)

	PIO A		PADA "T"
	PIO B		PADB "C"
	PIO A		PADA "T"
	PIO B	· · · · ·	PADB "C"
	PIO A		PADA "T"
	PIO B	↓+	PADB "C"
	PIO A		PADA "T"
	PIO B	┃┣	PADB "C"
DOG	PIO A	sysIO Buffer	
 ■ DQ5 		Delay	LVDS Pair
+ DQS	PIO B	Delay	LVDS Pair
↓ DQS	PIO B PIO A		PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
	→ PIO B → PIO A → PIO B		PADA "1" LVDS Pair PADB "C" PADA "T" LVDS Pair LVDS Pair PADA "C"
			PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
			PADA T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair LVDS Pair PADB "C"
			PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"

Figure 2-29. DQS Input Routing (Top and Bottom)

	PIO A		PADA "T"
	PIO B	+	PADB "C"
	PIO A		PADA "T"
	PIO B	· · · · ·	PADB "C"
—	PIO A		PADA "T" LVDS Pair
	PIO B	→	PADB "C"
	PIO A		PADA "T"
<u> </u>	PIO B	→	PADB "C"
	PIO A	syslO Buffer	·
DQS		Palay	
•		Delay	LVDS Pair
	PIO B		LVDS Pair I I PADB "C" I
	PIO B PIO A		LVDS Pair I PADB "C"
	→ PIO B → PIO A → PIO B		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"
	→ PIO B → PIO A → PIO B → PIO A		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
	→ PIO B → PIO A → PIO B → PIO A → PIO B		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair I PADA "T" PADA "C"
	→ PIO B → PIO A → PIO A → PIO A → PIO A → PIO B → PIO A		LVDS Pair PADA "T" LVDS Pair PADA "T" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADA "T" LVDS Pair
			LVDS Pair PADA "T" LVDS Pair PADA "T" PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"
			LVDS Pair PADA "T" LVDS Pair PADB "C" PADB "C" PADB "C" PADB "C" PADB "C" PADB "C" PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADA "T" LVDS Pair



- 1. Unlocked
- 2. Key Locked Presenting the key through the programming interface allows the device to be unlocked.
- 3. Permanently Locked The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is always accessible regardless of the device security settings. For more information, see TN1137, LatticeXP2 Memory Usage Guide and TN1141, LatticeXP2 sysCONFIG Usage Guide.

Figure 2-34. Serial TAG Memory Diagram



Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. **Decryption Support**

LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1087, <u>Minimizing System Interruption During Configuration</u>. Using TransFR Technology.

3. Dual Boot Image Support

Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the



Initialization Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
		XP2-5	20	mA
		XP2-8	21	mA
I _{CC}	Core Power Supply Current	XP2-17	44	mA
		XP2-30	58	mA
		XP2-40	62	mA
		XP2-5	67	mA
ICCAUX	Auxiliary Power Supply Current ⁷	XP2-8	74	mA
		XP2-17	112	mA
		XP2-30	124	mA
		XP2-40	130	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		1.8	mA
I _{CCIO}	Bank Power Supply Current (per Bank)		6.4	mA
ICCJ	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Does not include additional current from bypass or decoupling capacitor across the supply.

5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

6. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual
auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the
auxiliary power supply.



Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (after R _P)	1.43	V
V _{OL}	Output Low Voltage (after R _P)	1.07	V
V _{OD}	Output Differential Voltage (After R _P)	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.



MLVDS

The LatticeXP2 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.





Table 3-5. MLVDS DC Conditions¹

		Typical		
Parameter	Description	Ζο=50 Ω	Ζο=70 Ω	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R _{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R _{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V _{OH}	Output High Voltage (After R _{TL})	1.52	1.60	V
V _{OL}	Output Low Voltage (After R _{TL})	0.98	0.90	V
V _{OD}	Output Differential Voltage (After R _{TL})	0.54	0.70	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.



LatticeXP2 Internal Switching Characteristics¹ (Continued)

		-7 -6		-5				
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{RST_PIO}	Asynchronous reset time for PFU Logic	—	0.386	—	0.419	—	0.452	ns
t _{DEL}	Dynamic Delay Step Size	0.035	0.035	0.035	0.035	0.035	0.035	ns
EBR Timing	· · · · · ·							
t _{CO_EBR}	Clock (Read) to Output from Address or Data	_	2.774	_	3.142	_	3.510	ns
t _{COO_EBR}	Clock (Write) to Output from EBR Output Register	_	0.360	_	0.408	—	0.456	ns
^t SUDATA_EBR	Setup Data to EBR Memory (Write Clk)	-0.167	—	-0.198	_	-0.229	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory (Write Clk)	0.194	—	0.231	_	0.267	_	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory (Write Clk)	-0.117	—	-0.137	_	-0.157	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory (Write Clk)	0.157	_	0.182	_	0.207	_	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory (Write/Read Clk)	-0.135	_	-0.159	_	-0.182	_	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.158	—	0.186	_	0.214	_	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.144	—	0.160	_	0.176	_	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)	-0.097	—	-0.113	_	-0.129	_	ns
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchro- nous)	_	1.156	_	1.341	_	1.526	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.117	—	-0.137	_	-0.157	_	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.157	_	0.182	_	0.207	_	ns
t _{RSTREC_EBR}	Asynchronous reset recovery time for EBR	0.233	—	0.291		0.347	—	ns
t _{RST_EBR}	Asynchronous reset time for EBR	—	1.156	—	1.341	_	1.526	ns
PLL Paramete	ers							
t _{RSTKREC_PLL}	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.000	_	1.000	_	1.000	_	ns
t _{RSTREC_PLL}	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only ²)	1.000	_	1.000		1.000	_	ns
DSP Block Tir	ning							
t _{SUI_DSP}	Input Register Setup Time	0.135		0.151		0.166		ns
t _{HI_DSP}	Input Register Hold Time	0.021	—	-0.006	—	-0.031		ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.505	—	2.784	—	3.064	—	ns

Over Recommended Operating Conditions



LatticeXP2 Internal Switching Characteristics¹ (Continued)

		-7		-6		-5		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HP_DSP}	Pipeline Register Hold Time	-0.787	_	-0.890	_	-0.994	_	ns
t _{SUO_DSP}	Output Register Setup Time	4.896	—	5.413	—	5.931	—	ns
t _{HO_DSP}	Output Register Hold Time	-1.439	—	-1.604	—	-1.770	—	ns
t _{COI_DSP} ³	Input Register Clock to Output Time	_	4.513	—	4.947	—	5.382	ns
t _{COP_DSP} ³	Pipeline Register Clock to Output Time	_	2.153	—	2.272	—	2.391	ns
t _{COO_DSP} ³	Output Register Clock to Output Time	_	0.569	—	0.600	—	0.631	ns
t _{SUADSUB}	AdSub Input Register Setup Time	-0.270	—	-0.298	_	-0.327	—	ns
t _{HADSUB}	AdSub Input Register Hold Time	0.306	—	0.338	—	0.371	—	ns

Over Recommended Operating Conditions

1. Internal parameters are characterized, but not tested on every device.

2. RST resets VCO and all counters in PLL.

3. These parameters include the Adder Subtractor block in the path.







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



LatticeXP2 sysCONFIG Port Timing Specifications

Parameter	Description	Min	Max	Units					
sysCONFIG PO	sysCONFIG POR, Initialization and Wake Up								
t _{ICFG}	Minimum Vcc to INITN High	_	50	ms					
t _{VMC}	Time from t _{ICFG} to valid Master CCLK	_	2	μs					
t _{PRGMRJ}	PROGRAMN Pin Pulse Rejection	_	12	ns					
t _{PRGM}	PROGRAMN Low Time to Start Configuration	50	—	ns					
t _{DINIT} 1	PROGRAMN High to INITN High Delay	_	1	ms					
t _{DPPINIT}	Delay Time from PROGRAMN Low to INITN Low	_	50	ns					
t _{DPPDONE}	Delay Time from PROGRAMN Low to DONE Low	_	50	ns					
t _{IODISS}	User I/O Disable from PROGRAMN Low	_	35	ns					
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	_	25	ns					
t _{MWC}	Additional Wake Master Clock Signals after DONE Pin High	0	—	Cycles					
sysCONFIG SP	I Port (Master)								
t _{CFGX}	INITN High to CCLK Low	_	1	μs					
t _{CSSPI}	INITN High to CSSPIN Low	_	2	μs					
t _{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns					
t _{SOCDO}	CCLK Low to Output Valid	_	15	ns					
t _{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	2cyc	600+6cyc	ns					
f _{MAXSPI}	Max CCLK Frequency	—	20	MHz					
t _{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns					
t _{HSPI}	SOSPI Data Hold Time After CCLK	10	—	ns					
sysCONFIG SP	I Port (Slave)								
f _{MAXSPIS}	Slave CCLK Frequency	—	25	MHz					
t _{RF}	Rise and Fall Time	50	—	mV/ns					
t _{STCO}	Falling Edge of CCLK to SOSPI Active	—	20	ns					
t _{STOZ}	Falling Edge of CCLK to SOSPI Disable	—	20	ns					
t _{STSU}	Data Setup Time (SISPI)	8	—	ns					
t _{STH}	Data Hold Time (SISPI)	10	—	ns					
t _{sтскн}	CCLK Clock Pulse Width, High	0.02	200	μs					
t _{STCKL}	CCLK Clock Pulse Width, Low	0.02	200	μs					
t _{STVO}	Falling Edge of CCLK to Valid SOSPI Output		20	ns					
t _{SCS}	CSSPISN High Time	25	—	ns					
t _{SCSS}	CSSPISN Setup Time	25	—	ns					
t _{SCSH}	CSSPISN Hold Time	25	—	ns					

Over Recommended Operating Conditions

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of PROGRAMN.



On-Chip Oscillator and Configuration Master Clock Characteristics

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value -30%	Selected value +30%	MHz
Duty Cycle	40	60	%

Over Recommended Operating Conditions

Figure 3-9. Master SPI Configuration Waveforms





Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parar	neter	Min.	Тур.	Max.	Units
	PROGRAMN Low-to-	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
*	High. Transition to Done	XP2-17	—	1.7	2.0	ms
	High.	XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms
'REFRESH	Power-up refresh when PROGRAMN is pulled	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
	$(V_{CC}=V_{CC} Min)$	XP2-30	—	2.0	2.1	ms
		XP2-40		2.0	2.3	ms

Flash Program Time

Over Recommended Operating Conditions

			Program Time	
Device	Flash Density		Тур.	Units
	1.0M	TAG	1.0	ms
XF2-5	1.2101	Main Array	1.1	S
XP2-8 2.	2.0M	TAG	1.0	ms
	2.0101	Main Array	1.4	S
XP2-17	3.6M	TAG	1.0	ms
		Main Array	1.8	S
	6.014	TAG	2.0	ms
XF2-30	0.0101	Main Array	3.0	S
VP2 40	8 OM	TAG	2.0	ms
AF2-4U	0.000	Main Array	4.0	S

Flash Erase Time

Over Recommended Operating Conditions

	Flash Density		Erase Time	
Device			Тур.	Units
YP2_5	1.2M	TAG	1.0	s
XI 2-3	1.2101	Main Array	3.0	s
XP2-8	2.0M	TAG	1.0	S
	2.0101	Main Array	4.0	s
VD0 17	3.6M	TAG	1.0	s
XI 2-17		Main Array	5.0	S
XD2-30	6 OM	TAG	2.0	s
XI 2-30	0.0101	Main Array	7.0	s
XP2-40	8.0M	TAG	2.0	S
	8.0101	Main Array	9.0	S



Switching Test Conditions

Figure 3-11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-11. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

 Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	CL	Timing Ref.	V _T
				LVCMOS 3.3 = 1.5V	
LVTTL and other LVCMOS settings (L -> H, H -> L)				LVCMOS 2.5 = $V_{CCIO}/2$	
	∞	∞	0pF	LVCMOS 1.8 = V _{CCIO} /2	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = V _{CCIO} /2	_
LVCMOS 2.5 I/O (Z -> H)	8	1MΩ		V _{CCIO} /2	
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	8	100		V _{OH} - 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	17
LFXP2-17E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	17
LFXP2-17E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	17
LFXP2-17E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFXP2-17E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	17
LFXP2-17E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	30
LFXP2-30E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	30
LFXP2-30E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	30
LFXP2-30E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	30
LFXP2-30E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	30
LFXP2-30E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	40
LFXP2-40E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	40
LFXP2-40E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	40
LFXP2-40E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	40