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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1000 |
| Number of Logic Elements/Cells | 8000 |
| Total RAM Bits | 226304 |
| Number of I/O | 201 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-7ft256c |

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Four-input logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

### Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

### RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeXP2 devices, please see TN1137, LatticeXP2 Memory Usage Guide.

***Table 2-3. Number of Slices Required For Implementing Distributed RAM***

| | SPR 16X4 | PDPR 16X4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

### ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

## Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

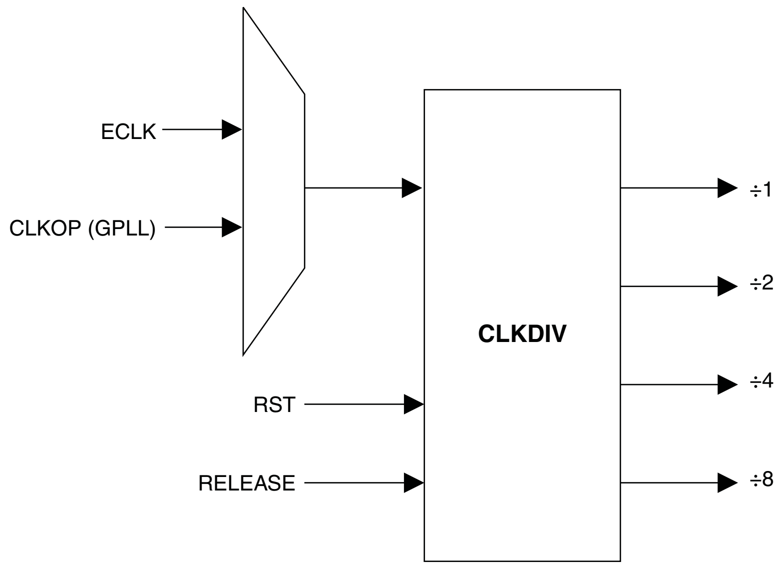
Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.

*Figure 2-5. Clock Divider Connections*




## Clock Distribution Network

LatticeXP2 devices have eight quadrant-based primary clocks and between six and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. The clock inputs are selected from external I/Os, the sysCLOCK PLLs, or routing. Clock inputs are fed throughout the chip via the primary, secondary and edge clock networks.

### Primary Clock Sources

LatticeXP2 devices derive primary clocks from four sources: PLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeXP2 devices have two to four sysCLOCK PLLs, located in the four corners of the device. There are eight dedicated clock inputs, two on each side of the device. Figure 2-6 shows the primary clock sources.

## Secondary Clock/Control Sources

LatticeXP2 devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-7 shows the secondary clock sources.

***Figure 2-7. Secondary Clock Sources***

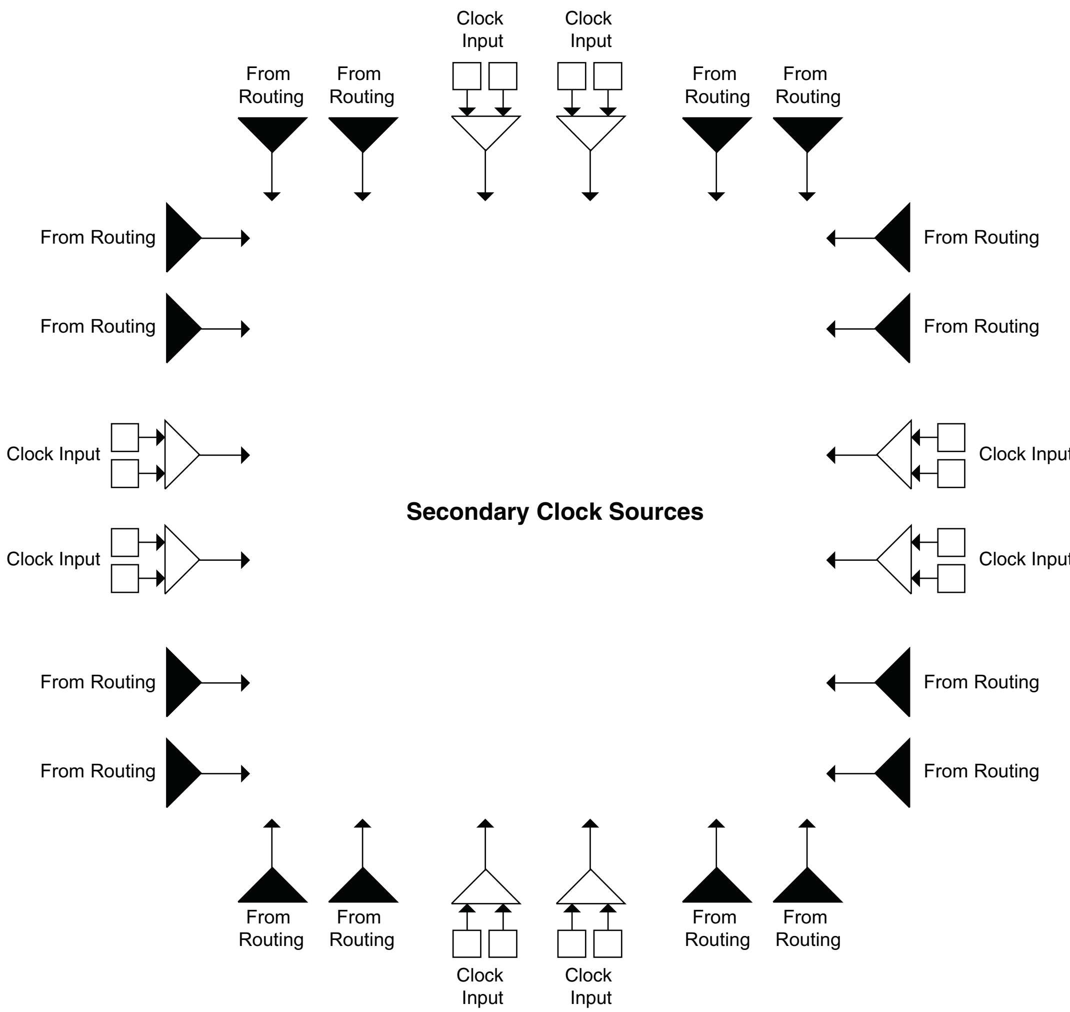
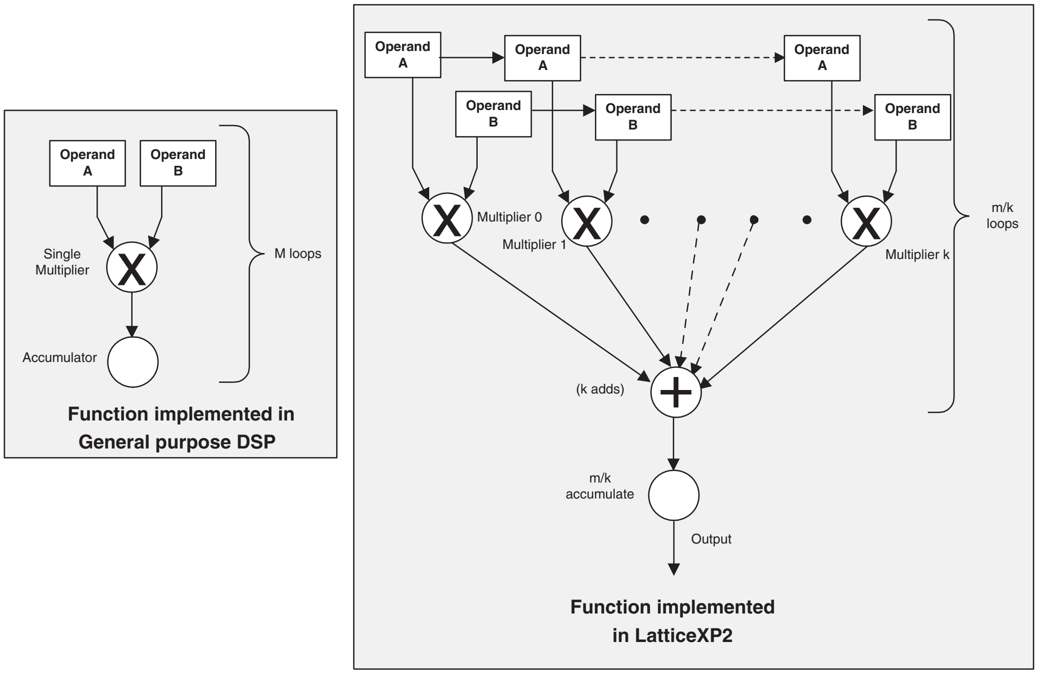


*Figure 2-19. Comparison of General DSP and LatticeXP2 Approaches*




## sysDSP Block Capabilities

The sysDSP block in the LatticeXP2 family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeXP2 family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-6 shows the capabilities of the block.

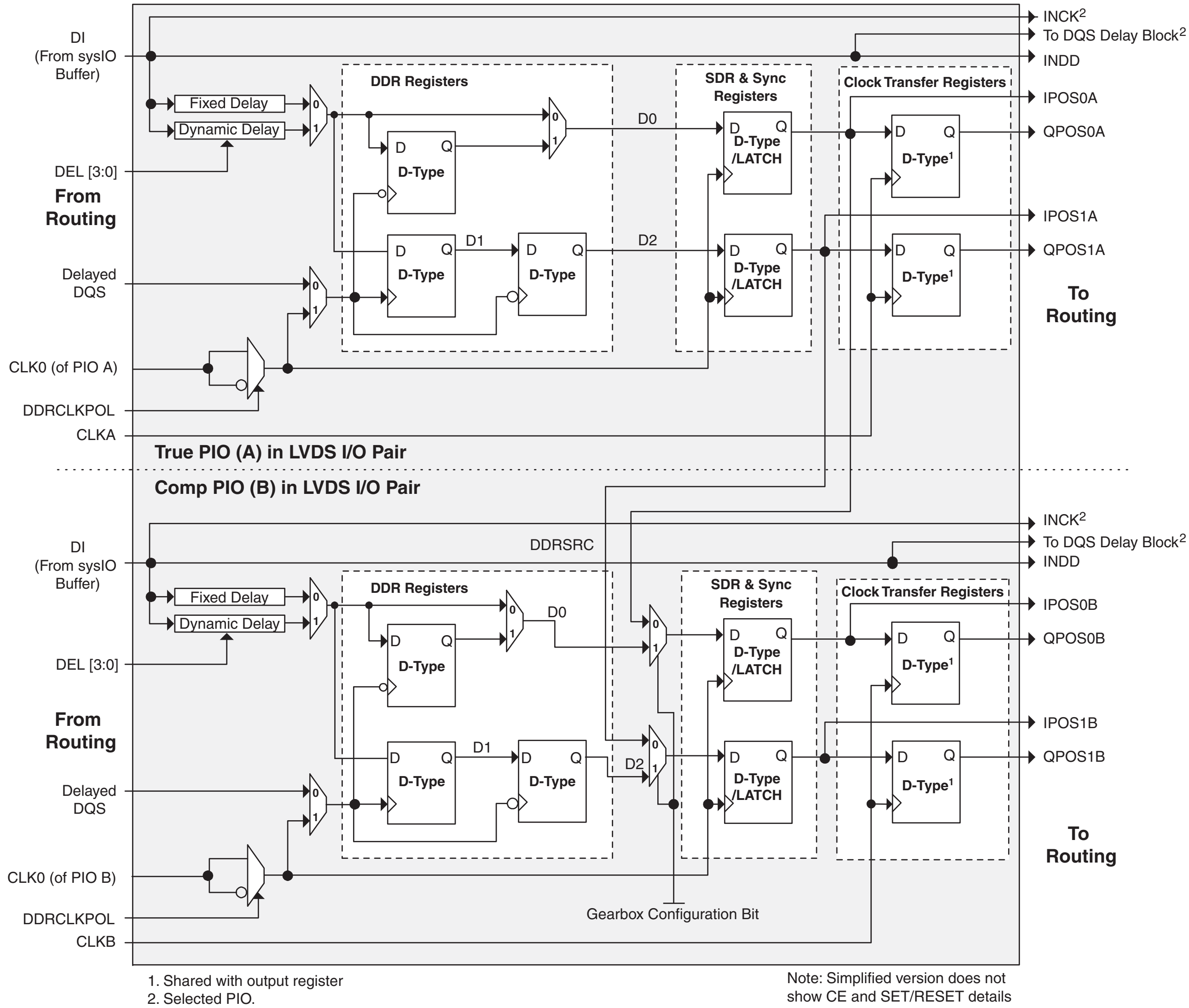
*Table 2-6. Maximum Number of Elements in a Block*

| Width of Multiply | x9 | x18 | x36 |
|---|---|---|---|
| MULT | 8 | 4 | 1 |
| MAC | 2 | 2 | — |
| MULTADDSUB | 4 | 2 | — |
| MULTADDSUBSUM | 2 | 1 | — |

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting ‘dynamic operation’ the following operations are possible:

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

***Figure 2-26. Input Register Block***



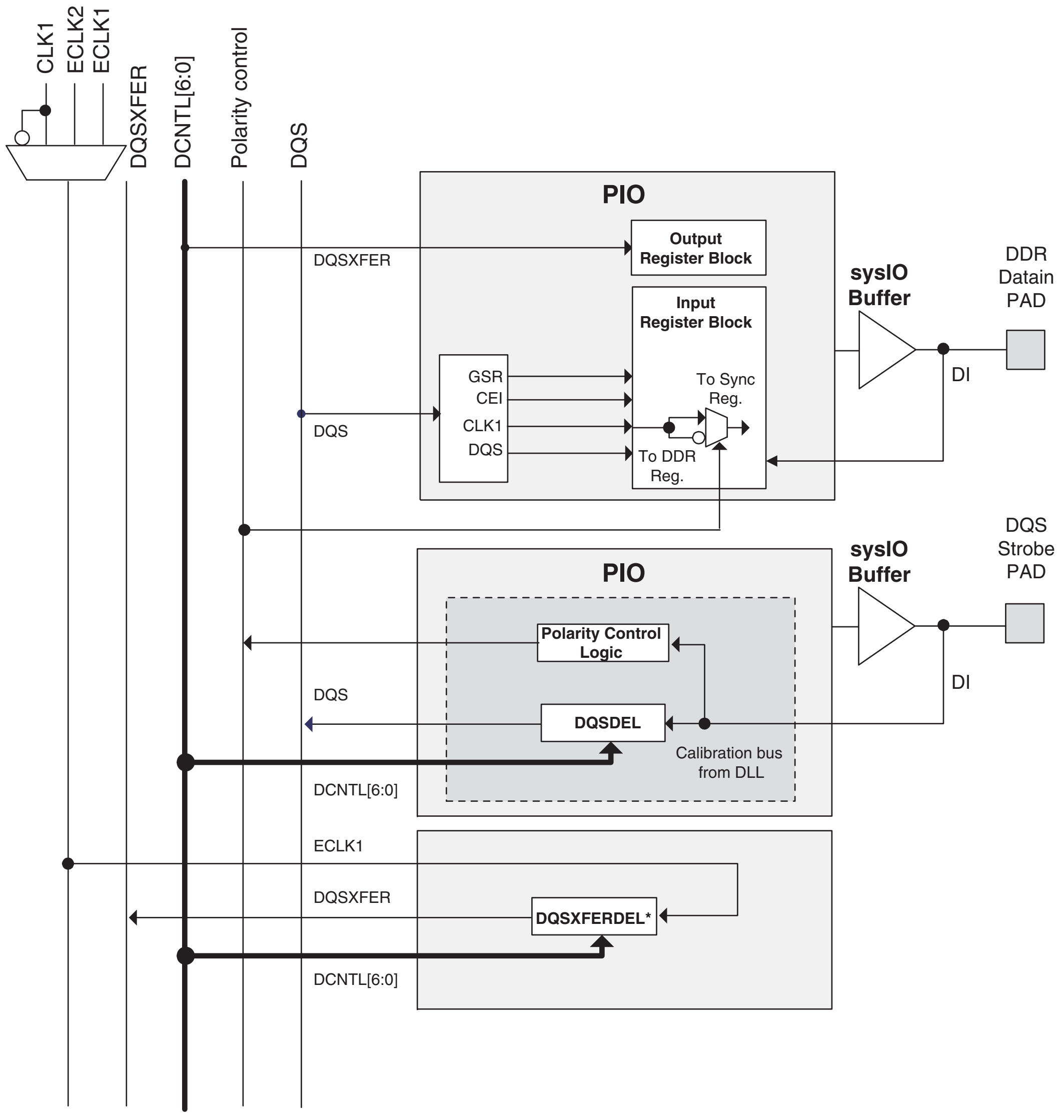

## Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. Figure 2-27 shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-27

*Figure 2-31. DQS Local Bus*




*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

## Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

*Table 2-12. Supported Input Standards*

| Input Standard | $V_{REF}$ (Nom.) | $V_{CCIO}$[1] (Nom.) |
|---|---|---|
| **Single Ended Interfaces** | | |
| LVTTL | — | — |
| LVCMOS33 | — | — |
| LVCMOS25 | — | — |
| LVCMOS18 | — | 1.8 |
| LVCMOS15 | — | 1.5 |
| LVCMOS12 | — | — |
| PCI33 | — | — |
| HSTL18 Class I, II | 0.9 | — |
| HSTL15 Class I | 0.75 | — |
| SSTL33 Class I, II | 1.5 | — |
| SSTL25 Class I, II | 1.25 | — |
| SSTL18 Class I, II | 0.9 | — |
| **Differential Interfaces** | | |
| Differential SSTL18 Class I, II | — | — |
| Differential SSTL25 Class I, II | — | — |
| Differential SSTL33 Class I, II | — | — |
| Differential HSTL15 Class I | — | — |
| Differential HSTL18 Class I, II | — | — |
| LVDS, MLVDS, LVPECL, BLVDS, RSDS | — | — |

1. When not specified, $V_{CCIO}$ can be set anywhere in the valid operating range (page 3-1).

*Table 2-13. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Nom.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA 16mA, 20mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA, 16mA, 20mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA, 16mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA 16mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA, 6mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II | N/A | 1.8 |
| HSTL15 Class I | N/A | 1.5 |
| SSTL33 Class I, II | N/A | 3.3 |
| SSTL25 Class I, II | N/A | 2.5 |
| SSTL18 Class I, II | N/A | 1.8 |
| **Differential Interfaces** | | |
| Differential SSTL33, Class I, II | N/A | 3.3 |
| Differential SSTL25, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL15, Class I | N/A | 1.5 |
| LVDS[1, 2] | N/A | 2.5 |
| MLVDS[1] | N/A | 2.5 |
| BLVDS[1] | N/A | 2.5 |
| LVPECL[1] | N/A | 3.3 |
| RSDS[1] | N/A | 2.5 |
| LVCMOS33D[1] | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |

1. Emulated with external resistors.
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

### Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

## IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in

# sysIO Differential Electrical Characteristics

## LVDS

**Over Recommended Operating Conditions**

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | | 0 | — | 2.4 | V |
| $V_{CM}$ | Input Common Mode Voltage | Half the Sum of the Two Inputs | 0.05 | — | 2.35 | V |
| $V_{THD}$ | Differential Input Threshold | Difference Between the Two Inputs | +/-100 | — | — | mV |
| $I_{IN}$ | Input Current | Power On or Power Off | — | — | +/-10 | µA |
| $V_{OH}$ | Output High Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output Low Voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output Voltage Differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ohm | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Between High and Low | | — | — | 50 | mV |
| $V_{OS}$ | Output Voltage Offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100 Ohm | 1.125 | 1.20 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between H and L | | — | — | 50 | mV |
| $I_{SA}$ | Output Short Circuit Current | $V_{OD}$ = 0V Driver Outputs Shorted to Ground | — | — | 24 | mA |
| $I_{SAB}$ | Output Short Circuit Current | $V_{OD}$ = 0V Driver Outputs Shorted to Each Other | — | — | 12 | mA |

## Differential HSTL and SSTL

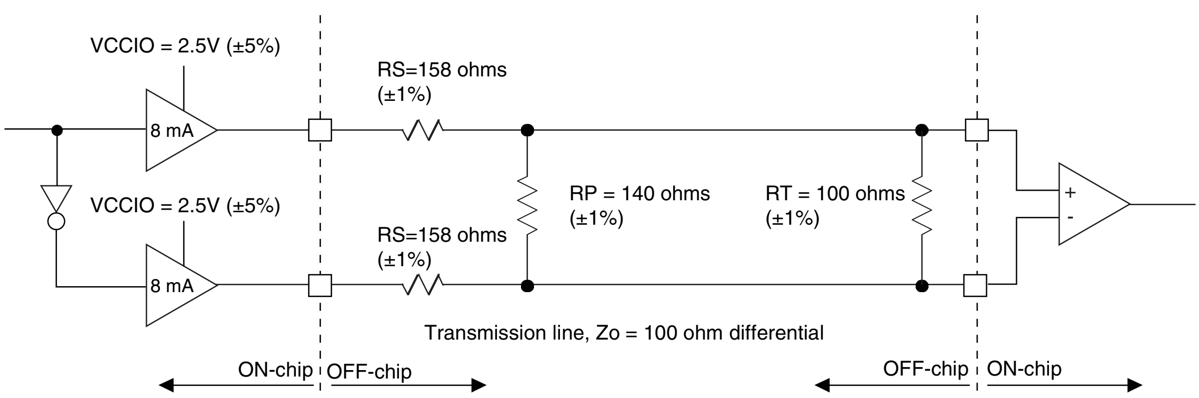
Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

## LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***



## RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

*Figure 3-4. RSDS (Reduced Swing Differential Standard)*

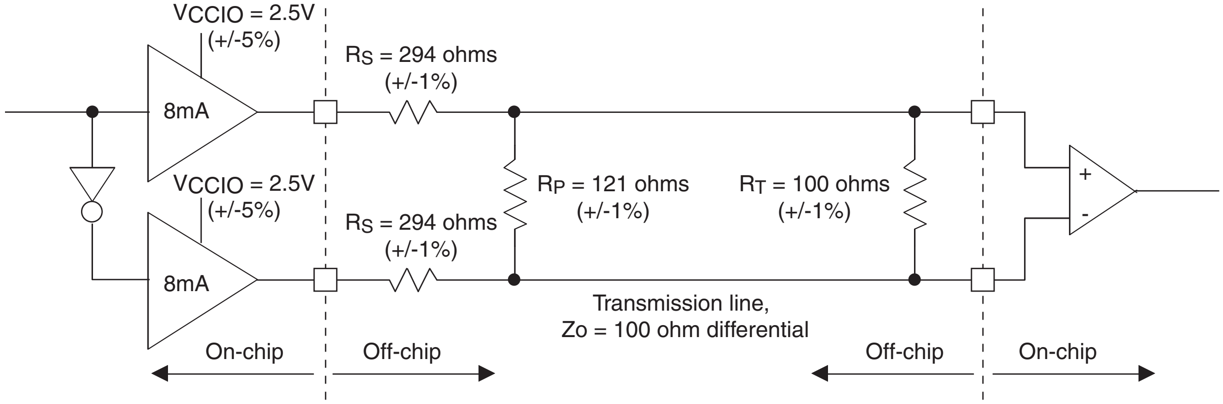


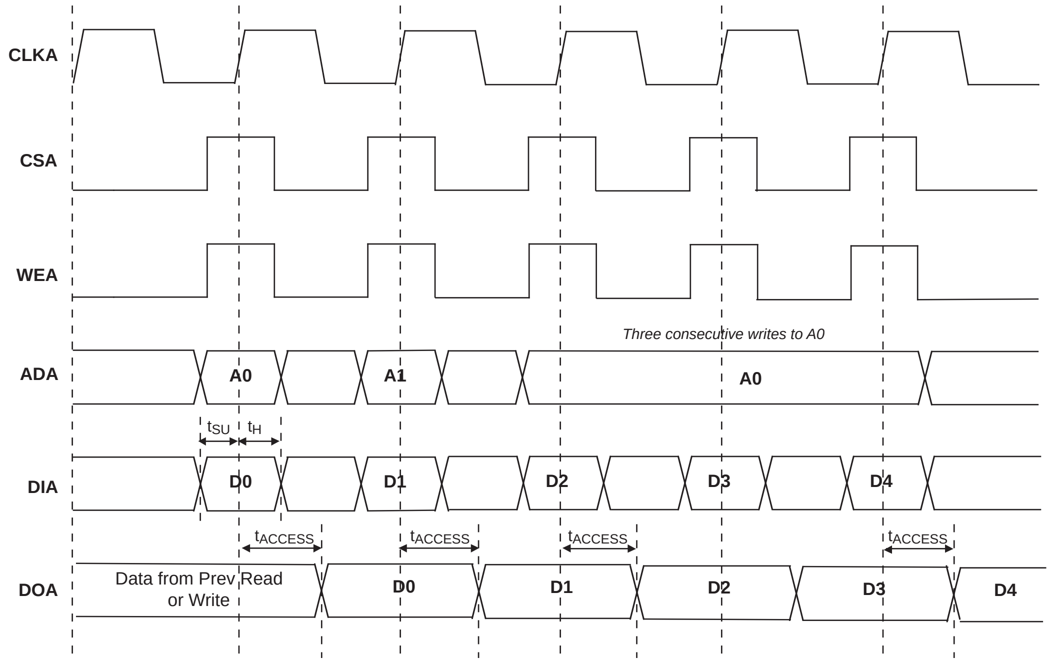

*Table 3-4. RSDS DC Conditions*[1]

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 20 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 294 | Ω |
| $R_P$ | Driver Parallel Resistor (+/-1%) | 121 | Ω |
| $R_T$ | Receiver Termination (+/-1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage (After $R_P$) | 1.35 | V |
| $V_{OL}$ | Output Low Voltage (After $R_P$) | 1.15 | V |
| $V_{OD}$ | Output Differential Voltage (After $R_P$) | 0.20 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | V |
| $Z_{BACK}$ | Back Impedance | 101.5 | Ω |
| $I_{DC}$ | DC Output Current | 3.66 | mA |

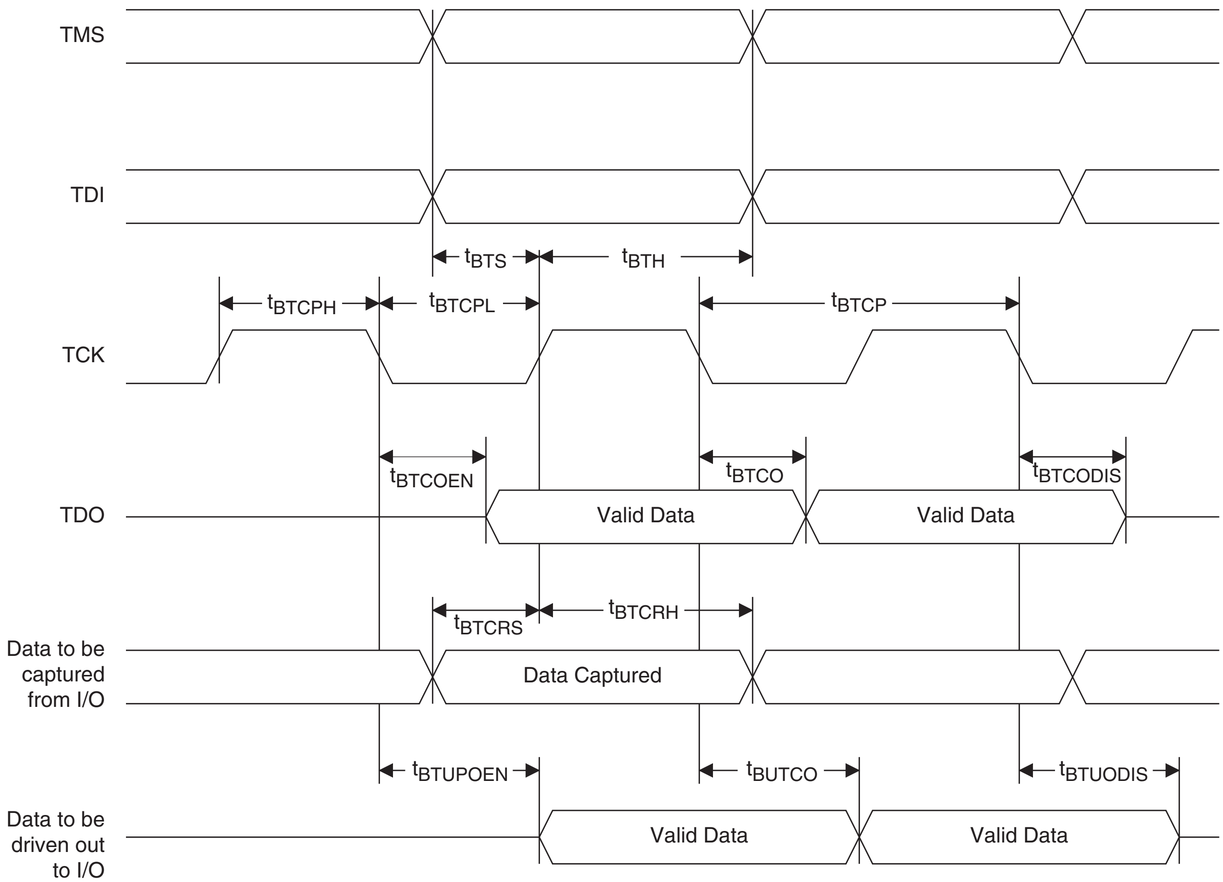
1. For input buffer, see LVDS table.

*Figure 3-8. Write Through (SP Read/Write on Port A, Input Registers Only)*




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

*Figure 3-10. JTAG Port Timing Waveforms*



## Signal Descriptions

| Signal Name | I/O | Description |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| GND | — | Ground. Dedicated pins. |
| $V_{CC}$ | — | Power supply pins for core logic. Dedicated pins. |
| $V_{CCAUX}$ | — | Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. |
| $V_{CCPLL}$ | — | PLL supply pins. csBGA, PQFP and TQFP packages only. |
| $V_{CCIOx}$ | — | Dedicated power supply pins for I/O bank x. |
| $V_{REF1\_x}$, $V_{REF2\_x}$ | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as $V_{REF}$ inputs. When not used, they may be used as I/O pins. |
| **PLL and Clock Functions** (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_$V_{CCPLL}$ | — | Power supply pin for PLL: LLC, LRC, URC, ULC, num = row from center. |
| [LOC][num]_GPLL[T, C]_IN_A | I | General Purpose PLL (GPLL) input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_GPLL[T, C]_FB_A | I | Optional feedback GPLL input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | I | Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank. |
| [LOC]DQS[num] | I | DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output. |
| **Test and Programming (Dedicated Pins)** | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |
| TDI | I | Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. |

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# LatticeXP2 Family Data Sheet Ordering Information

February 2012 | Data Sheet DS1009

## Part Number Description

LFXP2 – XX E – X XXXXX X

**Device Family**
XP2

**Logic Capacity**
5 = 5K LUTs
8 = 8K LUTs
17 = 17K LUTs
30 = 30K LUTs
40 = 40K LUTs

**Supply Voltage**
E = 1.2V

**Speed**
5 = Slowest
6
7 = Fastest

**Grade**
C = Commercial
I = Industrial

**Package**
M132 = 132-ball csBGA
FT256 = 256-ball ftBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA

MN132 = 132-ball Lead-Free csBGA
TN144 = 144-pin Lead-Free TQFP
QN208 = 208-pin Lead-Free PQFP
FTN256 = 256-ball Lead-Free ftBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA

## Ordering Information

The LatticeXP2 devices are marked with a single temperature grade, either Commercial or Industrial, as shown below.

LATTICE
LFXP2-17E
7FT256C
Datecode

LATTICE
LFXP2-17E
6FT256I
Datecode

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## Lead-Free Packaging

**Commercial**

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-5E-5MN132C | 1.2V | -5 | Lead-Free csBGA | 132 | COM | 5 |
| LFXP2-5E-6MN132C | 1.2V | -6 | Lead-Free csBGA | 132 | COM | 5 |
| LFXP2-5E-7MN132C | 1.2V | -7 | Lead-Free csBGA | 132 | COM | 5 |
| LFXP2-5E-5TN144C | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 5 |
| LFXP2-5E-6TN144C | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 5 |
| LFXP2-5E-7TN144C | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 5 |
| LFXP2-5E-5QN208C | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 5 |
| LFXP2-5E-6QN208C | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 5 |
| LFXP2-5E-7QN208C | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 5 |
| LFXP2-5E-5FTN256C | 1.2V | -5 | Lead-Free ftBGA | 256 | COM | 5 |
| LFXP2-5E-6FTN256C | 1.2V | -6 | Lead-Free ftBGA | 256 | COM | 5 |
| LFXP2-5E-7FTN256C | 1.2V | -7 | Lead-Free ftBGA | 256 | COM | 5 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-8E-5MN132C | 1.2V | -5 | Lead-Free csBGA | 132 | COM | 8 |
| LFXP2-8E-6MN132C | 1.2V | -6 | Lead-Free csBGA | 132 | COM | 8 |
| LFXP2-8E-7MN132C | 1.2V | -7 | Lead-Free csBGA | 132 | COM | 8 |
| LFXP2-8E-5TN144C | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 8 |
| LFXP2-8E-6TN144C | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 8 |
| LFXP2-8E-7TN144C | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 8 |
| LFXP2-8E-5QN208C | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 8 |
| LFXP2-8E-6QN208C | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 8 |
| LFXP2-8E-7QN208C | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 8 |
| LFXP2-8E-5FTN256C | 1.2V | -5 | Lead-Free ftBGA | 256 | COM | 8 |
| LFXP2-8E-6FTN256C | 1.2V | -6 | Lead-Free ftBGA | 256 | COM | 8 |
| LFXP2-8E-7FTN256C | 1.2V | -7 | Lead-Free ftBGA | 256 | COM | 8 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-17E-5QN208C | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 17 |
| LFXP2-17E-6QN208C | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 17 |
| LFXP2-17E-7QN208C | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 17 |
| LFXP2-17E-5FTN256C | 1.2V | -5 | Lead-Free ftBGA | 256 | COM | 17 |
| LFXP2-17E-6FTN256C | 1.2V | -6 | Lead-Free ftBGA | 256 | COM | 17 |
| LFXP2-17E-7FTN256C | 1.2V | -7 | Lead-Free ftBGA | 256 | COM | 17 |
| LFXP2-17E-5FN484C | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 17 |
| LFXP2-17E-6FN484C | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 17 |
| LFXP2-17E-7FN484C | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 17 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-17E-5QN208I | 1.2V | -5 | Lead-Free PQFP | 208 | IND | 17 |
| LFXP2-17E-6QN208I | 1.2V | -6 | Lead-Free PQFP | 208 | IND | 17 |
| LFXP2-17E-5FTN256I | 1.2V | -5 | Lead-Free ftBGA | 256 | IND | 17 |
| LFXP2-17E-6FTN256I | 1.2V | -6 | Lead-Free ftBGA | 256 | IND | 17 |
| LFXP2-17E-5FN484I | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 17 |
| LFXP2-17E-6FN484I | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 17 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-30E-5FTN256I | 1.2V | -5 | Lead-Free ftBGA | 256 | IND | 30 |
| LFXP2-30E-6FTN256I | 1.2V | -6 | Lead-Free ftBGA | 256 | IND | 30 |
| LFXP2-30E-5FN484I | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 30 |
| LFXP2-30E-6FN484I | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 30 |
| LFXP2-30E-5FN672I | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 30 |
| LFXP2-30E-6FN672I | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 30 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-40E-5FN484I | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 40 |
| LFXP2-40E-6FN484I | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 40 |
| LFXP2-40E-5FN672I | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 40 |
| LFXP2-40E-6FN672I | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 40 |

## Conventional Packaging

**Commercial**

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-5E-5M132C | 1.2V | -5 | csBGA | 132 | COM | 5 |
| LFXP2-5E-6M132C | 1.2V | -6 | csBGA | 132 | COM | 5 |
| LFXP2-5E-7M132C | 1.2V | -7 | csBGA | 132 | COM | 5 |
| LFXP2-5E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 5 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-8E-5M132C | 1.2V | -5 | csBGA | 132 | COM | 8 |
| LFXP2-8E-6M132C | 1.2V | -6 | csBGA | 132 | COM | 8 |
| LFXP2-8E-7M132C | 1.2V | -7 | csBGA | 132 | COM | 8 |
| LFXP2-8E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 8 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-17E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-5F484C | 1.2V | -5 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-6F484C | 1.2V | -6 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-7F484C | 1.2V | -7 | fpBGA | 484 | COM | 17 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-30E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-5F484C | 1.2V | -5 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-6F484C | 1.2V | -6 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-7F484C | 1.2V | -7 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-5F672C | 1.2V | -5 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-6F672C | 1.2V | -6 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-7F672C | 1.2V | -7 | fpBGA | 672 | COM | 30 |

# LatticeXP2 Family Data Sheet Supplemental Information

**February 2012** **Data Sheet DS1009**

## For Further Information

A variety of technical notes for the LatticeXP2 FPGA family are available on the Lattice Semiconductor web site at www.latticesemi.com.

- TN1136, LatticeXP2 sysIO Usage Guide
- TN1137, LatticeXP2 Memory Usage Guide
- TN1138, LatticeXP2 High Speed I/O Interface
- TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide
- TN1139, Power Estimation and Management for LatticeXP2 Devices
- TN1140, LatticeXP2 sysDSP Usage Guide
- TN1141, LatticeXP2 sysCONFIG Usage Guide
- TN1142, LatticeXP2 Configuration Encryption and Security Usage Guide
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- TN1220, LatticeXP2 Dual Boot Feature
- TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide
- TN1143, LatticeXP2 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

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| Date | Version | Section | Change Summary |
|---|---|---|---|
| April 2008 (cont.) | 01.4 (cont.) | DC and Switching Characteristics (cont.) | Updated Flash Download Time (From On-Chip Flash to SRAM) Table |
| | | | Updated Flash Program Time Table |
| | | | Updated Flash Erase Time Table |
| | | | Updated FlashBAK (from EBR to Flash) Table |
| | | | Updated Hot Socketing Specifications Table footnotes |
| | | Pinout Information | Updated Signal Descriptions Table |
| June 2008 | 01.5 | Architecture | Removed Read-Before-Write sysMEM EBR mode. |
| | | | Clarification of the operation of the secondary clock regions. |
| | | DC and Switching Characteristics | Removed Read-Before-Write sysMEM EBR mode. |
| | | Pinout Information | Updated DDR Banks Bonding Out per I/O Bank section of Pin Information Summary Table. |
| August 2008 | 01.6 | — | Data sheet status changed from preliminary to final. |
| | | Architecture | Clarification of the operation of the secondary clock regions. |
| | | DC and Switching Characteristics | Removed “8W” specification from Hot Socketing Specifications table. |
| | | | Removed "8W" footnote from DC Electrical Characteristics table. |
| | | | Updated Register-to-Register Performance table. |
| | | Ordering Information | Removed “8W” option from Part Number Description. |
| | | | Removed XP2-17 “8W” OPNs. |
| April 2011 | 01.7 | DC and Switching Characteristics | Recommended Operating Conditions table, added footnote 5. |
| | | | On-Chip Flash Memory Specifications table, added footnote 1. |
| | | | BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms. |
| | | | sysCONFIG Port Timing Specifications table, added footnote 1 for $t_{DINIT}$. |
| January 2012 | 01.8 | Multiple | Added support for Lattice Diamond design software. |
| | | Architecture | Corrected information regarding SED support. |
| | | DC and Switching Characteristics | Added reference to ESD Performance Qualification Summary information. |
| May 2013 | 01.9 | All | Updated document with new corporate logo. |
| | | Architecture | Architecture Overview – Added information on the state of the register on power up and after configuration. |
| | | | Added information regarding SED support. |
| | | DC and Switching Characteristics | Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table. |
| | | Ordering Information | Updated topside mark in Ordering Information diagram. |
| March 2014 | 02.0 | Architecture | Updated Typical sysIO I/O Behavior During Power-up section. Added information on POR signal deactivation. |
| August 2014 | 02.1 | Architecture | Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active. |
| September 2014 | 2.2 | DC and Switching Characteristics | Updated Switching Test Conditions section. Re-linked missing figure. |