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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	86
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-7m132c

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Figure 2-3. Slice Diagram



DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data

WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	MO	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-In ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



Figure 2-6. Primary Clock Sources for XP2-17



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.



Secondary Clock/Control Sources

LatticeXP2 devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-7 shows the secondary clock sources.

Figure 2-7. Secondary Clock Sources





Figure 2-12. Secondary Clock Selection



Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-13. Slice0 through Slice2 Clock Selection





Figure 2-16. FlashBAK Technology



Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

- 1. Normal Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

Figure 2-17. Memory Core Reset





For further information on the sysMEM EBR block, please see TN1137, LatticeXP2 Memory Usage Guide.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2-18. The GSR input to the EBR is always asynchronous.



Reset	
Clock	
Clock —————— Enable	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f_{MAX} (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

sysDSP™ Block

The LatticeXP2 family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications include Bit Correlators, Fast Fourier Transform (FFT) functions, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/ Decoder and Convolutional Encoder/Decoder. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeXP2 family, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-19 compares the fully serial and the mixed parallel and serial implementations.



MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

Figure 2-21. MAC sysDSP





MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUB sysDSP element.

Figure 2-22. MULTADDSUB





Table 2-11. PIO Signal List

Name	Туре	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, LatticeXP2 High Speed I/O Interface.



LatticeXP2 devices contain two types of sysIO buffer pairs.

1. Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs) The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC, V} C_{CCONFIG} (V_{CCIO7})$ and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, <u>LatticeXP2 sysIO</u> Usage Guide for additional information.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-12 and 2-13 show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1136, LatticeXP2 sysIO Usage Guide.



Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.



LatticeXP2 Family Data Sheet DC and Switching Characteristics

September 2014

Data Sheet DS1009

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V _{CC}
Supply Voltage V _{CCAUX}
Supply Voltage V _{CCJ}
Supply Voltage V _{CCPLL} ⁴ 0.5 to 3.75V
Output Supply Voltage V _{CCIO} 0.5 to 3.75V
Input or I/O Tristate Voltage Applied ⁵ 0.5 to 3.75V
Storage Temperature (Ambient)65 to 150°C
Junction Temperature Under Bias (Tj)+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice <u>Thermal Management</u> document is required.

3. All voltages referenced to GND.

4. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.

5. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Core Supply Voltage	1.14	1.26	V
V _{CCAUX} ^{4, 5}	Auxiliary Supply Voltage	3.135	3.465	V
V _{CCPLL} ¹	PLL Supply Voltage	3.135	3.465	V
V _{CCIO} ^{2, 3, 4}	I/O Driver Supply Voltage	1.14	3.465	V
V _{CCJ} ²	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t _{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t _{JIND}	Junction Temperature, Industrial Operation	-40	100	°C

1. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.

If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.

3. See recommended voltages by I/O standard in subsequent table.

4. To ensure proper I/O behavior, V_{CCIO} must be turned off at the same time or earlier than V_{CCAUX} .

5. In fpBGA and ftBGA packages, the PLLs are connected to, and powered from, the auxiliary power supply.

On-Chip Flash Memory Specifications

Symbol	Parameter	Max.	Units	
Nanagaya	Flash Programming Cycles per t _{RETENTION} ¹	10,000	Cycles	
NPROGCYC	Flash Functional Programming Cycles	100,000	Cycles	

1. The minimum data retention, t_{RETENTION}, is 20 years.

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Initialization Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
		XP2-5	20	mA
		XP2-8	21	mA
I _{CC}	Core Power Supply Current	XP2-17	44	mA
		XP2-30	58	mA
		XP2-40	62	mA
		XP2-5	67	mA
		XP2-8	74	mA
I _{CCAUX}	Auxiliary Power Supply Current ⁷	XP2-17	112	mA
		XP2-30	124	mA
		XP2-40	130	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		1.8	mA
I _{CCIO}	Bank Power Supply Current (per Bank)		6.4	mA
ICCJ	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Does not include additional current from bypass or decoupling capacitor across the supply.

5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

6. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual
auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the
auxiliary power supply.



MLVDS

The LatticeXP2 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.





Table 3-5. MLVDS DC Conditions¹

		Typical		
Parameter	Description	Ζο=50 Ω	Ζο=70 Ω	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R _{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R _{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V _{OH}	Output High Voltage (After R _{TL})	1.52	1.60	V
V _{OL}	Output Low Voltage (After R _{TL})	0.98	0.90	V
V _{OD}	Output Differential Voltage (After R _{TL})	0.54	0.70	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.



Register-to-Register Performance (Continued)

Function	-7 Timing	Units
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	198	MHz
1024-pt FFT	221	MHz
8X8 Matrix Multiplication	196	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device, design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.



sysCLOCK PLL Timing

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		10		435	MHz
fout	Output Clock Frequency (CLKOP, CLKOS)		10	—	435	MHz
f	K-Divider Output Frequency	CLKOK	0.078	_	217.5	MHz
'OUT2		CLKOK2	3.3		145	MHz
f _{VCO}	PLL VCO Frequency		435	_	870	MHz
f _{PFD}	Phase Detector Input Frequency		10	_	435	MHz
AC Characte	eristics					
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t _{CPA}	Coarse Phase Adjust		-5	0	5	%
t _{PH} ⁴	Output Phase Accuracy		-5	0	5	%
	Output Clock Period Jitter	f _{OUT} > 400 MHz	—		±50	ps
t _{OPJIT} 1		100 MHz < f _{OUT} < 400 MHz	—	_	±125	ps
		f _{OUT} < 100 MHz	—	_	0.025	UIPP
t _{SK}	Input Clock to Output Clock Skew	N/M = integer	—		±240	ps
t _{OPW}	Output Clock Pulse Width	At 90% or 10%	1	_	—	ns
+ 2	PLL Lock-in Time	25 to 435 MHz	_		50	μs
LOCK		10 to 25 MHz	—	_	100	μs
t _{IPJIT}	Input Clock Period Jitter		_		±200	ps
t _{FBKDLY}	External Feedback Delay		_		10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5		_	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5		_	ns
t _{RSTKW}	Reset Signal Pulse Width (RSTK)		10	—	—	ns
t _{RSTW}	Reset Signal Pulse Width (RST)		500		—	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.



Switching Test Conditions

Figure 3-11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-11. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

 Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	CL	Timing Ref.	V _T
				LVCMOS 3.3 = 1.5V	
				LVCMOS 2.5 = $V_{CCIO}/2$	
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 1.8 = V _{CCIO} /2	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = V _{CCIO} /2	_
LVCMOS 2.5 I/O (Z -> H)	x	1MΩ		V _{CCIO} /2	
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	x	100		V _{OH} - 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins					
For Left and Right Edges	of the Device						
D[Edgo] [n 4]	А	DQ					
r[Euge] [11-4]	В	DQ					
D[Edga] [n 2]	А	DQ					
r[Euge] [II-3]	В	DQ					
D[Edgo] [n 2]	А	DQ					
	В	DQ					
P[Edge] [n-1]	А	DQ					
	В	DQ					
P[Edge] [n]	А	[Edge]DQSn					
	В	DQ					
P[Edge] [n+1]	А	DQ					
	В	DQ					
P[Edge] [n+2]	А	DQ					
	В	DQ					
P[Edge] [n+3]	А	DQ					
	В	DQ					
For Top and Bottom Edge	es of the Device						
P[Edge] [n-4]	А	DQ					
	В	DQ					
P[Edge] [n-3]	A	DQ					
	В	DQ					
P[Edge] [n-2]	A	DQ					
. [=090] [=]	В	DQ					
P[Edge] [n-1]	A	DQ					
. [=090][]	В	DQ					
P[Edge] [n]	A	[Edge]DQSn					
. [====================================	В	DQ					
P[Edge] [n+1]	A	DQ					
. [=a90][]	В	DQ					
P[Edge] [n+2]	A	DQ					
. [=390] [5]	В	DQ					
P[Edge] [n+3]	A	DQ					
	В	DQ					
P[Edge] [n+4]	A	DQ					
. [=390][]	В	DQ					

Notes:

1. "n" is a row PIC number.

^{2.} The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.



Pin Information Summary

		XP2-5			XP2-8			XP2-17			XP2-30			XP2-40			
Pin Ty	ре	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		86	100	146	172	86	100	146	201	146	201	358	201	363	472	363	540
Differential Pair	Normal	35	39	57	66	35	39	57	77	57	77	135	77	137	180	137	204
User I/O	Highspeed	8	11	16	20	8	11	16	23	16	23	44	23	44	56	44	66
Configuration TAP Dedic	TAP	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
	Muxed	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Non Configura-	Muxed	5	5	7	7	7	7	9	9	11	11	21	7	11	13	11	13
tion	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Vcc		6	4	9	6	6	4	9	6	9	6	16	6	16	20	16	20
Vccaux		4	4	4	4	4	4	4	4	4	4	8	4	8	8	8	8
VCCPLL		2	2	2	-	2	2	2	-	4	-	-	-	-	-	-	-
	Bank0	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank1	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank2	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
VCCIO	Bank3	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
10010	Bank4	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank5	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank6	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank7	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
GND, GND0-GND7		15	15	20	20	15	15	22	20	22	20	56	20	56	64	56	64
NC		-	-	4	31	-	-	2	2	-	2	7	2	2	69	2	1
	Bank0	18/9	20/10	20/10	26/13	18/9	20/10	20/10	28/14	20/10	28/14	52/26	28/14	52/26	70/35	52/26	70/35
Single Ended/ Differential I/O per Bank	Bank1	4/2	6/3	18/9	18/9	4/2	6/3	18/9	22/11	18/9	22/11	36/18	22/11	36/18	54/27	36/18	70/35
	Bank2	16/8	18/9	18/9	22/11	16/8	18/9	18/9	26/13	18/9	26/13	46/23	26/13	46/23	56/28	46/23	64/32
	Bank3	4/2	4/2	16/8	20/10	4/2	4/2	16/8	24/12	16/8	24/12	44/22	24/12	46/23	56/28	46/23	66/33
	Bank4	8/4	8/4	18/9	18/9	8/4	8/4	18/9	26/13	18/9	26/13	36/18	26/13	38/19	54/27	38/19	70/35
	Bank5	14/7	18/9	20/10	24/12	14/7	18/9	20/10	24/12	20/10	24/12	52/26	24/12	53/26	70/35	53/26	70/35
	Bank6	6/3	8/4	18/9	22/11	6/3	8/4	18/9	27/13	18/9	27/13	46/23	27/13	46/23	56/28	46/23	66/33
	Bank7	16/8	18/9	18/9	22/11	16/8	18/9	18/9	24/12	18/9	24/12	46/23	24/12	46/23	56/28	46/23	64/32
True LVDS Pairs Bonding Out per Bank	Bank0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank2	3	4	4	5	3	4	4	6	4	6	11	6	11	14	11	16
	Bank3	1	1	4	5	1	1	4	6	4	6	11	6	11	14	11	17
	Bank4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank6	1	2	4	5	1	2	4	6	4	6	11	6	11	14	11	17
	Bank7	3	4	4	5	3	4	4	5	4	5	11	5	11	14	11	16
DDR Banks Bonding Out per I/O Bank ¹	Bank0	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank1	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank2	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4
	Bank3	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank4	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank5	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank6	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank7	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4



LatticeXP2 Family Data Sheet Ordering Information

February 2012

Data Sheet DS1009

Part Number Description



Ordering Information

The LatticeXP2 devices are marked with a single temperature grade, either Commercial or Industrial, as shown below.



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