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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1000
Number of Logic Elements/Cells	8000
Total RAM Bits	226304
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-8e-7tn144c

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Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two 4-input combinatorial Look-Up Tables (LUT4), which feed two registers. Slice 3 contains two LUT4s and no registers. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in PFF blocks. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured as positive/negative edge triggered or level sensitive clocks.

Table 2-1.	Resources	and Modes	Available	per Slice
			/ IT amaint	

	PFU E	BLock	PFF E	Block
Slice	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Slice 0 through Slice 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.



Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Fourinput logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeXP2 devices, please see TN1137, <u>LatticeXP2 Memory Usage Guide</u>.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

Number of slices	3 3	

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.



Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.



Figure 2-4. General Purpose PLL (GPLL) Diagram



Table 2-4 provides a description of the signals in the GPLL blocks.

Signal	I/O	Description	
CLKI	I	Clock input from external pin or routing	
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)	
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers	
RSTK	I	'1" to reset K-divider	
DPHASE [3:0]	I	DPA Phase Adjust input	
DDDUTY [3:0]	I	DPA Duty Cycle Select input	
WRDEL	I	DPA Fine Delay Adjust input	
CLKOS	0	PLL output clock to clock tree (phase shifted/duty cycle changed)	
CLKOP	0	PLL output clock to clock tree (no phase shift)	
CLKOK	0	PLL output to clock tree through secondary clock divider	
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)	
LOCK	0	"1" indicates PLL LOCK to CLKI	

Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.



Figure 2-12. Secondary Clock Selection



Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-13. Slice0 through Slice2 Clock Selection





For further information on the sysMEM EBR block, please see TN1137, LatticeXP2 Memory Usage Guide.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2-18. The GSR input to the EBR is always asynchronous.



Reset	
Clock	
Clock —————— Enable	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f_{MAX} (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

sysDSP™ Block

The LatticeXP2 family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications include Bit Correlators, Fast Fourier Transform (FFT) functions, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/ Decoder and Convolutional Encoder/Decoder. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeXP2 family, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-19 compares the fully serial and the mixed parallel and serial implementations.



- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.

Figure 2-20. MULT sysDSP Element





IPexpress[™]

The user can access the sysDSP block via the Lattice IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The Math-Works[®] to support instantiation in the Simulink[®] tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeXP2 Family

Table 2-8 shows the maximum number of multipliers for each member of the LatticeXP2 family. Table 2-9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
XP2-5	3	24	12	3
XP2-8	4	32	16	4
XP2-17	5	40	20	5
XP2-30	7	56	28	7
XP2-40	8	64	32	8

Table 2-8. Maximum Number of DSP Blocks in the LatticeXP2 Family

Table 2-9. Embedded SRAM/TAG Memor	v in the LatticeXP2 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)	TAG Memory (Bits)
XP2-5	9	166	632
XP2-8	12	221	768
XP2-17	15	276	2184
XP2-30	21	387	2640
XP2-40	48	885	3384

LatticeXP2 DSP Performance

Table 2-10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LatticeXP2 family.

Table 2-10. DSP Performance

Device	DSP Block	DSP Performance MMAC
XP2-5	3	3,900
XP2-8	4	5,200
XP2-17	5	6,500
XP2-30	7	9,100
XP2-40	8	10,400

For further information on the sysDSP block, please see TN1140, <u>LatticeXP2 sysDSP Usage Guide</u>.



Table 2-11. PIO Signal List

Name	Туре	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, LatticeXP2 High Speed I/O Interface.



shows the diagram using this gearbox function. For more information on this topic, see TN1138, <u>LatticeXP2 High</u> <u>Speed I/O Interface</u>.







Table 2-12. Supported Input Standards

Input Standard	V _{REF} (Nom.)	V _{CCIO} ¹ (Nom.)
Single Ended Interfaces		-
LVTTL	—	—
LVCMOS33	_	_
LVCMOS25	—	—
LVCMOS18	—	1.8
LVCMOS15	_	1.5
LVCMOS12	_	—
PCI33	—	—
HSTL18 Class I, II	0.9	_
HSTL15 Class I	0.75	—
SSTL33 Class I, II	1.5	—
SSTL25 Class I, II	1.25	_
SSTL18 Class I, II	0.9	—
Differential Interfaces		-
Differential SSTL18 Class I, II	—	—
Differential SSTL25 Class I, II	—	—
Differential SSTL33 Class I, II	—	—
Differential HSTL15 Class I	—	—
Differential HSTL18 Class I, II	—	—
LVDS, MLVDS, LVPECL, BLVDS, RSDS	—	_

1. When not specified, V_{CCIO} can be set anywhere in the valid operating range (page 3-1).



Table 2-13. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)		
Single-ended Interfaces				
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3		
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3		
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5		
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8		
LVCMOS15	4mA, 8mA	1.5		
LVCMOS12	2mA, 6mA	1.2		
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—		
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA			
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA			
LVCMOS15, Open Drain	4mA, 8mA	—		
LVCMOS12, Open Drain	2mA, 6mA	—		
PCI33	N/A	3.3		
HSTL18 Class I, II	N/A	1.8		
HSTL15 Class I	N/A	1.5		
SSTL33 Class I, II	N/A	3.3		
SSTL25 Class I, II	N/A	2.5		
SSTL18 Class I, II	N/A	1.8		
Differential Interfaces				
Differential SSTL33, Class I, II	N/A	3.3		
Differential SSTL25, Class I, II	N/A	2.5		
Differential SSTL18, Class I, II	N/A	1.8		
Differential HSTL18, Class I, II	N/A	1.8		
Differential HSTL15, Class I	N/A	1.5		
LVDS ^{1, 2}	N/A	2.5		
MLVDS ¹	N/A	2.5		
BLVDS ¹	N/A	2.5		
LVPECL ¹	N/A	3.3		
RSDS ¹	N/A	2.5		
LVCMOS33D1	4mA, 8mA, 12mA, 16mA, 20mA	3.3		

1. Emulated with external resistors.

2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in



Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.



LatticeXP2 External Switching Characteristics (Continued)

		-7		-6		-5			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		XP2-5	1.00	_	1.30	_	1.60	_	ns
		XP2-8	1.00	_	1.30	_	1.60	_	ns
t _{HE}	Clock to Data Hold - PIO Input Register	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60	_	1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	1.00		1.30	_	1.60		ns
		XP2-8	1.00		1.30	_	1.60		ns
t _{SU_DELE}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60		1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	0.00		0.00		0.00		ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
t _{H_DELE}	Clock to Data Hold - PIO Input Begister with Input Data Delay	XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00		0.00		0.00		ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
f _{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	_	420	_	357	_	311	MHz
General I/O Pir	Parameters (using Primary Clo	ck with PLL)1	1	1	1		1	
t _{COPLL}		XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8		3.00		3.30	_	3.70	ns
	Clock to Output - PIO Output Register	XP2-17		3.00		3.30	_	3.70	ns
		XP2-30	_	3.00		3.30		3.70	ns
		XP2-40		3.00		3.30	_	3.70	ns
		XP2-5	1.00		1.20		1.40		ns
		XP2-8	1.00		1.20		1.40		ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-17	1.00		1.20		1.40		ns
		XP2-30	1.00		1.20		1.40		ns
		XP2-40	1.00		1.20		1.40		ns
		XP2-5	0.90		1.10		1.30		ns
		XP2-8	0.90		1.10		1.30		ns
t _{HPLL}	Clock to Data Hold - PIO Input	XP2-17	0.90		1.10		1.30		ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
		XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90	—	2.10	—	2.30	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.90	—	2.10	—	2.30	—	ns
		XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

Over Recommended Operating Conditions



LatticeXP2 External Switching Characteristics (Continued)

			-7		-6		-5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		XP2-5	0.00	—	0.00		0.00		ns
		XP2-8	0.00	—	0.00		0.00		ns
t _{H_DELPLL}	Register with Input Data Delay	XP2-17	0.00	—	0.00		0.00		ns
		XP2-30	0.00	—	0.00	_	0.00	_	ns
		XP2-40	0.00	—	0.00	_	0.00	_	ns
DDR ² and DDF	2 ³ I/O Pin Parameters								
t _{DVADQ}	Data Valid After DQS (DDR Read)	XP2	—	0.29	—	0.29	—	0.29	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	XP2	0.71	—	0.71	_	0.71	_	UI
t _{DQVBS}	Data Valid Before DQS	XP2	0.25	—	0.25		0.25		UI
t _{DQVAS}	Data Valid After DQS	XP2	0.25	—	0.25		0.25		UI
f _{MAX_DDR}	DDR Clock Frequency	XP2	95	200	95	166	95	133	MHz
f _{MAX_DDR2}	DDR Clock Frequency	XP2	133	200	133	200	133	166	MHz
Primary Clock									
f _{MAX_PRI}	Frequency for Primary Clock Tree	XP2	—	420	—	357	—	311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	XP2	1	—	1	_	1	_	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	XP2	_	160	_	160	_	160	ps
Edge Clock (E	Edge Clock (ECLK1 and ECLK2)								
f _{MAX_ECLK}	Frequency for Edge Clock	XP2	_	420		357		311	MHz
tw_eclk	Clock Pulse Width for Edge Clock	XP2	1	_	1	_	1	_	ns
tskew_eclk	Edge Clock Skew Within an Edge of the Device	XP2	—	130	—	130	—	130	ps

Over Recommended Operating Conditions

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.

2. DDR timing numbers based on SSTL25.

3. DDR2 timing numbers based on SSTL18.







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



LatticeXP2 sysCONFIG Port Timing Specifications

Parameter	Description	Min	Max	Units				
sysCONFIG POR, Initialization and Wake Up								
t _{ICFG}	Minimum Vcc to INITN High	_	50	ms				
t _{VMC}	Time from t _{ICFG} to valid Master CCLK	_	2	μs				
t _{PRGMRJ}	PROGRAMN Pin Pulse Rejection	_	12	ns				
t _{PRGM}	PROGRAMN Low Time to Start Configuration	50	—	ns				
t _{DINIT} 1	PROGRAMN High to INITN High Delay	_	1	ms				
t _{DPPINIT}	Delay Time from PROGRAMN Low to INITN Low	_	50	ns				
t _{DPPDONE}	Delay Time from PROGRAMN Low to DONE Low	_	50	ns				
t _{IODISS}	User I/O Disable from PROGRAMN Low	_	35	ns				
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	_	25	ns				
t _{MWC}	Additional Wake Master Clock Signals after DONE Pin High	0	—	Cycles				
sysCONFIG SP	I Port (Master)							
t _{CFGX}	INITN High to CCLK Low	_	1	μs				
t _{CSSPI}	INITN High to CSSPIN Low	_	2	μs				
t _{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns				
t _{SOCDO}	CCLK Low to Output Valid	_	15	ns				
t _{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	2cyc	600+6cyc	ns				
f _{MAXSPI}	Max CCLK Frequency	—	20	MHz				
t _{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns				
t _{HSPI}	SOSPI Data Hold Time After CCLK	10	—	ns				
sysCONFIG SP	I Port (Slave)							
f _{MAXSPIS}	Slave CCLK Frequency	—	25	MHz				
t _{RF}	Rise and Fall Time	50	—	mV/ns				
t _{STCO}	Falling Edge of CCLK to SOSPI Active	—	20	ns				
t _{STOZ}	Falling Edge of CCLK to SOSPI Disable	—	20	ns				
t _{STSU}	Data Setup Time (SISPI)	8	—	ns				
t _{STH}	Data Hold Time (SISPI)	10	—	ns				
t _{sтскн}	CCLK Clock Pulse Width, High	0.02	200	μs				
t _{STCKL}	CCLK Clock Pulse Width, Low	0.02	200	μs				
t _{STVO}	Falling Edge of CCLK to Valid SOSPI Output		20	ns				
t _{SCS}	CSSPISN High Time	25	—	ns				
t _{SCSS}	CSSPISN Setup Time	25	—	ns				
t _{SCSH}	CSSPISN Hold Time	25	—	ns				

Over Recommended Operating Conditions

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of PROGRAMN.



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	17
LFXP2-17E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	17
LFXP2-17E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	17
LFXP2-17E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFXP2-17E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	17
LFXP2-17E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	30
LFXP2-30E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	30
LFXP2-30E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	30
LFXP2-30E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	30
LFXP2-30E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	30
LFXP2-30E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	40
LFXP2-40E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	40
LFXP2-40E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	40
LFXP2-40E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	40



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484I	1.2V	-5	fpBGA	484	IND	40
LFXP2-40E-6F484I	1.2V	-6	fpBGA	484	IND	40
LFXP2-40E-5F672I	1.2V	-5	fpBGA	672	IND	40
LFXP2-40E-6F672I	1.2V	-6	fpBGA	672	IND	40



Date	Version	Section	Change Summary
April 2008	01.4	DC and Switching	Updated Flash Download Time (From On-Chip Flash to SRAM) Table
(cont.)	(cont.)	Characteristics (cont.)	Updated Flash Program Time Table
			Updated Flash Erase Time Table
			Updated FlashBAK (from EBR to Flash) Table
			Updated Hot Socketing Specifications Table footnotes
		Pinout Information	Updated Signal Descriptions Table
June 2008	01.5	Architecture	Removed Read-Before-Write sysMEM EBR mode.
			Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Pinout Information	Updated DDR Banks Bonding Out per I/O Bank section of Pin Informa- tion Summary Table.
August 2008	01.6	—	Data sheet status changed from preliminary to final.
		Architecture	Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed "8W" specification from Hot Socketing Specifications table.
			Removed "8W" footnote from DC Electrical Characteristics table.
			Updated Register-to-Register Performance table.
		Ordering Information	Removed "8W" option from Part Number Description.
			Removed XP2-17 "8W" OPNs.
April 2011	01.7	DC and Switching Characteristics	Recommended Operating Conditions table, added footnote 5.
			On-Chip Flash Memory Specifications table, added footnote 1.
			BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms.
			sysCONFIG Port Timing Specifications table, added footnote 1 for t _{DINIT} .
January 2012	01.8	Multiple	Added support for Lattice Diamond design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary informa- tion.
May 2013	01.9	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			Added information regarding SED support.
		DC and Switching Characteristics	Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table.
		Ordering Information	Updated topside mark in Ordering Information diagram.
March 2014	02.0	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Added information on POR signal deactivation.
August 2014	02.1	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.
September 2014	2.2	DC and Switching Characteristics	Updated Switching Test Conditions section. Re-linked missing figure.