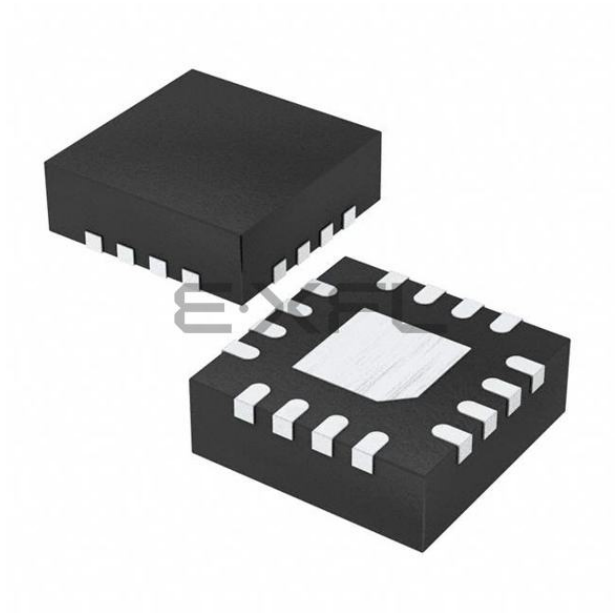

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1554-e-ml

TABLE 1-2: PIC16LF1554 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/ISCPDAT/ICDDAT	RA0	TTL	CMOS	General Purpose I/O
	AN0	AN	—	ADC Channel Input
	ICSPDAT	ST	CMOS	ICSP™ Data I/O
	ICDDAT	ST	CMOS	In-Circuit Debug Data
RA1/AN1/VREF+/ICSPCLK/ICDCLK	RA1	TTL	CMOS	General Purpose I/O
	AN1	AN	—	ADC Channel Input
	VREF+	AN	—	ADC Positive Voltage Reference Input
	ICSPCLK	ST	CMOS	ICSP Programming Clock
	ICDCLK	ST	CMOS	In-Circuit Debug Clock
RA2/AN2/TOCKI/INT/	RA2	TTL	CMOS	General Purpose I/O
	AN2	AN	—	ADC Channel Input
	TOCKI	ST	—	Timer0 Clock Input
	INT	ST	—	External Interrupt
RA3/VPP/$\overline{SS}$(1)/SDA(1)/SDI(1)/ $\overline{MCLR}$	RA3	TTL	CMOS	General Purpose Input with IOC and WPU
	VPP	HV	—	Programming Voltage
	$\overline{SS}$	ST	—	Slave Select Input
	SDA	I^2C	OD	I^2C Data Input/Output
	SDI	CMOS	—	SPI Data Input
	$\overline{MCLR}$	ST	—	Master Clear with Internal Pull-up
RA4/AN10/ADTRIG/CLKOUT/ RX(1)/DT(1)/SDO(1)/T1G	RA4	TTL	CMOS	General Purpose I/O
	AN10	AN	—	ADC Channel Input
	ADTRIG	ST	—	ADC Conversion Trigger Input
	CLKOUT	—	CMOS	FOSC/4 Output
	RX	ST	—	USART Asynchronous Input
	DT	ST	CMOS	USART Synchronous Data
	SDO	—	CMOS	SPI Data Output
	T1G	ST	—	Timer1 Gate Input
RA5/AN20/CLKIN/T1CKI	RA5	TTL	CMOS	General Purpose I/O
	AN20	AN	—	ADC Channel Input
	CLKIN	CMOS	—	External Clock Input (EC mode)
	T1CKI	ST	—	Timer1 Clock Input
RC0/AN13/SCL/SCK	RC0	TTL	CMOS	General Purpose I/O
	AN13	AN	—	ADC Channel Input
	SCL	I^2C	OD	I^2C Clock
	SCK	ST	CMOS	SPI Clock

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

TABLE 1-3: PIC16LF1559 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC6/AN14/$\overline{SS}$(1)	RC6	TTL	CMOS	General Purpose I/O
	AN14	AN	—	ADC Channel Input
	$\overline{SS}$	ST	—	Slave Select Input
RC7/AN24/SDO	RC7	TTL	CMOS	General Purpose I/O
	AN24	AN	—	ADC Channel Input
	SDO	—	CMOS	SPI Data Output

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Alternate pin function selected with the APFCON (Register 11-1) register.

TABLE 3-9: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 1											
080h	INDF0(1)	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
081h	INDF1(1)	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
082h	PCL(1)	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
083h	STATUS(1)	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
084h	FSR0L(1)	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
085h	FSR0H(1)	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
086h	FSR1L(1)	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
087h	FSR1H(1)	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
088h	BSR(1)	—	—	—	BSR<4:0>					---0 0000	---0 0000
089h	WREG(1)	Working Register								0000 0000	uuuu uuuu
08Ah	PCLATH(1)	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
08Bh	INTCON(1)	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
08Ch	TRISA	—	—	TRISA5	TRISA4	—	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
08Dh	TRISB(2)	Unimplemented								—	—
	TRISB(3)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	1111 ----
08Eh	TRISC(2)	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
	TRISC(3)	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
091h	PIE1	TMR1GIE	AD1IE	RCIE	TXIE	SSP1IE	—	TMR2IE	TMR1IE	0000 0-00	0000 0-00
092h	PIE2	—	AD2IE	—	—	BCLIE	—	—	—	-0-- 0---	-0-- 0---
095h	OPTION_REG	$\overline{WPUEN}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	—	$\overline{RWDT}$	$\overline{RMCLR}$	$\overline{RI}$	$\overline{POR}$	$\overline{BOR}$	00-1 11qq	00-q qquu
097h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	--01 0110	--01 0110
098h	—	Unimplemented								—	—
099h	OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		0011 1-00	0011 1-00
09Ah	OSCSTAT	—	PLLSR	—	HFIOFR	—	—	LFIOFR	HFIOFS	-0-0 --00	-q-q -q0q
09Bh	ADRESL/ AD1RES0L(4)	ADC1 Result Register 0 Low								xxxx xxxx	uuuu uuuu
09Ch	ADRESH/ AD1RES0H(4)	ADC1 Result Register 0 High								xxxx xxxx	uuuu uuuu
09Dh	ADCON0/ AD1CON0(4)	—	CHS4	CHS3	CHS2	CHS1	CHS0	GO/$\overline{DONE}$1	AD1ON	-000 0000	-000 0000
09Eh	ADCON1/ ADCOMCON(4)	ADFM	ADCS<2:0>			—	GO/ $\overline{DONE}$_ALL	ADPREF<1:0>		0000 -000	0000 -000
09Fh	ADCON2/ AD1CON2(4)	—	TRIGSEL<2:0>			—	—	—	—	-000 ----	-000 ----

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: These registers can be accessed from any bank.

2: PIC16LF1554.

3: PIC16LF1559.

4: These registers/bits are available at two address locations, in Bank 1 and Bank 14.

TABLE 3-9: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 31											
F80h	INDF0(1)	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
F81h	INDF1(1)	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
F82h	PCL(1)	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
F83h	STATUS(1)	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
F84h	FSR0L(1)	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
F85h	FSR0H(1)	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
F86h	FSR1L(1)	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
F87h	FSR1H(1)	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
F88h	BSR(1)	—	—	—	BSR<4:0>					---0 0000	---0 0000
F89h	WREG(1)	Working Register								0000 0000	uuuu uuuu
F8Ah	PCLATH(1)	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
F8Bh	INTCON(1)	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
F8Ch — FE2h	—	Unimplemented								—	—
FE3h	—	Unimplemented								—	—
FE4h	STATUS_-SHAD	—	—	—	—	—	Z	DC	C	---- -xxx	---- -uuu
FE5h	WREG_SHAD	Working Register Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FE6h	BSR_SHAD	—	—	—	Bank Select Register Normal (Non-ICD) Shadow					---x xxxx	---u uuuu
FE7h	PCLATH_-SHAD	—	Program Counter Latch High Register Normal (Non-ICD) Shadow							-xxx xxxx	uuuu uuuu
FE8h	FSR0L_SHAD	Indirect Data Memory Address 0 Low Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FE9h	FSR0H_SHAD	Indirect Data Memory Address 0 High Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FEAh	FSR1L_SHAD	Indirect Data Memory Address 1 Low Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FEBh	FSR1H_SHAD	Indirect Data Memory Address 1 High Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FECh	—	Unimplemented								—	—
FEDh	STKPTR	—	—	—	Current Stack pointer					---1 1111	---1 1111
FEEh	TOSL	Top of Stack Low byte								xxxx xxxx	uuuu uuuu
FEFh	TOSH	—	Top of Stack High byte							-xxx xxxx	-uuu uuuu

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: These registers can be accessed from any bank.
2: PIC16LF1554.
3: PIC16LF1559.
4: These registers/bits are available at two address locations, in Bank 1 and Bank 14.

6.12 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON registers are updated to indicate the cause of the Reset. Table 6-3 and Table 6-4 show the Reset conditions of these registers.

TABLE 6-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

STKOVF	STKUNF	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	0	1	1	1	0	x	1	1	Power-on Reset
0	0	1	1	1	0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	0	1	1	1	0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
0	0	u	1	1	u	0	1	1	Brown-out Reset
u	u	0	u	u	u	u	0	u	WDT Reset
u	u	u	u	u	u	u	0	0	WDT Wake-up from Sleep
u	u	u	u	u	u	u	1	0	Interrupt Wake-up from Sleep
u	u	u	0	u	u	u	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	u	0	u	u	u	1	0	$\overline{\text{MCLR}}$ Reset during Sleep
u	u	u	u	0	u	u	u	u	RESET Instruction Executed
1	u	u	u	u	u	u	u	u	Stack Overflow Reset (STVREN = 1)
u	1	u	u	u	u	u	u	u	Stack Underflow Reset (STVREN = 1)

TABLE 6-4: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	---1 1000	00-- 110x
$\overline{\text{MCLR}}$ Reset during normal operation	0000h	---u uuuu	uu-- 0uuu
$\overline{\text{MCLR}}$ Reset during Sleep	0000h	---1 0uuu	uu-- 0uuu
WDT Reset	0000h	---0 uuuu	uu-- uuuu
WDT Wake-up from Sleep	PC + 1	---0 0uuu	uu-- uuuu
Brown-out Reset	0000h	---1 1uuu	00-- 11u0
Interrupt Wake-up from Sleep	PC + 1(1)	---1 0uuu	uu-- uuuu
RESET Instruction Executed	0000h	---u uuuu	uu-- u0uu
Stack Overflow Reset (STVREN = 1)	0000h	---u uuuu	1u-- uuuu
Stack Underflow Reset (STVREN = 1)	0000h	---u uuuu	u1-- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and the Global Interrupt Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

REGISTER 7-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0
TMR1GIE	AD1IE	RCIE	TXIE	SSP1IE	—	TMR2IE	TMR1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enables the Timer1 gate acquisition interrupt
0 = Disables the Timer1 gate acquisition interrupt

bit 6 **AD1IE:** Analog-to-Digital Converter (ADC1) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **RCIE:** USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

bit 4 **TXIE:** USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3 **SSP1IE:** Synchronous Serial Port (MSSP) Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2 **Unimplemented:** Read as '0'

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 7-5: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	R/W-0/0	U-0	U-0	R/W-0/0	U-0	U-0	U-0
—	AD2IF	—	—	BCLIF	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6 **AD2IF:** ADC 2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **BCLIF:** MSSP Bus Collision Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2-0 **Unimplemented:** Read as '0'

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	77
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			166
PIE1	TMR1GIE	AD1IE	RCIE	TXIE	SSP1IE	—	TMR2IE	TMR1IE	78
PIE2	—	AD2IE	—	—	BCLIE	—	—	—	79
PIR1	TMR1GIF	AD1IF	RCIF	TXIF	SSP1IF	—	TMR2IF	TMR1IF	80
PIR2	—	AD2IF	—	—	BCLIF	—	—	—	81

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

REGISTER 10-3: PMADRL: PROGRAM MEMORY ADDRESS LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PMADR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PMADR<7:0>**: Specifies the Least Significant bits for program memory address

REGISTER 10-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH BYTE REGISTER

U-1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	PMADR<14:8>						
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented:** Read as ‘1’

bit 6-0 **PMADR<14:8>**: Specifies the Most Significant bits for program memory address

13.3 Register Definitions: FVR Control

REGISTER 13-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
FVREN	FVRRDY	TSEN	TSRNG	—	—	ADFVR<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **FVREN:** Fixed Voltage Reference Enable bit
1 = Fixed Voltage Reference is enabled
0 = Fixed Voltage Reference is disabled

bit 6 **FVRRDY:** Fixed Voltage Reference Ready Flag bit
1 = Fixed Voltage Reference output is ready for use
0 = Fixed Voltage Reference output is not ready or not enabled

bit 5 **TSEN:** Temperature Indicator Enable bit(1)
1 = Temperature Indicator is enabled
0 = Temperature Indicator is disabled

bit 4 **TSRNG:** Temperature Indicator Range Selection bit(1)
1 = $V_{OUT} = V_{DD} - 4V_T$ (High Range)
0 = $V_{OUT} = V_{DD} - 2V_T$ (Low Range)

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **ADFVR<1:0>:** ADC Fixed Voltage Reference Selection bit
11 = ADC Fixed Voltage Reference Peripheral output is off
10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V)
00 = ADC Fixed Voltage Reference Peripheral output is off

Note 1: See **Section 14.0 "Temperature Indicator Module"** for additional information.
2: Fixed Voltage Reference output cannot exceed V_{DD}.

TABLE 13-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	—	—	ADFVR<1:0>		124

Legend: Shaded cells are unused by the Fixed Voltage Reference module.

REGISTER 16-6: AADxCON2: HARDWARE CVD CONTROL REGISTER 2(1)

U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
—	TRIGSEL<2:0>(1)			—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **TRIGSEL<2:0>:** Auto-Conversion Trigger Selection bits
- 000 = No Auto Conversion Trigger selected
- 001 = Reserved
- 010 = Reserved
- 011 = Timer0 Overflow(2)
- 100 = Timer1 Overflow(2)
- 101 = Timer2 Match to PR2(2)
- 110 = ADTRIG Rising Edge
- 111 = ADTRIG Falling Edge

bit 3-0 **Unimplemented:** Read as '0'

Note 1: See **Section 16.1.11 "Hardware CVD Register Mapping"** for more information.

2: Signal used to set the corresponding interrupt flag.

TABLE 16-2: SUMMARY OF REGISTERS ASSOCIATED WITH HARDWARE CVD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
AADxCAP	—	—	—	—	ADDxCAP<3:0>				160
AAD1CON0	—	CHS4	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$1	AD1ON	150
AAD2CON0	—	CHS4	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$2	AD2ON	151
AADCON1/ ADCOMCON	ADFM	ADCS<2:0>			—	GO/$\overline{\text{DONE}}$_ALL	ADPREF<1:0>		154
AADxCON2	—	TRIGSEL<2:0>			—	—	—	—	155
AADxCON3	ADxEPPOL	ADxIPPOL	—	—	—	—	ADxIPEN	ADxDSEN	156
AADxGRD	GRDxBOE	GRDxAOE	GRDxPOL	—	—	—	—	—	159
AADxPRE	—	ADxPRE<6:0>							158
AADxRES0H	ADC Result 0 Register High								161
AADxRES0L	ADC Result 0 Register Low								161
AADxRES1H	ADC Result 1 Register High								162
AADxRES1L	ADC Result 1 Register Low								162
AADSTAT	—	AD2CONV	AD2STG<1:0>		—	AD1CONV	AD1STG<1:0>		157
AADxACQ	—	AADxACQ<6:0>							158
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	109
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—	113
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	117
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	—	—	ADFVR<1:0>		124
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	77
PIE1	TMR1GIE	AD1IE	RCIE	TXIE	SSP1IE	—	TMR2IE	TMR1IE	78
PIE2	—	AD2IE	—	—	BCLIE	—	—	—	79
PIR1	TMR1GIF	AD1IF	RCIF	TXIF	SSP1IF	—	TMR2IF	TMR1IF	80
PIR2	—	AD2IF	—	—	BCLIF	—	—	—	81
TRISA	—	—	TRISA5	TRISA4	—(1)	TRISA2	TRISA1	TRISA0	108
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	112
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	116

Legend: — = unimplemented read as '0'. Shaded cells are not used for hardware CVD module.

Note 1: Unimplemented, read as '1'.

FIGURE 18-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE

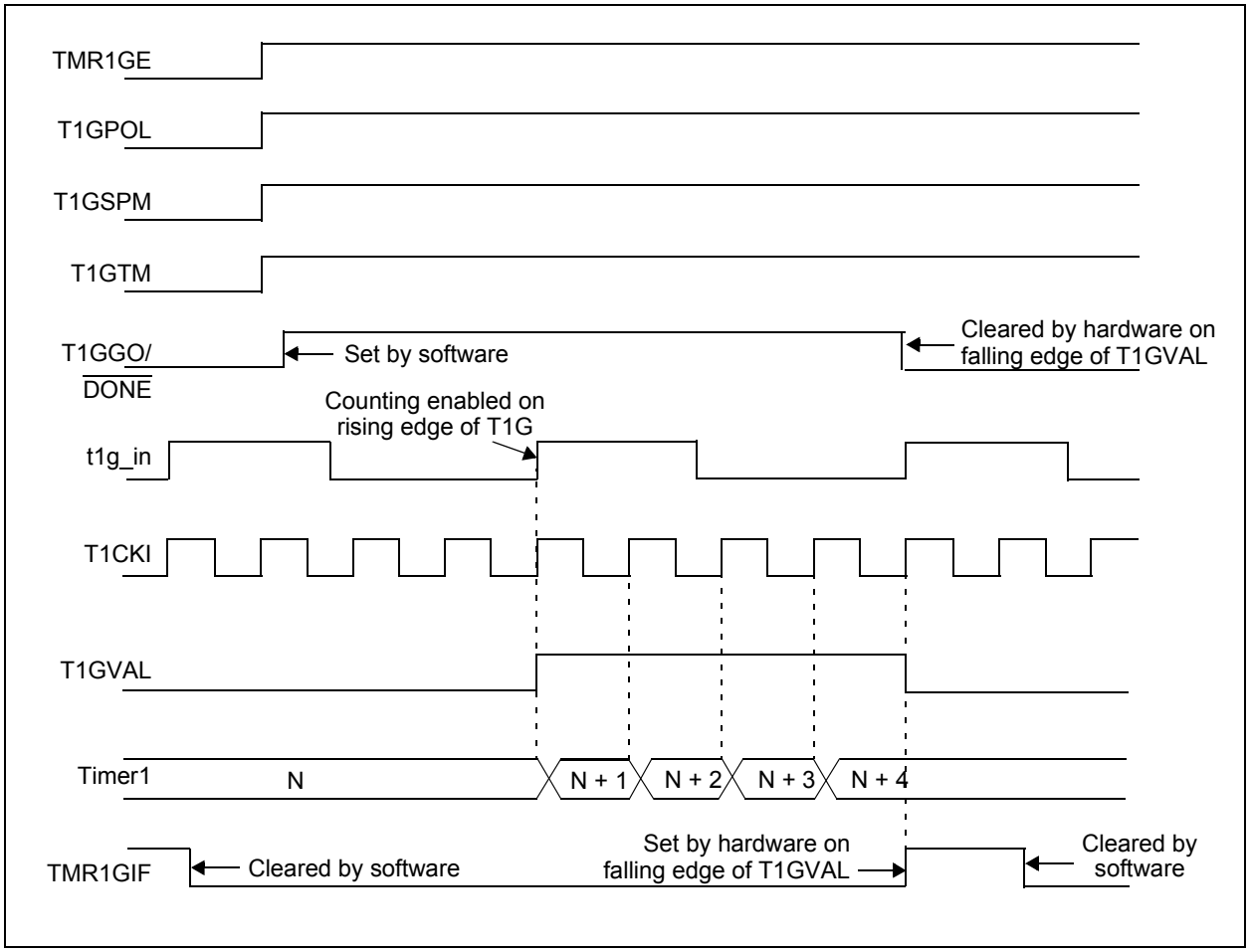


FIGURE 20-16: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 1)

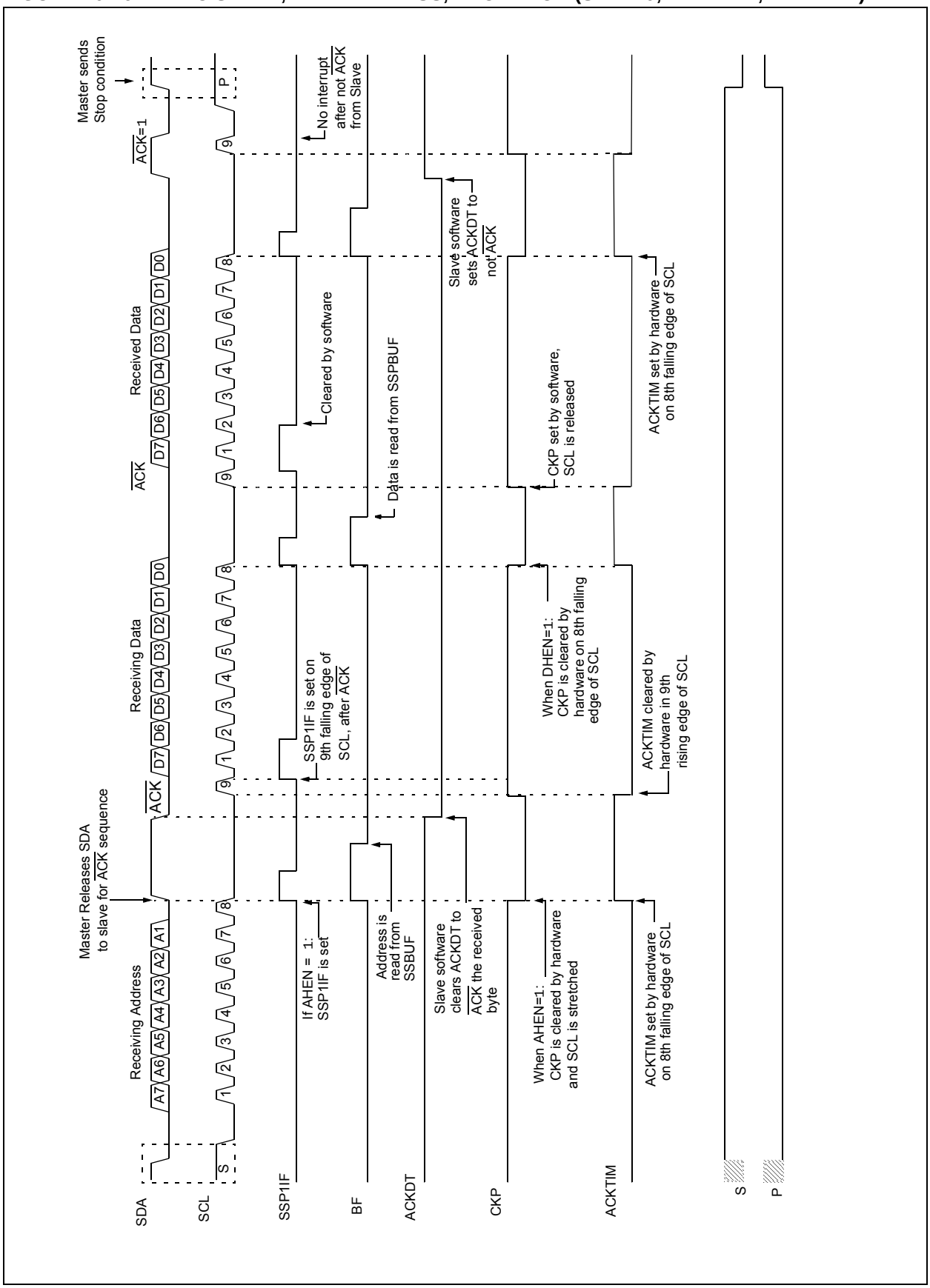
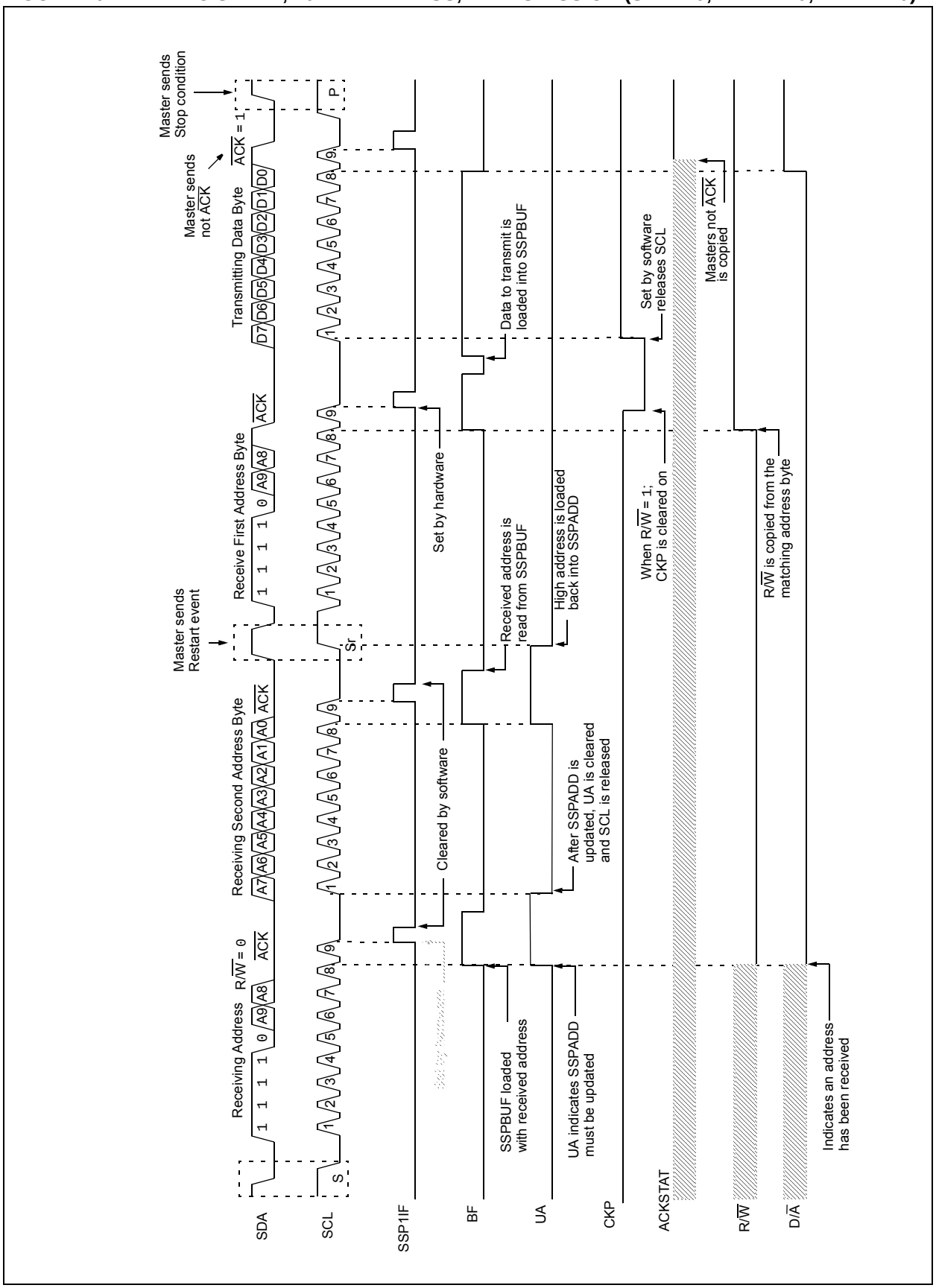


FIGURE 20-22: I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)



20.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out (Case 1).

b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high (Case 2).

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPADD and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 20-38). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 20-39).

FIGURE 20-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

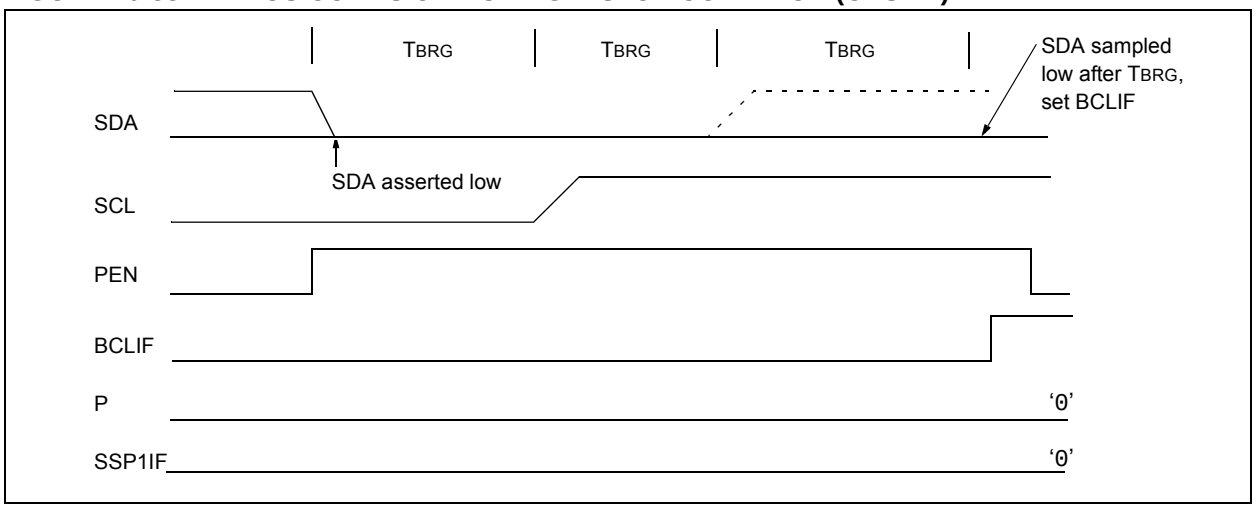
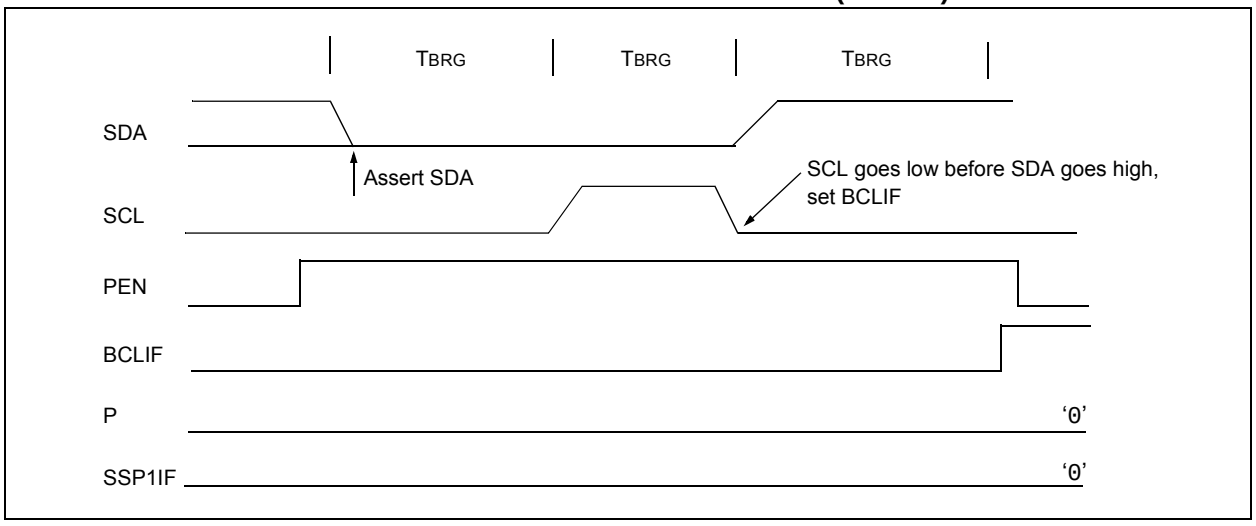


FIGURE 20-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



20.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I^2C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPADD register (Register 20-6). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

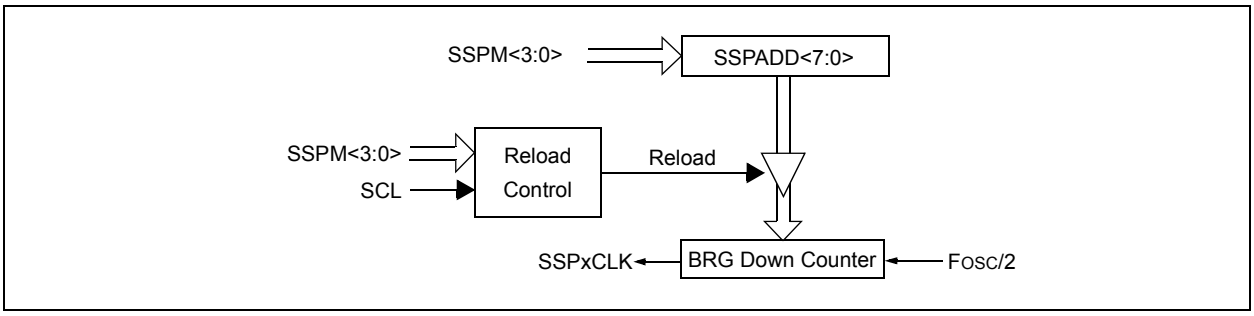
An internal signal "Reload" in Figure 20-40 triggers the value from SSPADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 20-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

EQUATION 20-1:

$$F_{CLOCK} = \frac{F_{OSC}}{(SSPxADD + 1)(4)}$$

FIGURE 20-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPADD when used as a Baud Rate Generator for I^2C. This is an implementation limitation.

TABLE 20-4: MSSP CLOCK RATE W/BRG

FOSC	FCY	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz(1)
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz(1)
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note 1: Refer to the I/O port electrical and timing specifications in Table 25-9 and Figure 25-5 to ensure the system is designed to support the I/O timing requirements.

20.7.1 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 11.1 "Alternate Pin Function"** for more information.

21.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as ADC or DAC integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 21-1 and Figure 21-2.

The EUSART transmit output (TX_out) is available to the TX/CK pin and internally to the following peripherals:

- Configurable Logic Cell (CLC)

FIGURE 21-1: EUSART TRANSMIT BLOCK DIAGRAM

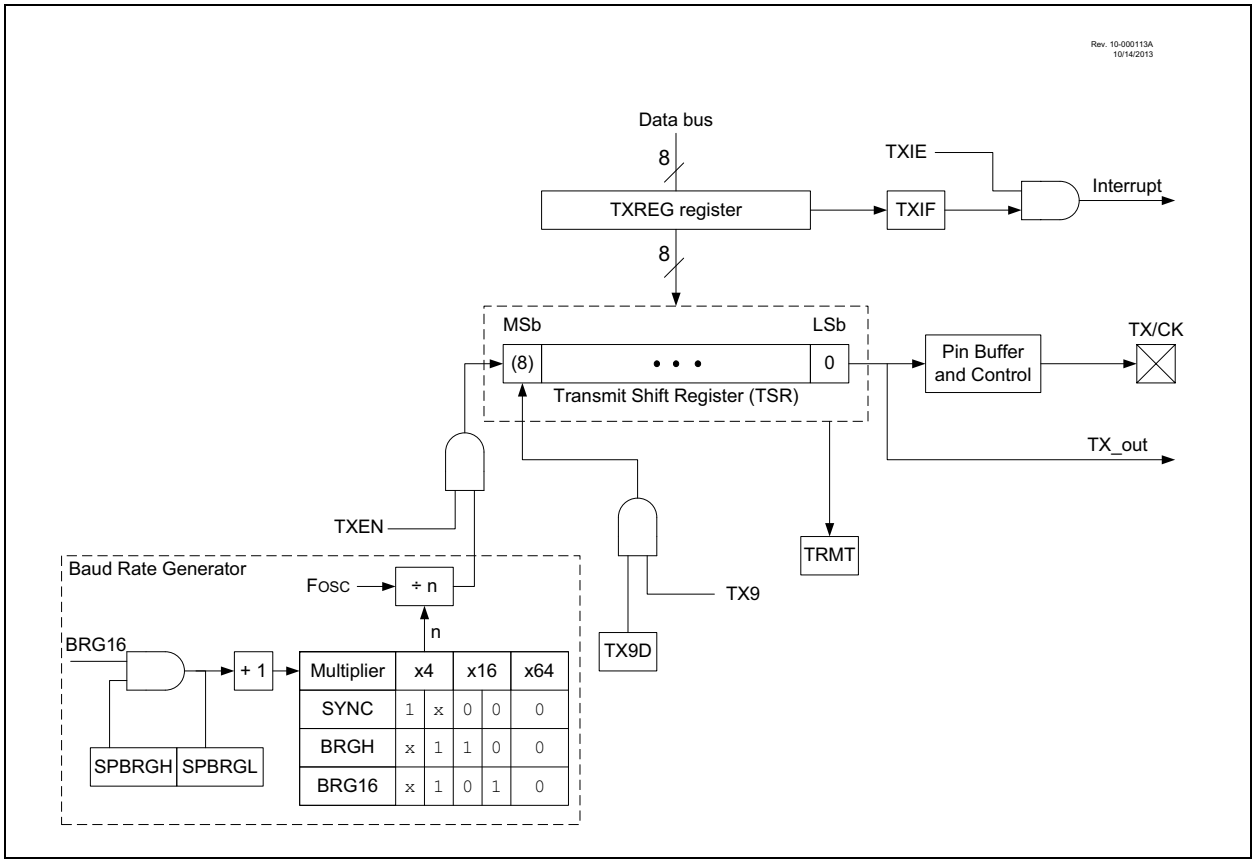


TABLE 25-18: I²C BUS DATA REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
SP100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1CB	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
SP107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
SP109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
SP111	CB	Bus capacitive loading		—	400	pF	

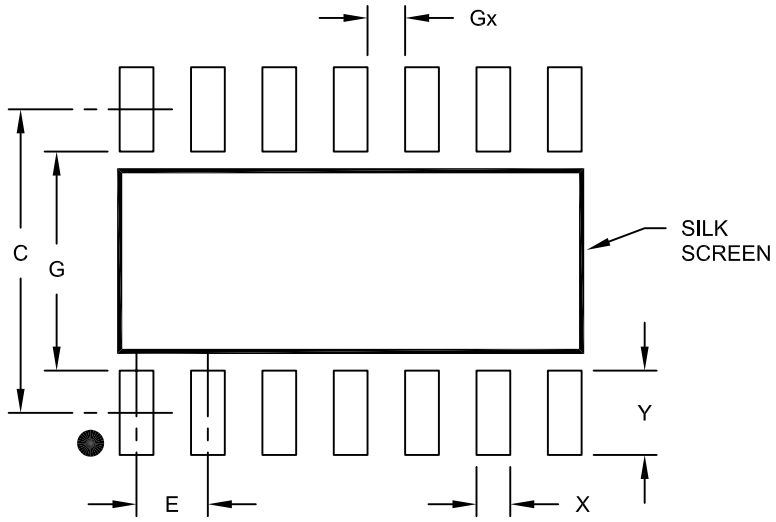
* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement TSU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

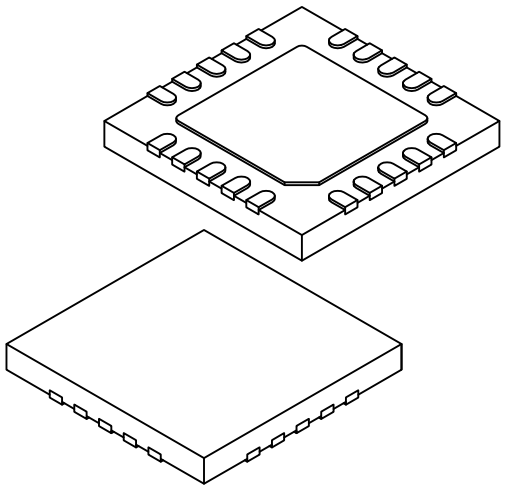
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-255A Sheet 2 of 2