Microchip Technology - TSPC603RVA8LC Datasheet

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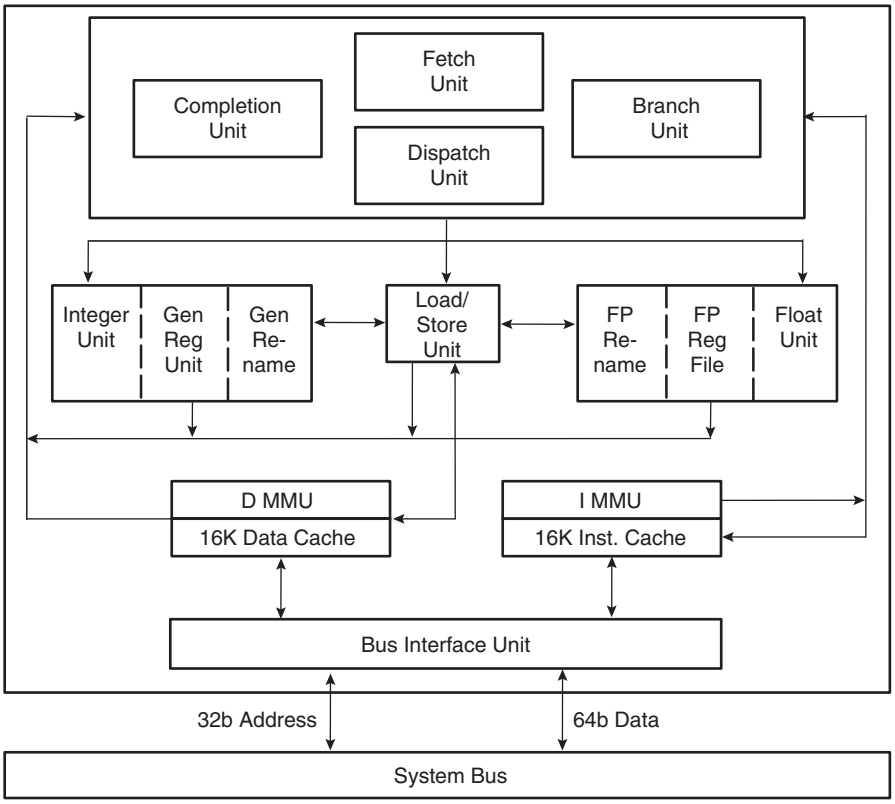
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	240-BFCQFP
Supplier Device Package	240-CERQUAD (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tspc603rva8lc

3. Block Diagram

Figure 3-1. Block Diagram



4. Overview

The 603R is a low-power implementation of the PowerPC microprocessor family of Reduced Instruction Set Computing (RISC) microprocessors. The 603R implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603R provides four software controllable power-saving modes. Three of the modes (nap, doze, and sleep) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603R to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603R is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can be executed in any order for increased performance, but, the 603R makes completion appear sequential.

The 603e integrates five execution units:

- an Integer Unit (IU)
- a Floating-point Unit (FPU)
- a Branch Processing Unit (BPU)

8. Thermal Characteristics

8.1 CBGA 255 and CI-CGA 255 Packages

The data found in this section concerns 603R devices packaged in the 255-lead 21 mm multi-layer ceramic (MLC) and ceramic BGA package. Data is included for use with a Thermalloy #2328B heat sink.

The internal thermal resistance for this package is negligible due to the exposed die design. A thermal interface material is recommended at the package lid to heat sink interface to minimize the thermal contact resistance.

Additionally, the CBGA package offers an excellent thermal connection to the card and power planes. Heat generated at the chip is dissipated through the package, the heat sink (when used) and the card. The parallel heat flow paths result in the lowest overall thermal resistance as well as offer significantly better power dissipation capability if a heat sink is not used.

The thermal characteristics for the flip-chip CBGA and CI-CGA packages are as follows:

Thermal resistance (junction-to-case) = R_{jc} or
θ_{jc} = 0.095°C/Watt for the 2 packages.

Thermal resistance (junction-to-ball) = R_{jb} or
θ_{jb} = 3.5°C/Watt for the CBGA package.

Thermal resistance (junction-to-bottom SCI) = R_{js} or
θ_{js} = 3.7°C/Watt for the CI-CGA package.

The junction temperature can be calculated from the junction to ambient thermal resistance, as follow:

Junction temperature:

$$T_j = T_a + (R_{jc} + R_{cs} + R_{sa}) \times P$$

where: T_a is the ambient temperature in the vicinity of the device

R_{jc} is the die junction to case thermal resistance of the device

R_{cs} is the case to heat sink thermal resistance of the interface material

R_{sa} is the heat sink to ambient thermal resistance

P is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained at a lower value than the value specified in ”Recommended Operating Conditions” on page 6.

The thermal resistance of the thermal interface material (R_{cs}) is typically about 1°C/Watt.

Assuming a T_a of 85°C and a consumption (P) of 3.6 Watts, the junction temperature of the device would be as follow:

T_j = 85°C + (0.095°C/Watt + 1°C/Watt + R_{sa}) × 3.5 Watts.

For the Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (R_{sa}) versus airflow velocity is shown in Figure 8-1.

9.2 Programmable Power Modes

The 603R provides four programmable power states, full power, doze, nap and sleep. The software selects these modes by setting one (and only one) of the three power saving mode bits. The hardware can enable a power management state through external asynchronous interrupts. The hardware interrupt causes the transfer of program flow to interrupt the handler code. The appropriate mode is then set by the software. The 603R provides a separate interrupt and interrupt vector for power management, the System Management Interrupt (SMI). The 603R also contains a decrement timer which allows it to enter the nap or doze mode for a predetermined amount of time and then return to full power operation through the Decrementer Interrupt (DI). Note that the 603R cannot switch from power-on management mode to another without first returning to full on mode. The nap and sleep modes disable bus snooping; therefore, a hardware handshake is provided to ensure coherency before the 603R enters these power management modes.

Table 9-1 summarizes the four power states.

Table 9-1. Power PC 603R Microprocessor Programmable Power Modes

PM Mode	Functioning Units	Activation Method	Full-power Wake-up Method
Full Power	All units active	–	–
Full Power (with DPM)	Requested logic by demand	By instruction dispatch	–
Doze	- Bus snooping - Data cache as needed - Decrementer timer	Controlled by SW	External asynchronous exceptions(1) Decrementer interrupt Reset
Nap	Decrementer timer	Controlled by hardware and software	External asynchronous exceptions Decrementer interrupt Reset
Sleep	None	Controlled by hardware and software	External asynchronous exceptions Reset

Note: 1. Exceptions are referred to as interrupts in the architecture specification.

9.3 Power Management Modes

The following describes the characteristics of the 603R's power management modes, the requirements for entering and exiting the various modes, and the system capabilities provided by the 603R while the power management modes are active.

Full Power Mode with DPM Disabled

Full power mode with DPM disabled; power mode is selected when the DPM enable bit (bit 11) in HID0 is cleared

- Default state following power-up and $\overline{\text{HRESET}}$
- All functional units are operating at full processor speed at all times

Full Power Mode with DPM Enabled

Full power mode with DPM enabled (HID0[11] = 1); provides on-chip power management without affecting the functionality or performance of the 603R

- Required functional units are operating at full processor speed

Sleep Mode

Sleep mode consumes the least amount of power of the four modes since all functional units are disabled. To conserve the maximum amount of power, the PLL may be disabled and the SYSCLK may be removed. Due to the fully static design of the 603R, the internal processor state is preserved when no internal clock is present. Because the time base and decrementer are disabled while the 603R is in sleep mode, the 603R's time base contents will have to be updated from an external time base following sleep mode if accurate time-of-day maintenance is required. Before the 603R enters the sleep mode, the 603R will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603R will enter the sleep mode.

In this mode:

- All functional units are disabled (including bus snooping and time base)
- All non-essential input receivers are disabled
  - Internal clock regenerators are disabled
  - The PLL is still running (see below)
- Sleep mode sequence
  - Set sleep bit (HID0[10] = 1)
  - 603R asserts quiesce request ($\overline{\text{QREQ}}$)
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$)
  - 603R enters sleep mode after several processor clocks
- There are several methods for returning to full-power mode
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, or $\overline{\text{MCP}}$ interrupts
  - Assert hard reset or soft reset
- The PLL may be disabled and SYSCLK may be removed while in sleep mode
- Return to full-power mode after PLL and SYSCLK disabled in sleep mode
  - Enable SYSCLK
  - Reconfigure PLL into the desired processor clock mode
  - System logic waits for PLL startup and relock time (100 µs)
  - System logic asserts one of the sleep recovery signals (for example, INT or SMI)

9.4 Power Management Software Considerations

Since the 603R is a dual issue processor with out-of-order execution capabilities, care must be taken with the way the power management mode is entered. Furthermore, nap and sleep modes require all outstanding bus operations to be completed before the power management mode is entered. Normally, during the system configuration time, one of the power management modes would be selected by setting the appropriate HID0 mode bit. Later on, the power management mode is invoked by setting the MSR[POW] bit. To provide a clean transition into and out of the power management mode, the **stmsr**[POW] should be preceded by a **sync** instruction and followed by an **isync** instruction.

10.2.1 Pinout Listing

Table 10-3. Power and Ground Pins

	CERQUAD Pin Number	
	VCC	**GND**
PLL (AV_{DD})	209	
Internal Logic	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239
Output Drivers	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238

Table 10-4. Signal Pinout Listing

Signal Name	CERQUAD Pin Number
A[0-31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37
$\overline{\text{AACK}}$	28
$\overline{\text{ABB}}$	36
AP[0-3]	231,230,227,226
$\overline{\text{APE}}$	218
$\overline{\text{ARTRY}}$	32
$\overline{\text{BG}}$	27
$\overline{\text{BR}}$	219
$\overline{\text{CI}}$	237
$\overline{\text{CKSTP\_IN}}$	215
$\overline{\text{CKSTP\_OUT}}$	216
CLK_OUT	221
CSE[0-1]	225,150
$\overline{\text{DBB}}$	145
$\overline{\text{DBG}}$	26
$\overline{\text{DBDIS}}$	153
$\overline{\text{DBWO}}$	25
DH[0-31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66
DL[0-31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64
DP[0-7]	38, 40, 41, 42, 46, 47, 48, 50
$\overline{\text{DPE}}$	217
$\overline{\text{DRTRY}}$	156
$\overline{\text{GBL}}$	1
$\overline{\text{HRESET}}$	214

Table 10-4. Signal Pinout Listing (Continued)

Signal Name	CERQUAD Pin Number
$\overline{\text{INT}}$	188
L1_TSTCLK[1]	204
L2_TSTCLK[1]	203
$\overline{\text{LSSD\_MODE}}$[1]	205
$\overline{\text{MCP}}$	186
PLL_CFG[0-3]	213, 211, 210, 208
$\overline{\text{QACK}}$	235
$\overline{\text{QREQ}}$	31
$\overline{\text{RSRV}}$	232
$\overline{\text{SMI}}$	187
$\overline{\text{SRESET}}$	189
SYSCLK	212
$\overline{\text{TA}}$	155
TBEN	234
$\overline{\text{TBST}}$	192
TC[0-1]	224, 223
TCK	201
TDI	199
TDO	198
$\overline{\text{TEA}}$	154
$\overline{\text{TLBISYNC}}$	233
TMS	200
$\overline{\text{TRST}}$	202
$\overline{\text{TS}}$	149
TSIZ[0-2]	197, 196, 195
TT[0-4]	191, 190, 185, 184, 180
$\overline{\text{WT}}$	236
NC	

Notes: 1. These are test signals for factory use only and must be pulled up to V_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core. Future members of the 603 family may use different OV_{DD} and V_{DD} input levels.

Table 10-5. Address and Data Bus Signal Index for Cerquad, CBGA 255 and CI-CGA 255 Packages

Signal Name	Abbreviation	Signal Function	Signal Type
Address Bus	A[0-31]	If output, physical address of data to be transferred If input, represents the physical address of a snoop operation	I/O
Data Bus	DH[0-31]	Represents the state of data, during a data write operation if output, or during a data read operation if input	I/O
Data Bus	DL[0-31]	Represents the state of data, during a data write operation if output, or during a data read operation if input	I/O

Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages

Signal Name	Abbreviation	Signal Function	Signal Type
Address Acknowledge	$\overline{\text{AACK}}$	The address phase of a transaction is complete	Input
Address Bus Busy	$\overline{\text{ABB}}$	If output, the 603R is the address bus master If input, the address bus is in use	I/O
Address Bus Parity	AP[0-3]	If output, represents odd parity for each of 4 bytes of the physical address for a transaction If input, represents odd parity for each of 4 bytes of the physical address for snooping operations	I/O
Address Parity Error	$\overline{\text{APE}}$	Incorrect address bus parity detected on a snoop	Output
Address Retry	$\overline{\text{ARTRY}}$	If output, detects a condition in which a snooped address tenure must be retried If input, must retry the preceding address tenure	I/O
Bus Grant	$\overline{\text{BG}}$	May, with the proper qualification, assume mastership of the address bus	Input
Bus Request	$\overline{\text{BR}}$	Request mastership of the address bus	Output
Cache Inhibit	$\overline{\text{CI}}$	A single-beat transfer will not be cached	Output
Checkstop Input	$\overline{\text{CKSTP\_IN}}$	Must terminate operation by internally gating off all clocks, and release all outputs	Input
Checkstop Output	$\overline{\text{CKSTP\_OUT}}$	Has detected a checkstop condition and has ceased operation	Output
Cache Set Entry	CSE[0-1]	Cache replacement set element for the current transaction reloading into or writing out of the cache	Output
Data Bus Busy	$\overline{\text{DBB}}$	If output, the 603R is the data bus master If input, another device is bus master	I/O
Data Bus Disable	$\overline{\text{DBDIS}}$	(For a write transaction) must release data bus and the data bus parity to high impedance during the following cycle	Input
Data Bus Grant	$\overline{\text{DBG}}$	May, with the proper qualification, assume mastership of the data bus	Input
Data Bus Write Only	$\overline{\text{DBW0}}$	May run the data bus tenure	Input
Data Bus Parity	DP[0-7]	If output, odd parity for each of 8 bytes of data write transactions If input, odd parity for each byte of read data	I/O
Data Parity Error	$\overline{\text{DPE}}$	Incorrect data bus parity	Output
Data Retry	$\overline{\text{DRTRY}}$	Must invalidate the data from the previous read operation	Input

Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

Signal Name	Abbreviation	Signal Function	Signal Type
Global	$\overline{\text{GBL}}$	If output, a transaction is global If input, a transaction must be snooped by the 603R	I/O
Hard Reset	$\overline{\text{HRESET}}$	Initiates a complete hard reset operation	Input
Interrupt	$\overline{\text{INT}}$	Initiates an interrupt if bit EE of MSR register is set	Input
Factory Test	$\overline{\text{LSSD\_MODE}}$	LSSD test control signal for factory use only	Input
	L1_TSTCLK	LSSD test control signal for factory use only	Input
	L2_TSTCLK	LSSD test control signal for factory use only	Input
Machine Check Interrupt	$\overline{\text{MCP}}$	Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set	Input
PLL Configuration	PLL_CFG[0-3]	Configures the operation of the PLL and the internal processor clock frequency	Input
Power supply indicator	VOLTDETGND	Available only on BGA package Indicates to the power supply that a low-voltage processor is present.	Output
Quiescent Acknowledge	$\overline{\text{QACK}}$	All bus activity has terminated and the 603R may enter a quiescent (or low power) state	Input
Quiescent Request	$\overline{\text{QREQ}}$	Is requesting all bus activity normally to enter a quiescent (low power) state	Output
Reservation	$\overline{\text{RSRV}}$	Represents the state of the reservation coherency bit in the reservation address register	Output
System Management Interrupt	$\overline{\text{SMI}}$	Initiates a system management interrupt operation if the bit EE of MSR register is set	Input
Soft Reset	$\overline{\text{SRESET}}$	Initiates processing for a reset exception	Input
System Clock	SYSCLK	Represents the primary clock input for the 603R, and the bus clock frequency for 603R bus operation	Input
Test Clock	CLK_OUT	Provides PLL clock output for PLL testing and monitoring	Output
Transfer Acknowledge	$\overline{\text{TA}}$	A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully	Input
Timebase Enable	TBEN	The timebase should continue clocking	Input
Transfer Burst	$\overline{\text{TBST}}$	If output, a burst transfer is in progress If input, when snooping for single-beat reads	I/O
Transfer Code	TC[0-1]	Special encoding for the transfer in progress	Output
Test Clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)	Input
Test Data Input	TDI	Serial data input for the TAP	Input
Test Data Output	TDO	Serial data output for the TAP	Output
Transfer Error Acknowledge	$\overline{\text{TEA}}$	A bus error occurred	Input
TLBI Sync	$\overline{\text{TLBISYNC}}$	Instruction execution should stop after execution of a **tlbsync** instruction	Input
Test Mode Select	TMS	Selects the principal operations of the test-support circuitry	Input
Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset of the TAP controller	Input
Transfer Size	TSIZ[0-2]	For memory accesses, these signals along with $\overline{\text{TBST}}$ indicate the data transfer size for the current bus operation	I/O

Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

Signal Name	Abbreviation	Signal Function	Signal Type
Transfer Start	$\overline{TS}$	If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$)	I/O
Transfer Type	TT[0-4]	Type of transfer in progress	I/O
Write-through	$\overline{WT}$	A single-beat transaction is write-through	Output

11. Electrical Characteristics

11.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 11-1: Static electrical characteristics for the electrical variants
- Table 11-2: Dynamic electrical characteristics for the 603R

The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0 to PLL_CFG3 signals. All timings are respectively specified to the rising edge of SYSCLK.

These specifications are for 166 MHz to 300 MHz processor core frequencies for CBGA 255, HiTCE CBGA 255 and CI-CGA 255 packages and 166 MHz to 200 MHz processor core frequencies for the Cerquad 240 package.

11.2 Static Characteristics

Table 11-1. Electrical Characteristics with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Characteristics		Symbol	Min	Max	Unit
Input High Voltage (all inputs except SYSCLK)		V_{IH}	2	5.5	V
Input Low Voltage (all inputs except SYSCLK)		V_{IL}	GND	0.8	V
SYSCLK Input High Voltage		CV_{IH}	2.4	5.5	V
SYSCLK Input Low Voltage		CV_{IL}	GND	0.4	V
Input Leakage Current	V_{IN} = 3.465V(1)(3)	I_{IN}	-	30	µA
	V_{IN} = 5.5V(1)(3)	I_{IN}	-	300	µA
Hi-Z (off-state) Leakage Current	V_{IN} = 3.465V(1)(3)	I_{TSI}	-	30	µA
	V_{IN} = 5.5V(1)(3)	I_{TSI}	-	300	µA
Output High Voltage	I_{OH} = -7 mA	V_{OH}	2.4	-	V
Output Low Voltage	I_{OL} = +7 mA	V_{OL}	-	0.4	V
Capacitance, V_{IN} = 0V, f = 1 MHz(2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{IN}	-	10	pF
Capacitance, V_{IN} = 0V, f = 1 MHz(2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{IN}	-	15	pF

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100% tested.

Figure 11-7. Boundary-scan Timing Diagram

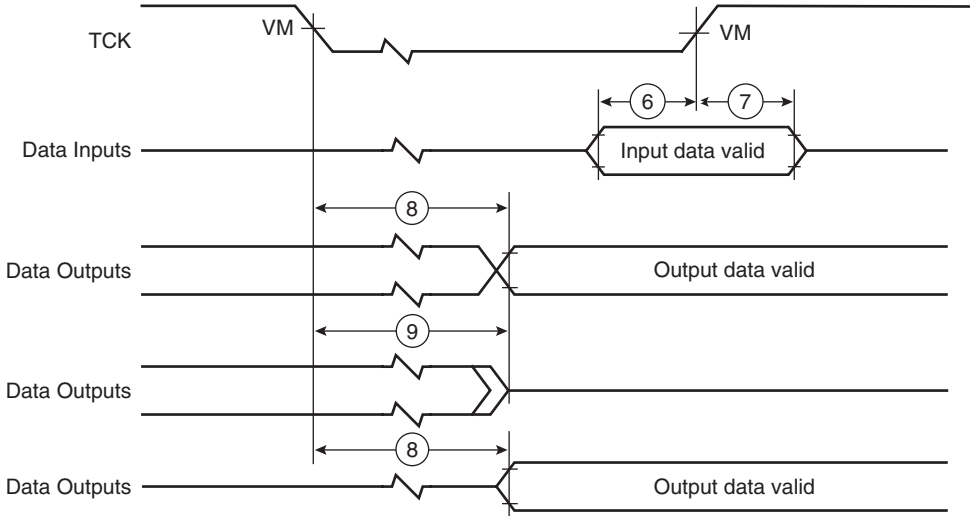
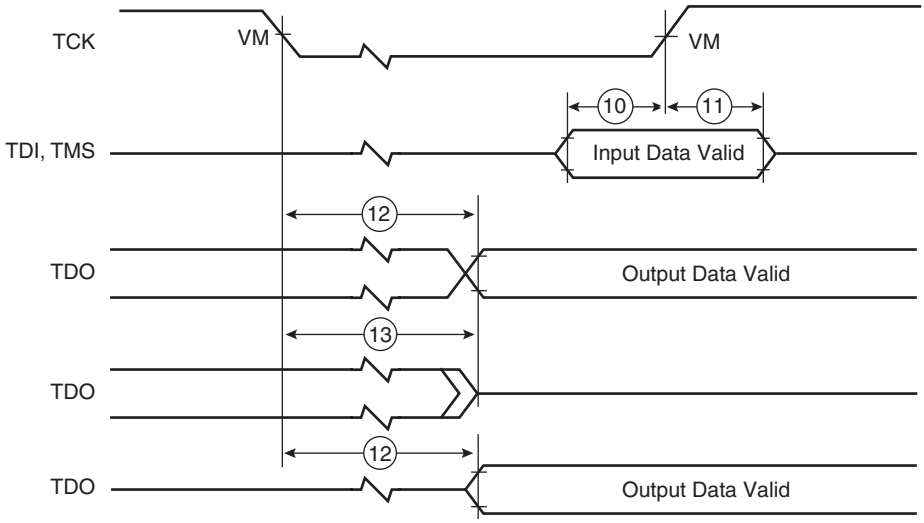


Figure 11-8. Test Access Port Timing Diagram



12. Functional Description

12.1 PowerPC Registers and Programming Model

The PowerPC architecture defines register-to-register operations for most computational instructions. Source operands for these instructions are accessed from the registers or are provided as immediate values embedded in the instruction opcode. The three-register instruction format allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory.

PowerPC processors have two levels of privilege—supervisor mode of operation (typically used by the operating system) and user mode of operation (used by the application software). The programming models incorporate 32 GPRs, 32 FPRs, Special-purpose Registers (SPRs) and several miscellaneous registers. Each PowerPC microprocessor also has its own unique set of Hardware Implementation (HID) registers.

12.2 Instruction Set and Addressing Modes

The following subsections describe the PowerPC instruction set and addressing modes in general.

12.2.1 PowerPC Instruction Set and Addressing Modes

All PowerPC instructions are encoded as single-word (32-bit) opcodes. Instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses. This fixed instruction length and consistent format greatly simplifies instruction pipelining.

PowerPC Instruction Set

The PowerPC instructions are divided into the following categories:

- **Integer Instructions** – these include computational and logical instructions
  - Integer arithmetic instructions
  - Integer compare instructions
  - Integer logical instructions
  - Integer rotate and shift instructions
- **Floating-point Instructions** – these include floating-point computational instructions, as well as instructions that affect the FPSCR
  - Floating-point arithmetic instructions
  - Floating-point multiply/add instructions
  - Floating-point rounding and conversion instructions
  - Floating-point compare instructions
  - Floating-point status and control instructions
- **Load/Store Instructions** – these include integer and floating-point load and store instructions
  - Integer load and store instruction
  - Integer load and store multiple instructions
  - Floating-point load and store
  - Primitives used to construct atomic memory operations (**lwarx** and **stwcx** instructions)
- **Flow Control Instructions** – these include branching instructions, condition register logical instructions, trap instructions, and other instructions that affect the instruction flow
  - Branch and trap instructions
  - Condition register logical instructions
- **Processor Control Instructions** – these instructions are used for synchronizing memory accesses and management of caches, TLBs, and the segment registers
  - Move to/from SPR instructions
  - Move to/from MSR
  - Synchronize
  - Instruction synchronize

- **Synchronous, Imprecise** – the PowerPC architecture defines two imprecise floating-point exception modes, recoverable and nonrecoverable. Even though the 603R provides a means to enable the imprecise modes, it implements these modes identically to the precise mode (That is, all enabled floating-point exceptions are always precise on the 603R).
- **Asynchronous, Maskable** – the external, SMI, and decrementer interrupts are maskable asynchronous exceptions. When these exceptions occur, their handling is postponed until the next instruction, and any exceptions associated with that instruction completes execution. If there are no instructions in the execution units, the exception is taken immediately upon determination of the correct restart address (for loading SRR0).
- **Asynchronous, Non-maskable** – there are two non-maskable asynchronous exceptions: the system reset and machine check exception. These exceptions may not be recoverable, or may provide a limited degree of recoverability. All exceptions report recoverability through the SMR[RI] bit.

12.3.5 PowerPC 603R Microprocessor Exception Model

As specified by the PowerPC architecture, all 603R exceptions can be described as either precise or imprecise and either synchronous or asynchronous. Asynchronous exceptions (some of which are maskable) are caused by events external to the processor's execution; synchronous exceptions, which are all handled precisely by the 603R, are caused by instructions. The 603R exception classes are shown in Table 12-1.

Table 12-1. PowerPC 603R Microprocessor Exception Classifications

Synchronous/Asynchronous	Precise/Imprecise	Exception Type
Asynchronous, Non Maskable	Imprecise	Machine check System reset
Asynchronous, Maskable	Precise	External interrupt Decrementer System management interrupt
Synchronous	Precise	Instruction-caused exceptions

Although exceptions have other characteristics as well, such as whether they are maskable or non-maskable, the distinctions shown in Table 12-1 define categories of exceptions that the 603R handles uniquely. Note that Table 12-1 includes no synchronous imprecise instructions. While the PowerPC architecture supports imprecise handling of floating-point exceptions, the 603R implements these exception modes as precise exceptions.

The 603R's exceptions, and conditions that cause them, are listed in Table 12-2. Exceptions that are specific to the 603R are indicated.

Table 12-2. Exceptions and Conditions

Exception Type	Vector Offset (hex)	Causing Conditions
Reserved	00000	–
System reset	00100	A system reset is caused by the assertion of either SRESET or HRESET
Machine check	00200	A machine check is caused by the assertion of the TEA signal during a data bus transaction, assertion of MCP, or an address or data parity error

Table 12-2. Exceptions and Conditions (Continued)

Exception Type	Vector Offset (hex)	Causing Conditions
DSI	00300	The cause of a DSI exception can be determined by the bit settings in the DSISR, listed as follows: 1 Set if the translation of an attempted access is not found in the primary hash table entry group (HTEG), or in the rehashed secondary HTEG, or in the range of the DBAT register; otherwise cleared 4 Set if a memory access is not permitted by the page or DBAT protection mechanism; otherwise cleared 5 Set by an **eciwx** or **ecowx** instruction if the access is to an address that is marked as write-through, or execution of a load/store instruction that accesses a direct-store segment 6 Set for a store operation and cleared for a load operation 11 Set if **eciwx** or **ecowx** is used and EAR[E] is cleared
ISI	00400	An ISI exception is caused when an instruction fetch cannot be performed for any of the following reasons: • The effective (logical) address cannot be translated. That is, there is a page fault for this portion of the translation, so an ISI exception must be taken to load the PTE (and possibly the page) into memory • The fetch access violates memory protection. If the key bits (Ks and Kp) in the segment register and the PP bits in the PTE are set to prohibit read access, instructions cannot be fetched from this location
External interrupt	00500	An external interrupt is caused when MSR[EE] = 1 and the INT signal is asserted
Alignment	00600	An alignment exception is caused when the 603e cannot perform a memory access for any of the reasons described below: • The operand of a floating-point load or store instruction is not word-aligned • The operand of **lmw**, **stmw**, **lwarx**, and **stwcx**, instructions are not aligned • The operand of a single-register load or store operation is not aligned, and the 603e is in little-endian mode • The instruction is **lmw**, **stmw**, **lswi**, **lwsx**, **stswi**, **stswx** and the 603e is in little-endian mode • The operand of **dcbz** is in storage that is write-through-required, or caching inhibited

- The complete/writeback pipeline stage maintains the correct architectural machine state and transfers the contents of the rename registers to the GPRs and FPRs as instructions are retired. If the completion logic detects an instruction causing an exception, all following instructions are cancelled, their execution results in rename registers are discarded, and instructions are fetched from the correct instruction stream.

A superscalar processor is one that issues multiple independent instructions into multiple pipelines allowing instructions to execute in parallel. The 603R has five independent execution units, one each for integer instructions, floating-point instructions, branch instructions, load/store instructions, and system register instructions. The IU and the FPU each have dedicated register files for maintaining operands (GPRs and FPRs, respectively), enabling integer calculations and floating-point calculations to occur simultaneously without interference.

Because the PowerPC architecture can be applied to such a wide variety of implementations, instruction timing among various PowerPC processors varies accordingly.

13. Preparation for Delivery

13.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

13.2 Certificate of Compliance

Atmel offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with the MIL-STD-883 standard and guaranteeing the parameters that are not tested at temperature extremes for the entire temperature range.

13.3 Handling

MOS devices must be handled with certain precautions to avoid damage caused by an accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

1. The devices should be handled on benches with conductive and grounded surfaces.
2. Ground test equipment and tools should be used.
3. The devices should not be handled by the leads.
4. The devices should be stored in conductive foam or carriers.
5. Use of plastic, rubber, or silk in MOS areas should be avoided.
6. Relative humidity above 50 percent should be maintained if practical.

13.4 Choice of Clock Relationships

The 603R microprocessors provide customers with numerous clocking options. An internal phase-lock loop synchronizes the processor (CPU) clock to the bus or system clock (SYSCLK) at various ratios.

Inside each PowerPC microprocessor is a phase-lock loop circuit. A Voltage Controlled Oscillator (VCO) is precisely controlled in frequency and phase by a frequency/phase detector which compares the input bus frequency (SYSCLK frequency) to a submultiple of the VCO.

The ratio of CPU to SYSCLK frequencies is often referred to as the bus mode (for example, 2:1 bus mode).

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz
1010	4x	2x	–	–	160 (320)	200 (400)	–	–
0111	4.5x	2x	–	150 (300)	180 (360)	–	–	–
1011	5x	2x	–	166 (333)	200 (400)	–	–	–
1001	5.5x	2x	–	183 (366)	–	–	–	–
1101	6x	2x	150 (300)	200 (400)	–	–	–	–
0011	PLL bypass							
1111	Clock off							

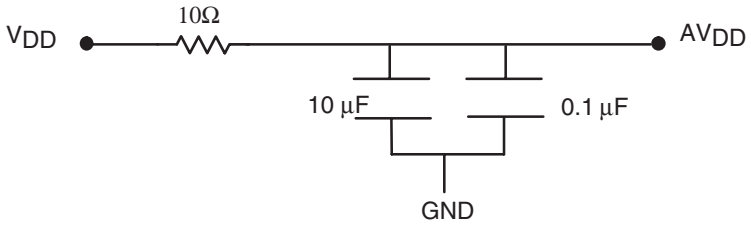
Notes: 1. Some PLL configurations may select bus, CPU or VCO frequencies which are not supported.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
The AC timing specifications given in this document do not apply in PLL-bypass mode.
3. In clock-off mode, no clocking occurs inside the 603e regardless of the SYSCLK input.

14. System Design Information

14.1 PLL Power Supply Filtering

The AV_{DD} power signal is implemented on the 603e to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 14-1. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible. The 0.1 µF capacitor should be closest to the AV_{DD} pin, followed by the 10 µF capacitor, and finally the 10Ω resistor to V_{DD}. These traces should be kept short and direct.

Figure 14-1. PLL Power Supply Filter Circuit



14.2 Decoupling Recommendations

Due to the 603e's dynamic power management feature, large address and data buses, and high operating frequencies, the 603e can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 603e system, and the 603e itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} and OV_{DD} pin of the 603e. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 µF to provide both high and low frequency filtering, and should be placed as close as possible to their associated V_{DD} or OV_{DD} pin. The suggested values for the V_{DD} pins are 220 pF (ceramic), 0.01 µF (ceramic) and 0.1 µf (ceramic). The suggested values for the OV_{DD} pins are 0.01 µF (ceramic), 0.1 µF (ceramic), and 10 µF (tantalum). Only SMT (Surface Mount Technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should also have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. The suggested bulk capacitors are 100 µF (AVX TPS tantalum) or 330 µf (AVX TPS tantalum).

14.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD}. Unused active high inputs should be connected to GND. All NC (non-connected) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins of the 603e.

14.4 Pull-up Resistor Requirements

The 603e requires high-resistive (weak: 10 kΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the 603e or other bus master. These signals are: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$.

In addition, the 603e has three open-drain style outputs that require pull-up resistors (weak or stronger: 4.7 kΩ - 10 kΩ) if they are used by the system. These signals are: $\overline{APE}$, $\overline{DPE}$, and $\overline{CKSTP\_OUT}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the 603e must continually monitor these signals for snooping, this floating condition may cause excessive power to be drawn by the input revivers on the 603e. It is recommended that these signals be pulled up through weak (10 kΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are: A[0-3], AP[0-3], TT[0-4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

15.2 CBGA Package Parameters

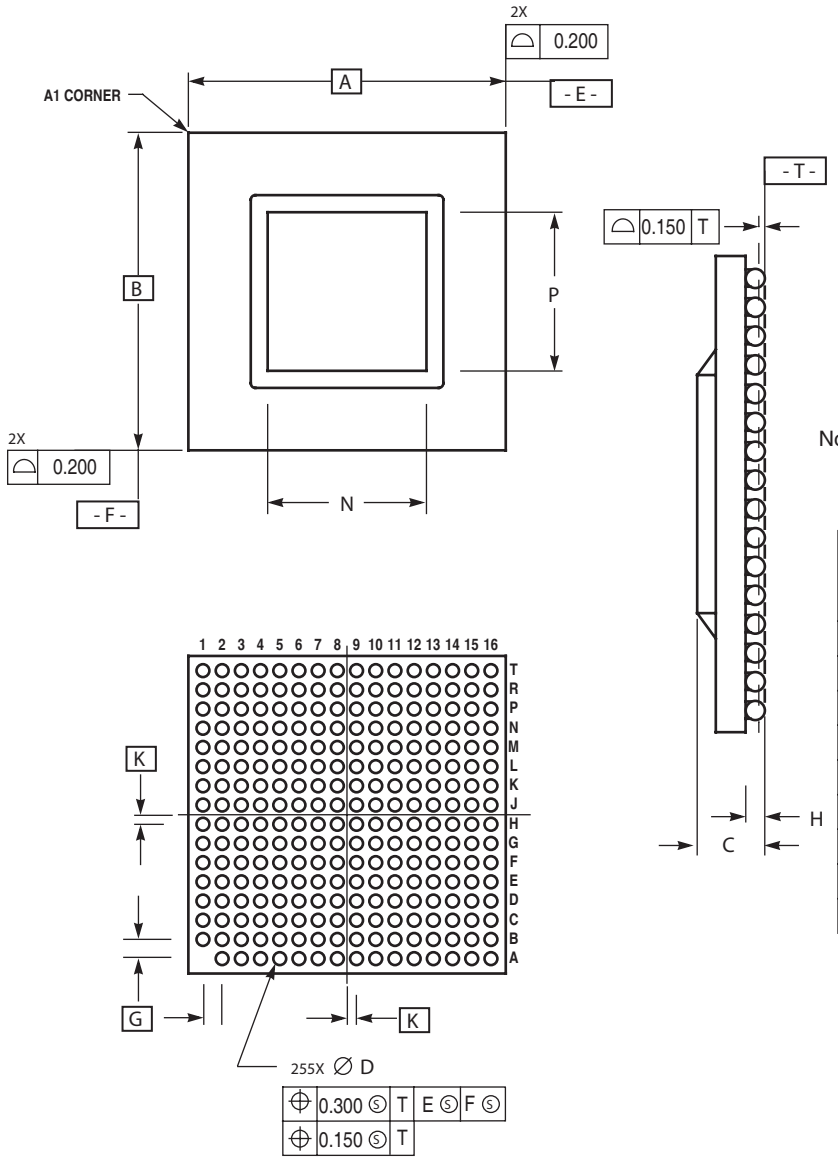
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead Ceramic Ball Grid Array (CBGA).

Package outline	21 mm × 21 mm
Interconnects	255
Pitch	1.27 mm
Maximum module height	3 mm

15.2.1 Mechanical Dimensions of the CBGA Package

Figure 15-2 provides the mechanical dimensions and bottom surface nomenclature of the CBGA package.

Figure 15-2. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package

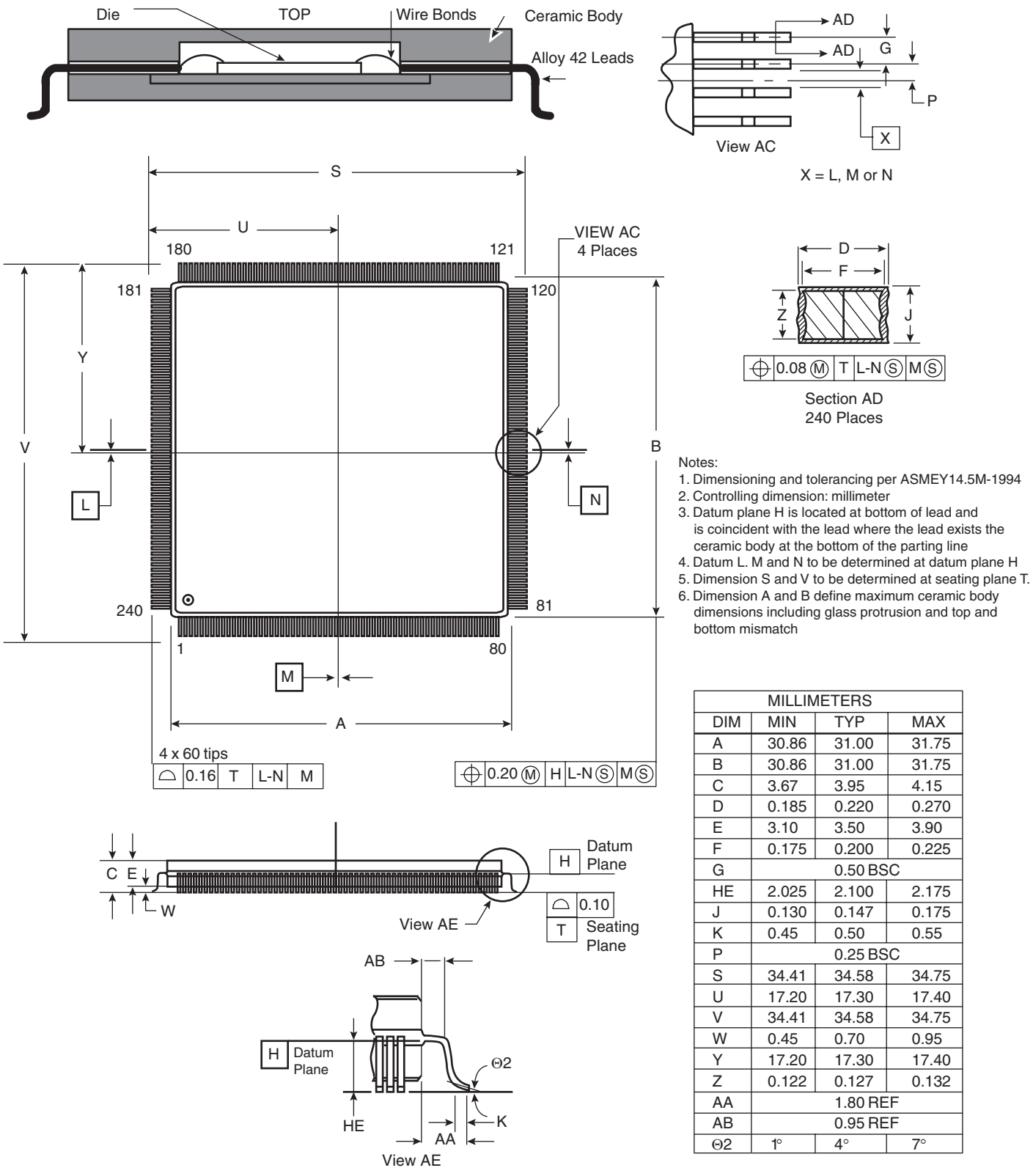


Notes: 1. Dimensioning and tolerancing per ASME Y14.5M - 1994
2. controlling dimension: millimeter

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.450	3.000	0.097	0.118
D	0.820	0.930	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

15.4 CERQUAD 240 Package

Figure 15-4. Mechanical Dimensions of the Wire-bond CERQUAD Package



Notes:
1. Dimensioning and tolerancing per ASMEY14.5M-1994
2. Controlling dimension: millimeter
3. Datum plane H is located at bottom of lead and is coincident with the lead where the lead exists the ceramic body at the bottom of the parting line
4. Datum L. M and N to be determined at datum plane H
5. Dimension S and V to be determined at seating plane T.
6. Dimension A and B define maximum ceramic body dimensions including glass protrusion and top and bottom mismatch

MILLIMETERS			
DIM	MIN	TYP	MAX
A	30.86	31.00	31.75
B	30.86	31.00	31.75
C	3.67	3.95	4.15
D	0.185	0.220	0.270
E	3.10	3.50	3.90
F	0.175	0.200	0.225
G		0.50 BSC	
HE	2.025	2.100	2.175
J	0.130	0.147	0.175
K	0.45	0.50	0.55
P		0.25 BSC	
S	34.41	34.58	34.75
U	17.20	17.30	17.40
V	34.41	34.58	34.75
W	0.45	0.70	0.95
Y	17.20	17.30	17.40
Z	0.122	0.127	0.132
AA		1.80 REF	
AB		0.95 REF	
Θ2	1°	4°	7°

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