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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	233MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	255-BCBGA Exposed Pad
Supplier Device Package	255-HiTCE-CBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgh10lc

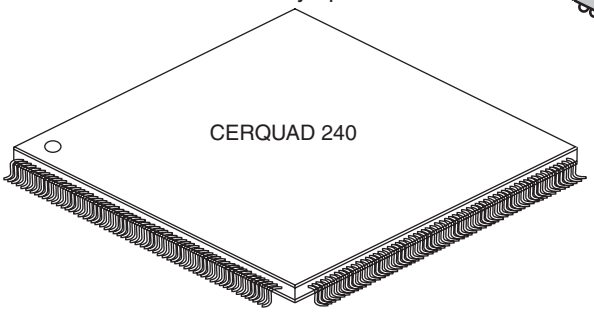
The 603R uses an advanced, 2.5/3.3V CMOS process technology and maintains full interface compatibility with TTL devices. It also integrates in-system testability and debugging features through JTAG boundary-scan capabilities.

2. Screening/Quality/Packaging

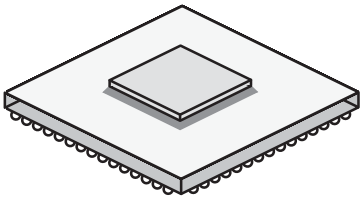
This product is manufactured in full compliance with:

- HiTCE CBGA according to Atmel Standards
- CI-CGA 255 and Cerquad: MIL-PRF-38535 class Q or according to Atmel standards
- CBGA 255: Upscreenings based upon Atmel standards
- CBGA, CI-CGA, HiTCE packages:
  - Full military temperature range (T_C = -55°C, T_j = +125°C)
  - Industrial temperature range (T_C = -40°C, T_j = +110°C)
- Cerquad:
  - Full military temperature range (T_C = -55°C, T_c = +125°C)
  - Industrial temperature range (T_C = -40°C, T_c = +110°C)
  - Commercial temperature ranges (T_C = 0°C, T_C = +70°C)
- Internal I/O Power Supply = 2.5 ±5% // 3.3V ±5%

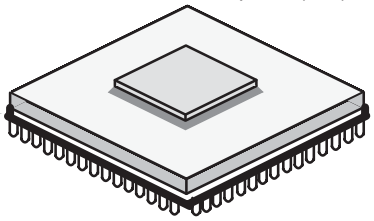
A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier
Cavity up



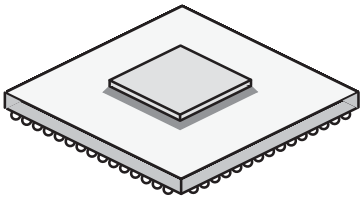
G suffix
CBGA 255
Ceramic Ball Grid Array



GS suffix
CI-CGA 255
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)

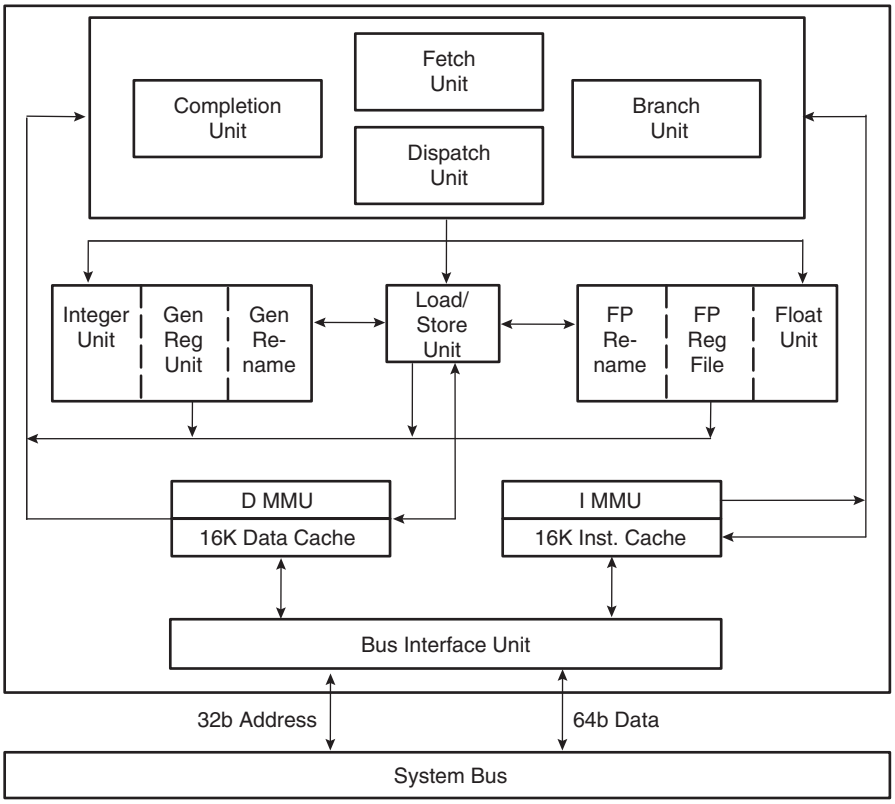


GH suffix
HiTCE 255
Ceramic Ball Grid Array



3. Block Diagram

Figure 3-1. Block Diagram



4. Overview

The 603R is a low-power implementation of the PowerPC microprocessor family of Reduced Instruction Set Computing (RISC) microprocessors. The 603R implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603R provides four software controllable power-saving modes. Three of the modes (nap, doze, and sleep) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603R to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603R is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can be executed in any order for increased performance, but, the 603R makes completion appear sequential.

The 603e integrates five execution units:

- an Integer Unit (IU)
- a Floating-point Unit (FPU)
- a Branch Processing Unit (BPU)

7.1 Design and Construction

7.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 10-2 on page 15, Table 10-4 on page 18, "Recommended Operating Conditions" on page 6, Figure 15-2 on page 49, Figure 15-4 on page 52 and Figure 5-1 on page 5.

7.1.2 *Lead Material and Finish*

Lead material and finish shall be as specified in MIL-STD-1835. (See "Package Mechanical Data" on page 47.)

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only and functional operation at the maximum is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

7.2.1 Absolute Maximum Ratings for the 603R(1)(2)(3)

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	-0.3	2.75	V
PLL supply voltage	AV_{DD}	-0.3	2.75	V
I/O supply voltage	OV_{DD}	-0.3	3.6	V
Input voltage	V_{IN}	-0.3	5.5	V
Storage temperature range	T_{STG}	-55	+150	°C

Notes:
1. **Caution**: The input voltage must not be greater than OV_{DD} by more than 2.5V at any time, including during power-on reset.
2. **Caution**: The OV_{DD} voltage must not be greater than V_{DD}/AV_{DD} by more than 1.2V at any time, including during power-on reset.
3. **Caution**: The V_{DD}/AV_{DD} voltage must not be greater than OV_{DD} by more than 0.4V at any time, including during power-on reset.

Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

7.2.2 Recommended Operating Conditions

The following are the recommended and tested operating conditions. Proper device operation outside of these ranges is not guaranteed.

7.2.3 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	2.375	2.625	V
PLL supply voltage	AV_{DD}	2.375	2.625	V
I/O supply voltage	OV_{DD}	3.135	3.465	V
Input voltage	V_{IN}	GND	5.5	V
Operating temperature	T_c	-55	+125	°C
Junction operating temperature specific to Cerquad	T_j	–	+135	°C

8. Thermal Characteristics

8.1 CBGA 255 and CI-CGA 255 Packages

The data found in this section concerns 603R devices packaged in the 255-lead 21 mm multi-layer ceramic (MLC) and ceramic BGA package. Data is included for use with a Thermalloy #2328B heat sink.

The internal thermal resistance for this package is negligible due to the exposed die design. A thermal interface material is recommended at the package lid to heat sink interface to minimize the thermal contact resistance.

Additionally, the CBGA package offers an excellent thermal connection to the card and power planes. Heat generated at the chip is dissipated through the package, the heat sink (when used) and the card. The parallel heat flow paths result in the lowest overall thermal resistance as well as offer significantly better power dissipation capability if a heat sink is not used.

The thermal characteristics for the flip-chip CBGA and CI-CGA packages are as follows:

Thermal resistance (junction-to-case) = R_{jc} or
θ_{jc} = 0.095°C/Watt for the 2 packages.

Thermal resistance (junction-to-ball) = R_{jb} or
θ_{jb} = 3.5°C/Watt for the CBGA package.

Thermal resistance (junction-to-bottom SCI) = R_{js} or
θ_{js} = 3.7°C/Watt for the CI-CGA package.

The junction temperature can be calculated from the junction to ambient thermal resistance, as follow:

Junction temperature:

$$T_j = T_a + (R_{jc} + R_{cs} + R_{sa}) \times P$$

where: T_a is the ambient temperature in the vicinity of the device

R_{jc} is the die junction to case thermal resistance of the device

R_{cs} is the case to heat sink thermal resistance of the interface material

R_{sa} is the heat sink to ambient thermal resistance

P is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained at a lower value than the value specified in ”Recommended Operating Conditions” on page 6.

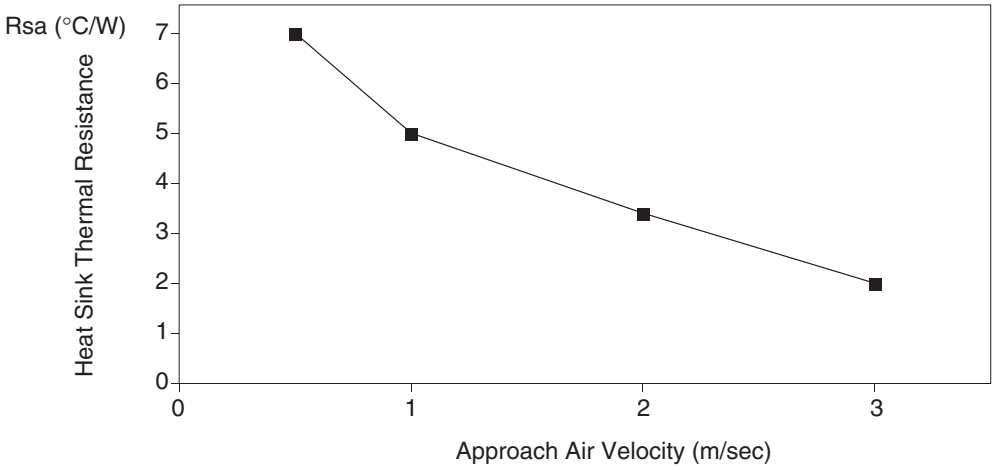
The thermal resistance of the thermal interface material (R_{cs}) is typically about 1°C/Watt.

Assuming a T_a of 85°C and a consumption (P) of 3.6 Watts, the junction temperature of the device would be as follow:

T_j = 85°C + (0.095°C/Watt + 1°C/Watt + R_{sa}) × 3.5 Watts.

For the Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (R_{sa}) versus airflow velocity is shown in Figure 8-1.

Figure 8-1. CBGA Thermal Management Example



Assuming an air velocity of 1 m/sec, the associated overall thermal resistance and junction temperature, found in Table 8-1 will result.

Table 8-1. Thermal Resistance and Junction Temperature

Configuration	R_{ja} (°C/W)	T_j (°C)
With 2328B heat sink	5	106

Vendors such as Aavid, Thermalloy®, and Wakefield Engineering can supply heat sinks with a wide range of thermal performance.

8.2 HiTCE CBGA Package

Table 8-2. HiTCE CBGA Package

Characteristic	Symbol	Value	Unit
Junction-to-bottom of balls(1)	$R\theta_J$	7.5	°C/W
Junction-to-ambient thermal resistance natural convection, four-layer (2s2p) board	$R\theta_{JMA}$	22.4(2)	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.7(3)	°C/W

Notes: 1. Simulation, no convection air flow.
2. Per JEDEC JESD51-2 with the board horizontal.
3. Per JEDEC JESD51-8 with the board horizontal.

8.3 CERQUAD 240 Package

This section provides thermal management data for the 603R. This information is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, wire-bond CERQUAD package with the cavity up (the silicon die is attached to the bottom of the package). This configuration enables dissipation through the PCB.

The thermal characteristics for a wire-bond CERQUAD package are as follows:

- Thermal resistance (junction to bottom of the case) (typical) = $R_{\theta jc}$ or θ_{jc} = 2.5°C/Watt
- Thermal resistance (junction to top of the case) is typically 16°C/W

- Functional units are clocked only when needed
- No software or hardware intervention required after mode is set
- Software/hardware and performance are transparent

Doze Mode

The doze mode disables most functional units but maintains cache coherency by enabling the bus interface unit and snooping. A snoop hit will cause the 603R to enable the data cache, copy the data back to the memory, disable the cache, and fully return to the doze state. In this mode:

- Most functional units are disabled
- Bus snooping and time base/decrementer are still enabled
- Dose mode sequence:
  - Set doze bit (HID0[8] = 1)
  - 603R enters doze mode after several processor clocks
- There are several methods for returning to full-power mode
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- The Transition to full-power state takes no more than a few processor cycles
- Phase Locked Loop (PLL) running and locked to SYSCLK

Nap Mode

The nap mode disables the 603R but still maintains the phase locked loop (PLL) and the time base/decrementer. The time base can be used to restore the 603R to full-on state after a programmed amount of time. Because bus snooping is disabled for nap and sleep modes, a hardware handshake using the quiesce request ($\overline{\text{QREQ}}$) and quiesce acknowledge ($\overline{\text{QACK}}$) signals is required to maintain data coherency. The 603R will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603R will enter the sleep or nap mode. In this mode:

- The time base/decrementer is still enabled
- Most functional units are disabled (including bus snooping)
- All non-essential input receivers are disabled
- Nap mode sequence:
  - Set nap bit (HID0[9] = 1)
  - 603R asserts quiesce request ($\overline{\text{QREQ}}$) signal
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$) signal
  - 603R enters sleep mode after several processor clocks
- There are several methods for returning to full-power mode:
  - Assert $\overline{\text{INT}}$, $\overline{\text{SPI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- Transition to full-power takes no more than a few processor cycles
- The PLL is running and locked to SYSCLK

Figure 10-1. CBGA 255, HiTCE CBGA 255 and CI–CGA 255 Top View

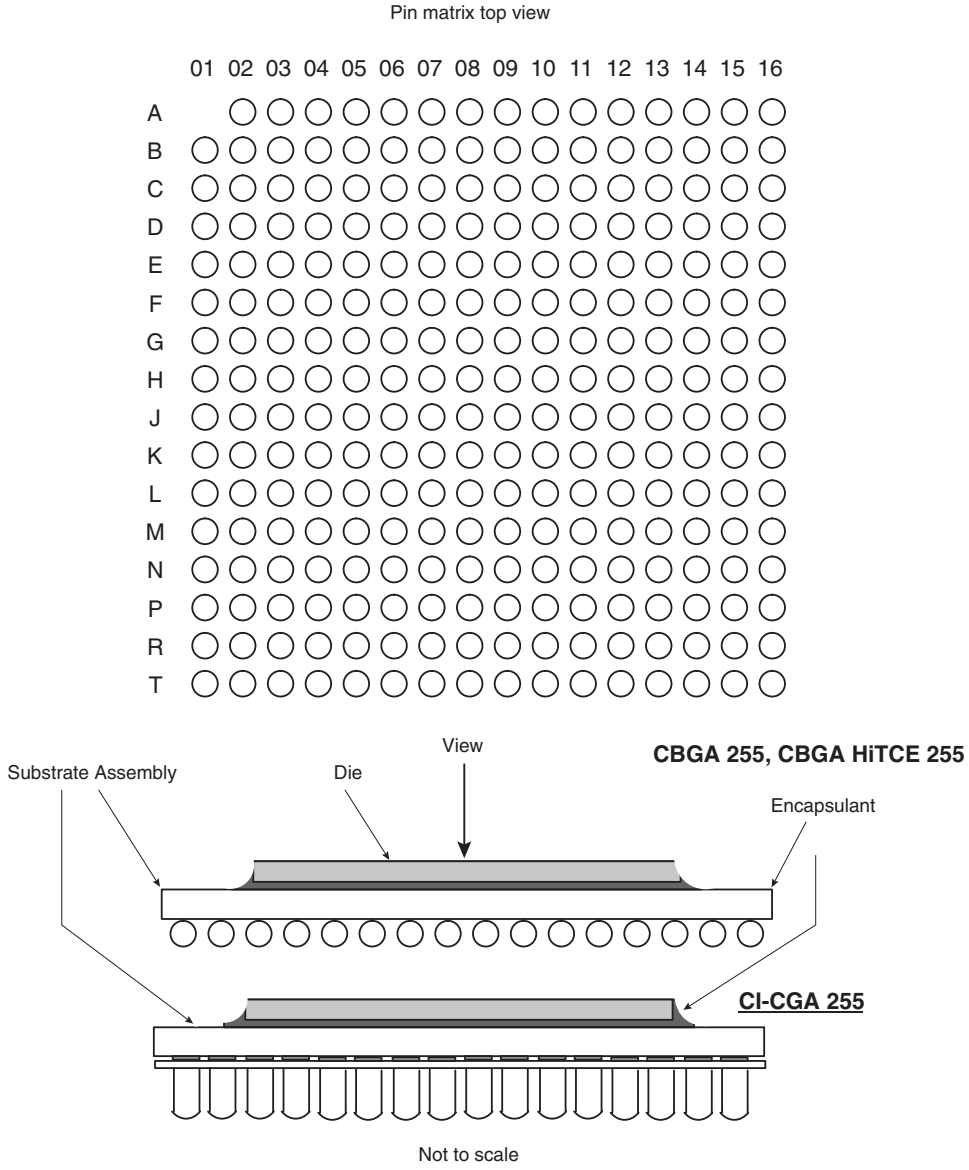


Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

Signal Name	Abbreviation	Signal Function	Signal Type
Global	$\overline{\text{GBL}}$	If output, a transaction is global If input, a transaction must be snooped by the 603R	I/O
Hard Reset	$\overline{\text{HRESET}}$	Initiates a complete hard reset operation	Input
Interrupt	$\overline{\text{INT}}$	Initiates an interrupt if bit EE of MSR register is set	Input
Factory Test	$\overline{\text{LSSD\_MODE}}$	LSSD test control signal for factory use only	Input
	L1_TSTCLK	LSSD test control signal for factory use only	Input
	L2_TSTCLK	LSSD test control signal for factory use only	Input
Machine Check Interrupt	$\overline{\text{MCP}}$	Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set	Input
PLL Configuration	PLL_CFG[0-3]	Configures the operation of the PLL and the internal processor clock frequency	Input
Power supply indicator	VOLTDETGND	Available only on BGA package Indicates to the power supply that a low-voltage processor is present.	Output
Quiescent Acknowledge	$\overline{\text{QACK}}$	All bus activity has terminated and the 603R may enter a quiescent (or low power) state	Input
Quiescent Request	$\overline{\text{QREQ}}$	Is requesting all bus activity normally to enter a quiescent (low power) state	Output
Reservation	$\overline{\text{RSRV}}$	Represents the state of the reservation coherency bit in the reservation address register	Output
System Management Interrupt	$\overline{\text{SMI}}$	Initiates a system management interrupt operation if the bit EE of MSR register is set	Input
Soft Reset	$\overline{\text{SRESET}}$	Initiates processing for a reset exception	Input
System Clock	SYSCLK	Represents the primary clock input for the 603R, and the bus clock frequency for 603R bus operation	Input
Test Clock	CLK_OUT	Provides PLL clock output for PLL testing and monitoring	Output
Transfer Acknowledge	$\overline{\text{TA}}$	A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully	Input
Timebase Enable	TBEN	The timebase should continue clocking	Input
Transfer Burst	$\overline{\text{TBST}}$	If output, a burst transfer is in progress If input, when snooping for single-beat reads	I/O
Transfer Code	TC[0-1]	Special encoding for the transfer in progress	Output
Test Clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)	Input
Test Data Input	TDI	Serial data input for the TAP	Input
Test Data Output	TDO	Serial data output for the TAP	Output
Transfer Error Acknowledge	$\overline{\text{TEA}}$	A bus error occurred	Input
TLBI Sync	$\overline{\text{TLBISYNC}}$	Instruction execution should stop after execution of a **tlbsync** instruction	Input
Test Mode Select	TMS	Selects the principal operations of the test-support circuitry	Input
Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset of the TAP controller	Input
Transfer Size	TSIZ[0-2]	For memory accesses, these signals along with $\overline{\text{TBST}}$ indicate the data transfer size for the current bus operation	I/O

Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

Signal Name	Abbreviation	Signal Function	Signal Type
Transfer Start	$\overline{TS}$	If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$)	I/O
Transfer Type	TT[0-4]	Type of transfer in progress	I/O
Write-through	$\overline{WT}$	A single-beat transaction is write-through	Output

11. Electrical Characteristics

11.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 11-1: Static electrical characteristics for the electrical variants
- Table 11-2: Dynamic electrical characteristics for the 603R

The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0 to PLL_CFG3 signals. All timings are respectively specified to the rising edge of SYSCLK.

These specifications are for 166 MHz to 300 MHz processor core frequencies for CBGA 255, HiTCE CBGA 255 and CI-CGA 255 packages and 166 MHz to 200 MHz processor core frequencies for the Cerquad 240 package.

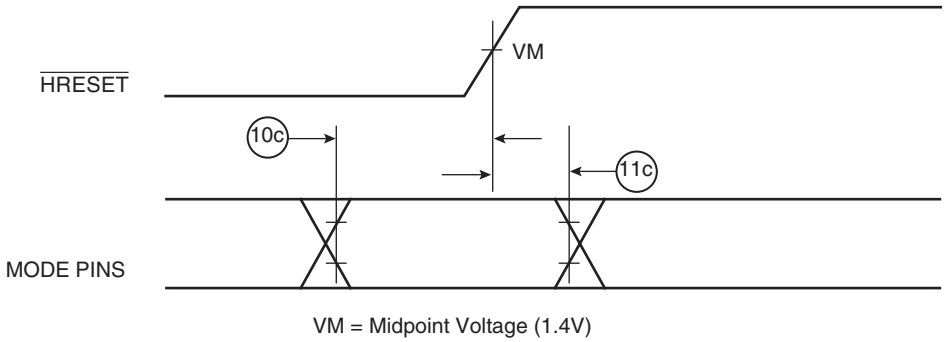
11.2 Static Characteristics

Table 11-1. Electrical Characteristics with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Characteristics		Symbol	Min	Max	Unit
Input High Voltage (all inputs except SYSCLK)		V_{IH}	2	5.5	V
Input Low Voltage (all inputs except SYSCLK)		V_{IL}	GND	0.8	V
SYSCLK Input High Voltage		CV_{IH}	2.4	5.5	V
SYSCLK Input Low Voltage		CV_{IL}	GND	0.4	V
Input Leakage Current	V_{IN} = 3.465V(1)(3)	I_{IN}	-	30	µA
	V_{IN} = 5.5V(1)(3)	I_{IN}	-	300	µA
Hi-Z (off-state) Leakage Current	V_{IN} = 3.465V(1)(3)	I_{TSI}	-	30	µA
	V_{IN} = 5.5V(1)(3)	I_{TSI}	-	300	µA
Output High Voltage	I_{OH} = -7 mA	V_{OH}	2.4	-	V
Output Low Voltage	I_{OL} = +7 mA	V_{OL}	-	0.4	V
Capacitance, V_{IN} = 0V, f = 1 MHz(2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{IN}	-	10	pF
Capacitance, V_{IN} = 0V, f = 1 MHz(2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{IN}	-	15	pF

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100% tested.

Figure 11-3. Mode Select Input Timing Diagram



11.3.3 Output AC Specifications

Table 11-4 provides the output AC timing specifications for the 603R (shown in Figure 11-4).

Table 11-4. Output AC Timing Specifications[1][2] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $55°C \le T_C \le 125°C$

Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages		CBGA 255, HiTCE CBGA 255 and CI-CGA 255				Unit	Note
		166, 200 MHz		233, 266 MHz		300 MHz			
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1	–	1	–	1	–	ns	
13a	SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(4)
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	8	–	8	–	8	ns	(6)
14a	SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11	–	11	–	11	ns	(4)
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(6)
15	SYSCLK to output invalid (output hold)	1	–	1	–	1	–	ns	(3)
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	8.5	–	8	–	8	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(7)
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	8	–	7.5	–	7.5	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK}	–	ns	(3)(5) (8)
20	Maximum delay to $\overline{ARTRY}$ precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(8)
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	–	2	–	2	–	2	t_{SYSCLK}	(6)(8)

Figure 11-7. Boundary-scan Timing Diagram

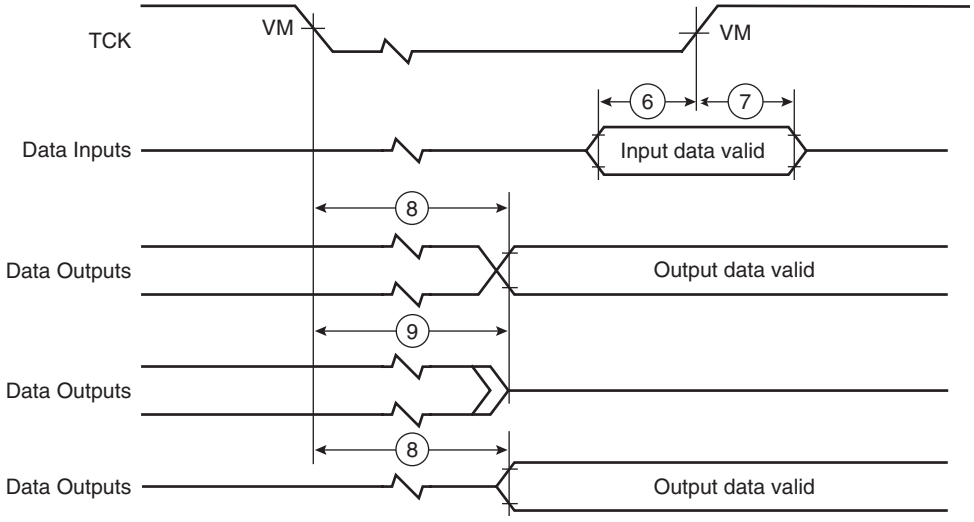
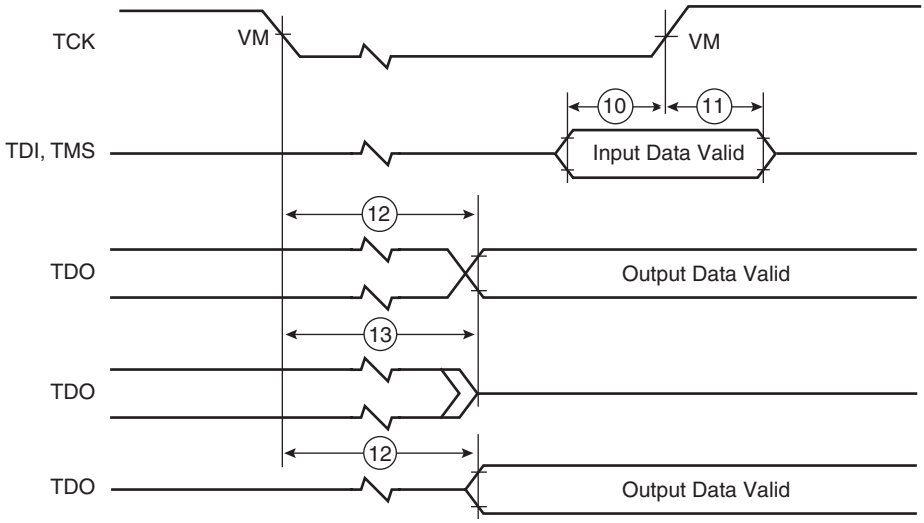


Figure 11-8. Test Access Port Timing Diagram



12. Functional Description

12.1 PowerPC Registers and Programming Model

The PowerPC architecture defines register-to-register operations for most computational instructions. Source operands for these instructions are accessed from the registers or are provided as immediate values embedded in the instruction opcode. The three-register instruction format allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory.

PowerPC processors have two levels of privilege—supervisor mode of operation (typically used by the operating system) and user mode of operation (used by the application software). The programming models incorporate 32 GPRs, 32 FPRs, Special-purpose Registers (SPRs) and several miscellaneous registers. Each PowerPC microprocessor also has its own unique set of Hardware Implementation (HID) registers.

12.2 Instruction Set and Addressing Modes

The following subsections describe the PowerPC instruction set and addressing modes in general.

12.2.1 PowerPC Instruction Set and Addressing Modes

All PowerPC instructions are encoded as single-word (32-bit) opcodes. Instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses. This fixed instruction length and consistent format greatly simplifies instruction pipelining.

PowerPC Instruction Set

The PowerPC instructions are divided into the following categories:

- **Integer Instructions** – these include computational and logical instructions
  - Integer arithmetic instructions
  - Integer compare instructions
  - Integer logical instructions
  - Integer rotate and shift instructions
- **Floating-point Instructions** – these include floating-point computational instructions, as well as instructions that affect the FPSCR
  - Floating-point arithmetic instructions
  - Floating-point multiply/add instructions
  - Floating-point rounding and conversion instructions
  - Floating-point compare instructions
  - Floating-point status and control instructions
- **Load/Store Instructions** – these include integer and floating-point load and store instructions
  - Integer load and store instruction
  - Integer load and store multiple instructions
  - Floating-point load and store
  - Primitives used to construct atomic memory operations (**lwarx** and **stwcx** instructions)
- **Flow Control Instructions** – these include branching instructions, condition register logical instructions, trap instructions, and other instructions that affect the instruction flow
  - Branch and trap instructions
  - Condition register logical instructions
- **Processor Control Instructions** – these instructions are used for synchronizing memory accesses and management of caches, TLBs, and the segment registers
  - Move to/from SPR instructions
  - Move to/from MSR
  - Synchronize
  - Instruction synchronize

- **Memory Control Instructions** – these instructions provide control of caches, TLBs, and segment registers
  - Supervisor-level cache management instructions
  - User-level cache instructions
  - Segment register manipulation instructions
  - Translation lookaside buffer management instructions

Note that this grouping of the instructions does not indicate which execution unit executes a particular instruction or group of instructions.

Integer instructions operate on byte, half-word, and word operands. Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands. The PowerPC architecture uses instructions that are four bytes long and word-aligned. It provides for byte, half-word, and word operand loads and stores between the memory and a set of 32 GPRs. It also provides for word and double-word operand loads and stores between the memory and a set of 32 Floating-point Registers (FPRs).

Computational instructions do not modify the memory. To use a memory operand in a computation and then modify the same or another memory location, the memory contents must be loaded into a register, modified, and then written back to the target location with distinct instructions.

PowerPC processors follow the program flow when they are in the normal execution state. However, the flow of instructions can be interrupted directly by the execution of an instruction or by an asynchronous event. Either kind of exception may cause one of several components of the system software to be invoked.

- Calculating Effective Address

  The Effective Address (EA) is the 32-bit address computed by the processor when executing a memory access or branch instruction or when fetching the next sequential instruction.

  The PowerPC architecture supports two simple memory addressing modes:

  - EA = (RA|0) + offset (including offset = 0) (register indirect with immediate index)
  - EA = (RA|0) + rB (register indirect with index)

These simple addressing modes allow efficient address generation for memory accesses. Calculation of the effective address for aligned transfers occurs in a single clock cycle.

For a memory access instruction, if the sum of the effective address and the operand length exceeds the maximum effective address, the memory operand is considered to wrap around from the maximum effective address to effective address 0.

Effective address computations for both data and instruction accesses use 32-bit unsigned binary arithmetic. A carry over from bit 0 is ignored in 32-bit implementations.

12.2.2 PowerPC 603R Microprocessor Instruction Set

The 603R instruction set is defined as follows:

- The 603R provides hardware support for all 32-bit PowerPC instructions.
- The 603R provides two implementation-specific instructions used for software table search operations following TLB misses:
  - Load Data TLB Entry (**tlbld**)
  - Load Instruction TLB Entry (**tlbli**)
- The 603R implements the following instructions which are defined as optional by the PowerPC architecture :
  - External Control in Word Indexed (**eciwx**)
  - External Control Out Word Indexed (**ecowx**)
  - Floating Select (**fsed**)
  - Floating Reciprocal Estimate Single-Precision (**fres**)
  - Floating Reciprocal Square Root Estimate (**frsqrte**)
  - Store Floating-Point as Integer Word (**stfiwx**)

12.3 Cache Implementation

The following subsections describe the way the PowerPC architecture deals with cache in general, and the 603R's specific implementation.

12.3.1 PowerPC Cache Characteristics

The PowerPC architecture does not define hardware aspects of cache implementations. For example, some PowerPC processors, including the 603R, have separate instruction and data caches (harvard architecture).

The PowerPC microprocessor controls the following memory access modes on a page or block basis:

- Write-back/write-through mode
- Cache-inhibited mode
- Memory coherency

Note that in the 603R, a cache line is defined as eight words. The VEA defines cache management instructions that provide a means by which the application programmer can affect the cache contents.

12.3.2 PowerPC 603R Microprocessor Cache Implementation

The 603R has two 16-Kbyte, four-way set-associative (instruction and data) caches. The caches are physically addressed, and the data cache can operate in either write-back or write-through modes as specified by the PowerPC architecture.

The data cache is configured as 128 sets of four lines each. Each line consists of 32 bytes, two state bits, and an address tag. The two state bits implement the three-state MEI (Modified/Exclusive/Invalid) protocol. Each line contains eight 32-bit words. Note that the PowerPC architecture defines the term block as the cacheable unit. For the 603R, the block size is equivalent to a cache line. A block diagram of the data cache organization is shown in Figure 12-2 on page 36.

- **Synchronous, Imprecise** – the PowerPC architecture defines two imprecise floating-point exception modes, recoverable and nonrecoverable. Even though the 603R provides a means to enable the imprecise modes, it implements these modes identically to the precise mode (That is, all enabled floating-point exceptions are always precise on the 603R).
- **Asynchronous, Maskable** – the external, SMI, and decrementer interrupts are maskable asynchronous exceptions. When these exceptions occur, their handling is postponed until the next instruction, and any exceptions associated with that instruction completes execution. If there are no instructions in the execution units, the exception is taken immediately upon determination of the correct restart address (for loading SRR0).
- **Asynchronous, Non-maskable** – there are two non-maskable asynchronous exceptions: the system reset and machine check exception. These exceptions may not be recoverable, or may provide a limited degree of recoverability. All exceptions report recoverability through the SMR[RI] bit.

12.3.5 PowerPC 603R Microprocessor Exception Model

As specified by the PowerPC architecture, all 603R exceptions can be described as either precise or imprecise and either synchronous or asynchronous. Asynchronous exceptions (some of which are maskable) are caused by events external to the processor's execution; synchronous exceptions, which are all handled precisely by the 603R, are caused by instructions. The 603R exception classes are shown in Table 12-1.

Table 12-1. PowerPC 603R Microprocessor Exception Classifications

Synchronous/Asynchronous	Precise/Imprecise	Exception Type
Asynchronous, Non Maskable	Imprecise	Machine check System reset
Asynchronous, Maskable	Precise	External interrupt Decrementer System management interrupt
Synchronous	Precise	Instruction-caused exceptions

Although exceptions have other characteristics as well, such as whether they are maskable or non-maskable, the distinctions shown in Table 12-1 define categories of exceptions that the 603R handles uniquely. Note that Table 12-1 includes no synchronous imprecise instructions. While the PowerPC architecture supports imprecise handling of floating-point exceptions, the 603R implements these exception modes as precise exceptions.

The 603R's exceptions, and conditions that cause them, are listed in Table 12-2. Exceptions that are specific to the 603R are indicated.

Table 12-2. Exceptions and Conditions

Exception Type	Vector Offset (hex)	Causing Conditions
Reserved	00000	–
System reset	00100	A system reset is caused by the assertion of either SRESET or HRESET
Machine check	00200	A machine check is caused by the assertion of the TEA signal during a data bus transaction, assertion of MCP, or an address or data parity error

The 603R's TLBs are 64-entry, 2-way set-associative caches that contain instruction and data address translations. The 603R provides hardware assistance for software table search operations through the ashed page table on the TLB misses. The supervisor software can invalidate TLB entries selectively.

The 603R also provides independent four-entry BAT arrays for instructions and data that maintain address translations for blocks of memory. These entries define blocks that can vary from 128 Kbytes to 256 Mbytes. The BAT arrays are maintained by system software.

As specified by the PowerPC architecture, the hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

Also as specified by the PowerPC architecture, the page table contains a number of Page Table Entry Groups (PTEGs). A PTEG contains eight Page Table Entries (PTEs) of eight bytes each; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

12.4.3 Instruction Timing

The 603R is a pipelined superscalar processor. A pipelined processor is one in which the processing of an instruction is reduced into discrete stages. Because the processing of an instruction is broken into a series of stages, an instruction does not require the entire resources of an execution unit. For example, after an instruction completes the decode stage, it can pass on to the next stage, while the subsequent instruction can advance into the decode stage. This improves the throughput of the instruction flow. For example, it may take three cycles for a floating-point instruction to complete, but if there are no stalls in the floating-point pipeline, a series of floating-point instructions can have a throughput of one instruction per cycle.

The instruction pipeline in the 603R has four major pipeline stages, described as follows:

- The fetch pipeline stage primarily involves retrieving instructions from the memory system and determining the location of the next instruction retrieval. Additionally, the BPU decodes branches during the fetch stage and folds out branch instructions before the dispatch stage if possible.
- The dispatch pipeline stage is responsible for decoding the instructions supplied by the instruction retrieval stage, and determining which of the instructions are eligible to be dispatched in the current cycle. In addition, the source operands of the instructions are read from the appropriate register file and dispatched with the instruction to the execute pipeline stage. At the end of the dispatch pipeline stage, the dispatched instructions and their operands are latched by the appropriate execution unit.
- During the execute pipeline stage each execution unit that has an executable instruction executes the selected instruction (perhaps over multiple cycles), writes the instruction's result into the appropriate rename register, and notifies the completion stage when the instruction has finished execution. In the case of an internal exception, the execution unit reports the exception to the completion/writeback pipeline stage and discontinues instruction execution until the exception is handled. The exception is not signaled until that instruction is the next to be completed. Execution of most floating-point instructions is pipelined within the FPU allowing up to three instructions to be executing in the FPU concurrently. The pipeline stages for the floating-point unit are multiply, add, and round-convert. Execution of most load/store instructions is also pipelined. The load/store unit has two pipeline stages. The first stage is for effective address calculation and MMU translation and the second stage is for accessing the data in the cache.

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz
1010	4x	2x	–	–	160 (320)	200 (400)	–	–
0111	4.5x	2x	–	150 (300)	180 (360)	–	–	–
1011	5x	2x	–	166 (333)	200 (400)	–	–	–
1001	5.5x	2x	–	183 (366)	–	–	–	–
1101	6x	2x	150 (300)	200 (400)	–	–	–	–
0011	PLL bypass							
1111	Clock off							

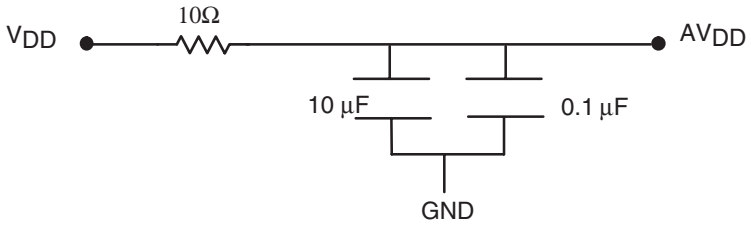
Notes: 1. Some PLL configurations may select bus, CPU or VCO frequencies which are not supported.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
The AC timing specifications given in this document do not apply in PLL-bypass mode.
3. In clock-off mode, no clocking occurs inside the 603e regardless of the SYSCLK input.

14. System Design Information

14.1 PLL Power Supply Filtering

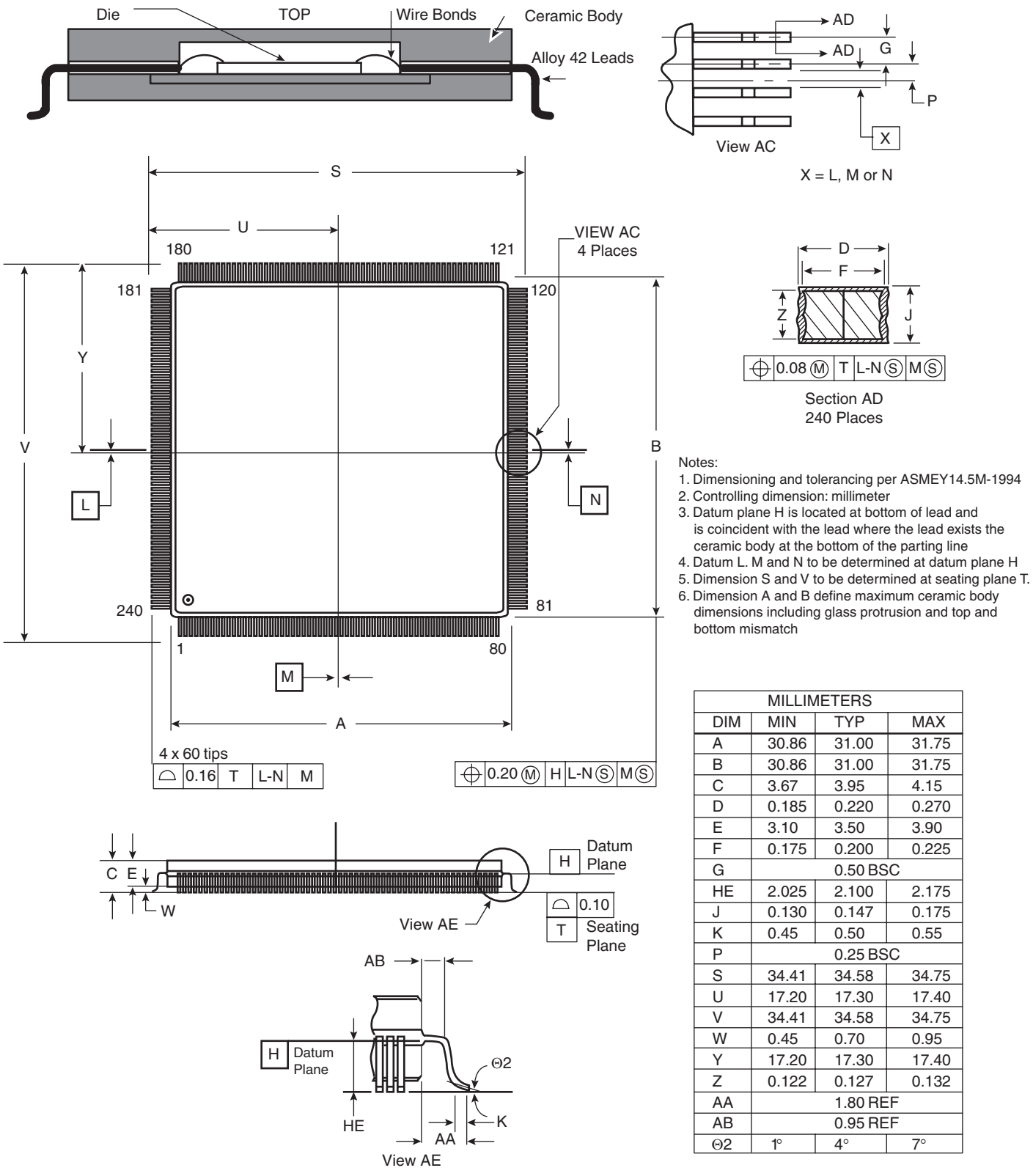
The AV_{DD} power signal is implemented on the 603e to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 14-1. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible. The 0.1 µF capacitor should be closest to the AV_{DD} pin, followed by the 10 µF capacitor, and finally the 10Ω resistor to V_{DD}. These traces should be kept short and direct.

Figure 14-1. PLL Power Supply Filter Circuit



15.4 CERQUAD 240 Package

Figure 15-4. Mechanical Dimensions of the Wire-bond CERQUAD Package

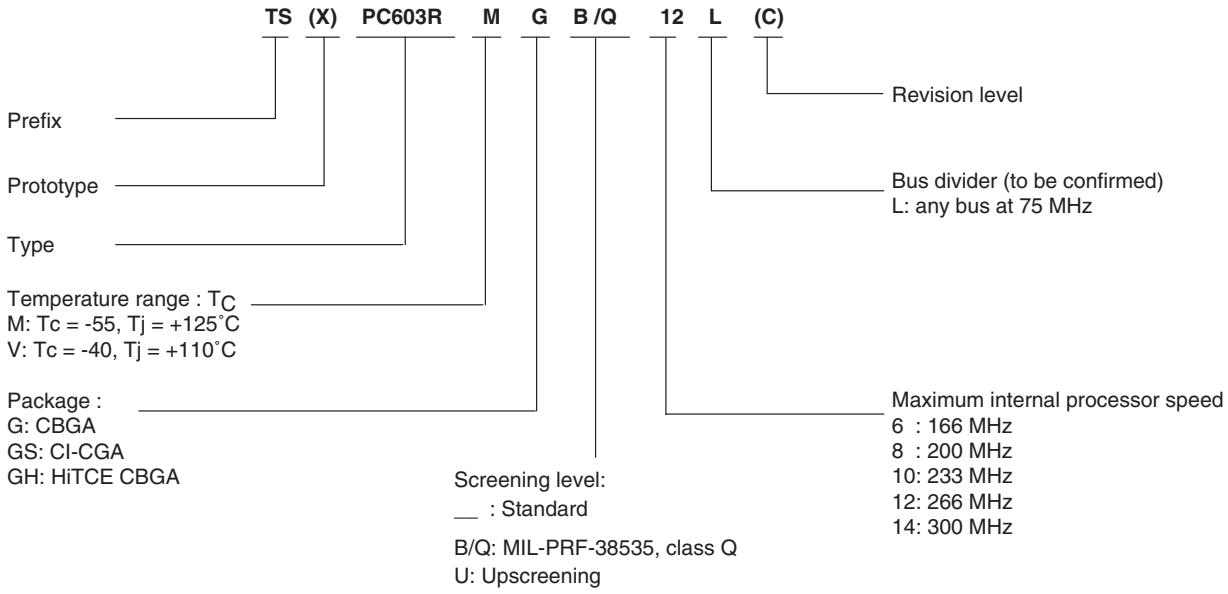


Notes:
1. Dimensioning and tolerancing per ASMEY14.5M-1994
2. Controlling dimension: millimeter
3. Datum plane H is located at bottom of lead and is coincident with the lead where the lead exists the ceramic body at the bottom of the parting line
4. Datum L. M and N to be determined at datum plane H
5. Dimension S and V to be determined at seating plane T.
6. Dimension A and B define maximum ceramic body dimensions including glass protrusion and top and bottom mismatch

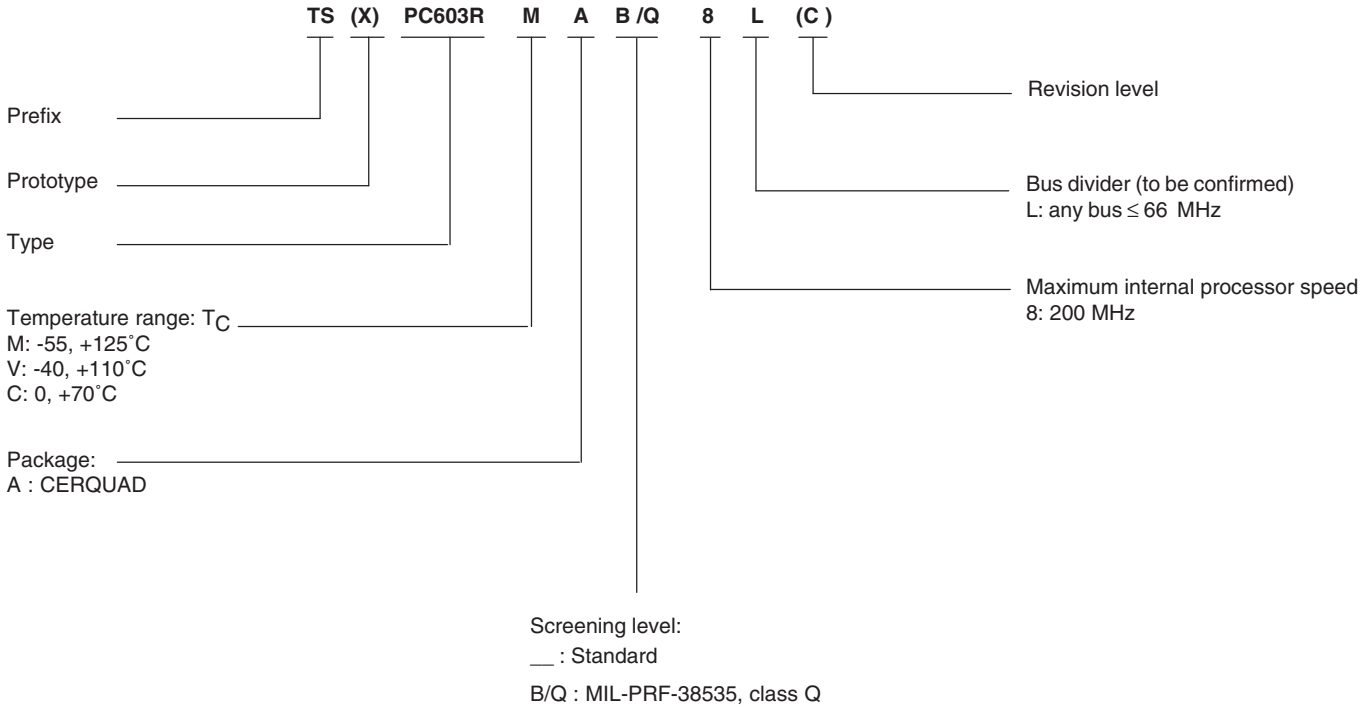
MILLIMETERS			
DIM	MIN	TYP	MAX
A	30.86	31.00	31.75
B	30.86	31.00	31.75
C	3.67	3.95	4.15
D	0.185	0.220	0.270
E	3.10	3.50	3.90
F	0.175	0.200	0.225
G		0.50 BSC	
HE	2.025	2.100	2.175
J	0.130	0.147	0.175
K	0.45	0.50	0.55
P		0.25 BSC	
S	34.41	34.58	34.75
U	17.20	17.30	17.40
V	34.41	34.58	34.75
W	0.45	0.70	0.95
Y	17.20	17.30	17.40
Z	0.122	0.127	0.132
AA		1.80 REF	
AB		0.95 REF	
Θ2	1°	4°	7°

16. Ordering Information

16.1 Ordering Information of the CBGA, CI-CGA and HiTCE Packages



16.2 Ordering Information of the CERQUAD 240 Package



Note: For availability of the different versions, contact your Atmel sales office.

17. Definitions

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with the customer and application validation	Before design phase
Target specification	This datasheet contains target or goal specifications for product development	Valid during the design phase
Preliminary specification α site	This datasheet contains preliminary data. Additional data may be published at a later date and could include simulation results	Valid before characterization phase
Preliminary specification β site	This datasheet also contains characterization results	Valid before the industrialization phase
Product specification	This datasheet contains final product specifications	Valid for production purpose
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stresses above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification		

17.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

18. Document Revision History

Table 18-1 provides a revision history for this hardware specification.

Table 18-1. Document Revision History

Revision Number	Date	Substantive Change(s)
B	07/2005	Added HiTCE package for PowerPC 603R
A	10/2004	This document is a merge of TSPC603R in CBGA255/CI-CGA 255 package (ref 2125B) and TSPC603R in Cerquad package (ref 2127A)