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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	255-BCBGA Exposed Pad
Supplier Device Package	255-HiTCE-CBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgh12lc

- a Load/Store Unit (LSU)
- a System Register Unit (SRU)

The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603R-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603R provides independent on-chip, 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data, as well as on-chip instruction and data Memory Management Units (MMUs). The MMUs contain 64-entry, two-way set-associative, Data and Instruction Translation Lookaside Buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a Least Recently Used (LRU) replacement algorithm. The 603R also supports block address translation through the use of two independent Instruction and Data Block Address Translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation has priority.

The 603R has a selectable 32- or 64-bit data bus and a 32-bit address bus. The 603R interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603R provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (Modified/Exclusive/Shared/Invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603R supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/Os.

The 603R uses an advanced, 0.29 µm 5-metal-layer CMOS process technology and maintains full interface compatibility with TTL devices.

5. Signal Description

Figure 5-1 on page 5, Table 10-5 and Table 10-6 on page 20 describe the signals on the TSPC603R and indicate signal functions. The test signals, $\overline{\text{TRST}}$, TMS, TCK, TDI and TDO, comply with the subset P-1149.1 of the IEEE testability bus standard.

The three signals $\overline{\text{LSSD\_MODE}}$, LI_TSTCLK and L2_TSTCLK are test signals for factory use only and must be pulled up to V_{DD} for normal machine operations.

9.2 Programmable Power Modes

The 603R provides four programmable power states, full power, doze, nap and sleep. The software selects these modes by setting one (and only one) of the three power saving mode bits. The hardware can enable a power management state through external asynchronous interrupts. The hardware interrupt causes the transfer of program flow to interrupt the handler code. The appropriate mode is then set by the software. The 603R provides a separate interrupt and interrupt vector for power management, the System Management Interrupt (SMI). The 603R also contains a decrement timer which allows it to enter the nap or doze mode for a predetermined amount of time and then return to full power operation through the Decrementer Interrupt (DI). Note that the 603R cannot switch from power-on management mode to another without first returning to full on mode. The nap and sleep modes disable bus snooping; therefore, a hardware handshake is provided to ensure coherency before the 603R enters these power management modes.

Table 9-1 summarizes the four power states.

Table 9-1. Power PC 603R Microprocessor Programmable Power Modes

PM Mode	Functioning Units	Activation Method	Full-power Wake-up Method
Full Power	All units active	–	–
Full Power (with DPM)	Requested logic by demand	By instruction dispatch	–
Doze	- Bus snooping - Data cache as needed - Decrementer timer	Controlled by SW	External asynchronous exceptions(1) Decrementer interrupt Reset
Nap	Decrementer timer	Controlled by hardware and software	External asynchronous exceptions Decrementer interrupt Reset
Sleep	None	Controlled by hardware and software	External asynchronous exceptions Reset

Note: 1. Exceptions are referred to as interrupts in the architecture specification.

9.3 Power Management Modes

The following describes the characteristics of the 603R's power management modes, the requirements for entering and exiting the various modes, and the system capabilities provided by the 603R while the power management modes are active.

Full Power Mode with DPM Disabled

Full power mode with DPM disabled; power mode is selected when the DPM enable bit (bit 11) in HID0 is cleared

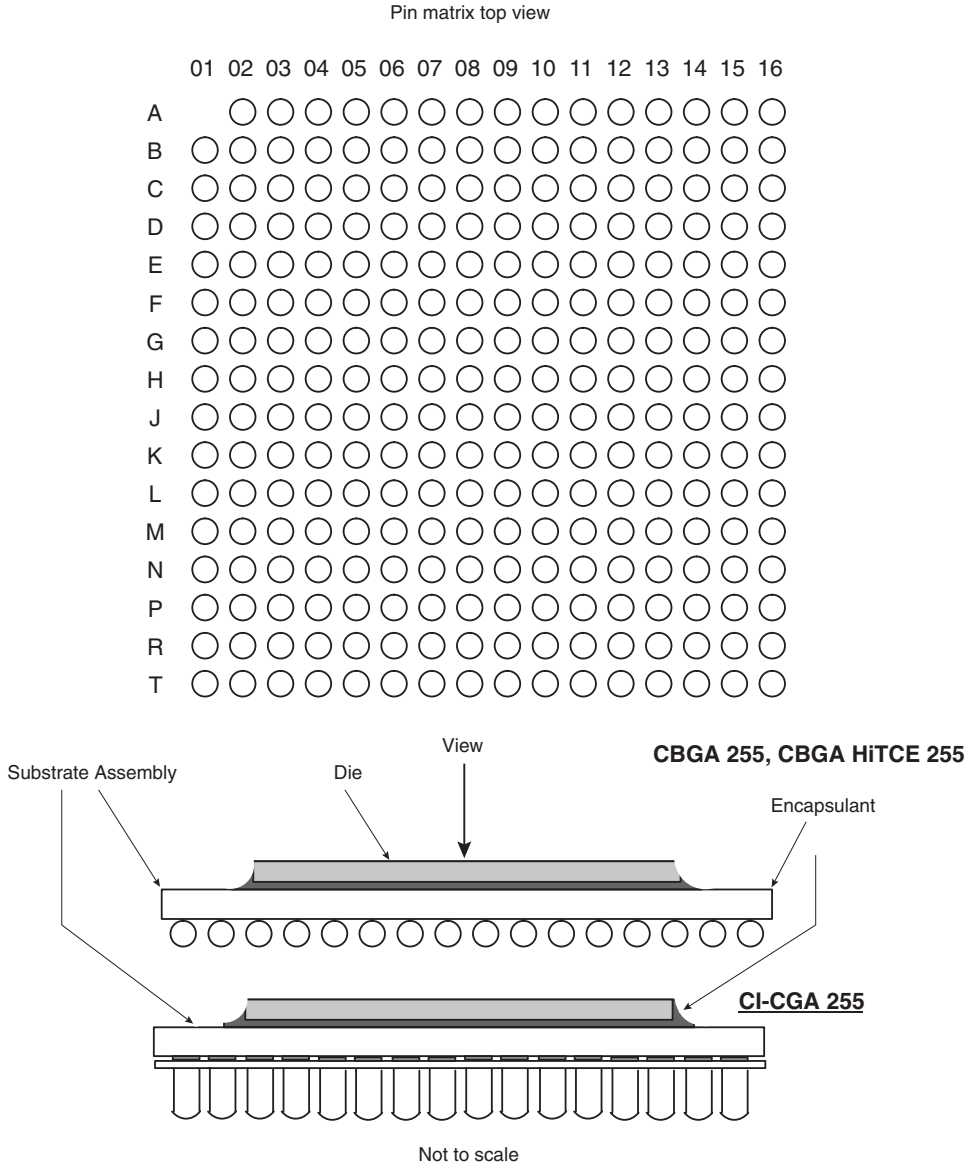
- Default state following power-up and $\overline{\text{HRESET}}$
- All functional units are operating at full processor speed at all times

Full Power Mode with DPM Enabled

Full power mode with DPM enabled (HID0[11] = 1); provides on-chip power management without affecting the functionality or performance of the 603R

- Required functional units are operating at full processor speed

Figure 10-1. CBGA 255, HiTCE CBGA 255 and CI–CGA 255 Top View



10.2.1 Pinout Listing

Table 10-3. Power and Ground Pins

	CERQUAD Pin Number	
	VCC	**GND**
PLL (AV_{DD})	209	
Internal Logic	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239
Output Drivers	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238

Table 10-4. Signal Pinout Listing

Signal Name	CERQUAD Pin Number
A[0-31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37
$\overline{\text{AACK}}$	28
$\overline{\text{ABB}}$	36
AP[0-3]	231,230,227,226
$\overline{\text{APE}}$	218
$\overline{\text{ARTRY}}$	32
$\overline{\text{BG}}$	27
$\overline{\text{BR}}$	219
$\overline{\text{CI}}$	237
$\overline{\text{CKSTP\_IN}}$	215
$\overline{\text{CKSTP\_OUT}}$	216
CLK_OUT	221
CSE[0-1]	225,150
$\overline{\text{DBB}}$	145
$\overline{\text{DBG}}$	26
$\overline{\text{DBDIS}}$	153
$\overline{\text{DBWO}}$	25
DH[0-31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66
DL[0-31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64
DP[0-7]	38, 40, 41, 42, 46, 47, 48, 50
$\overline{\text{DPE}}$	217
$\overline{\text{DRTRY}}$	156
$\overline{\text{GBL}}$	1
$\overline{\text{HRESET}}$	214

11.3.2 Input AC Specifications

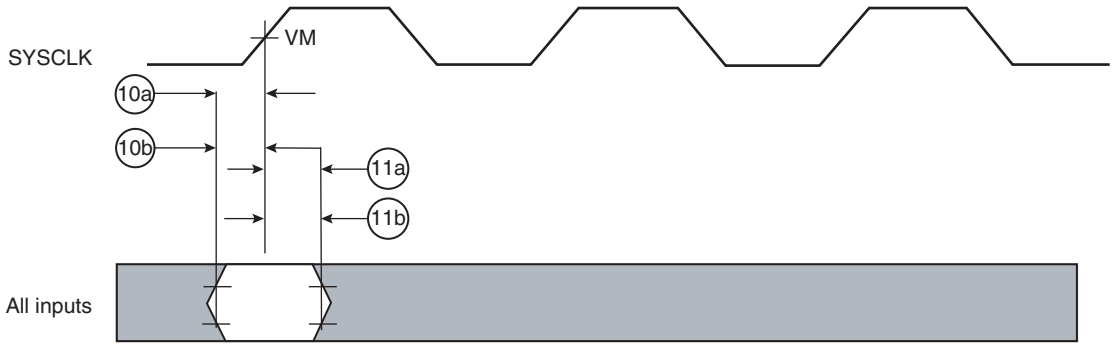
Table 11-3 provides the input AC timing specifications for the 603R as defined in Figure 11-2 and Figure 11-3.

Table 11-3. Input AC Timing Specifications[1] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Figure Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages		CBGA 255, HiTCE CBGA 255 and CI-CGA 255				Unit	Note
		166, 200 MHz		233, 266 MHz		300 MHz			
		Min	Max	Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	2.5	–	2.5	–	2.5	–	ns	(2)
10b	All other inputs valid to SYSCLK (input setup)	4	–	3.5	–	3.5	–	ns	(3)
10c	Mode select inputs valid to $\overline{HRESET}$ (input setup) (for $\overline{DRTRY}$, $\overline{QACK}$ and $\overline{TLBISYNC}$)	8	–	8	–	8	–	t_{sysclk}	(4)(5)(6)(7)
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1	–	1	–	1	–	ns	(2)
11b	SYSCLK to all other inputs invalid (input hold)	1	–	1	–	1	–	ns	(3)
11c	$\overline{HRESET}$ to mode select inputs invalid (input hold) (for $\overline{DRTRY}$, $\overline{QACK}$, and $\overline{TLBISYNC}$)	0	–	0	–	0	–	ns	(4)(6)(7)

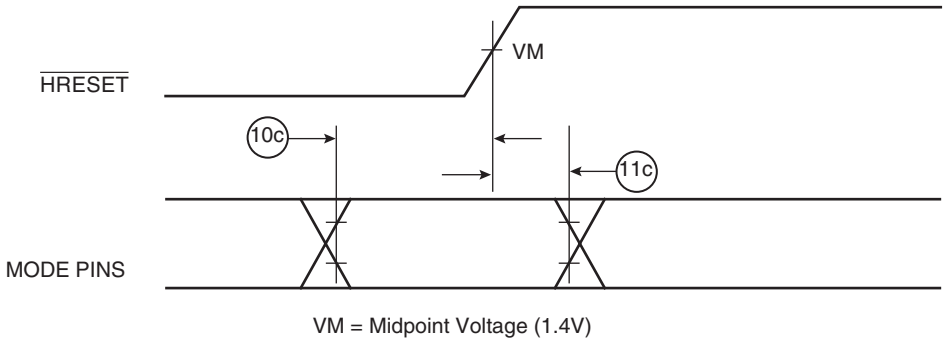
Notes:
1. All input specifications are measured from the TTL level (0.8 or 2V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 11-3.
2. Address/data/transfer attribute input signals are composed of the following: A[0-31], AP[0-3], TT[0-4], TC[0-1], $\overline{TBST}$, TSIZ[0-2], $\overline{GBL}$, DH[0-31], DL[0-31], DP[9-7].
3. All other input signals are composed of the following: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{AACK}$, $\overline{DBG}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{DRTRY}$, $\overline{TEA}$, $\overline{DBDIS}$, $\overline{HRESET}$, $\overline{SRESET}$, $\overline{INT}$, $\overline{SMI}$, $\overline{MCP}$, TBEN, $\overline{QACK}$, $\overline{TLBISYNC}$.
4. The setup and hold time is with respect to the rising edge of $\overline{HRESET}$. See Figure 11-3.
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode only. Also note that $\overline{HRESET}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.

Figure 11-2. Input Timing Diagram



VM = Midpoint Voltage (1.4V)

Figure 11-3. Mode Select Input Timing Diagram



11.3.3 Output AC Specifications

Table 11-4 provides the output AC timing specifications for the 603R (shown in Figure 11-4).

Table 11-4. Output AC Timing Specifications[1][2] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $55°C \le T_C \le 125°C$

Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages		CBGA 255, HiTCE CBGA 255 and CI-CGA 255				Unit	Note
		166, 200 MHz		233, 266 MHz		300 MHz			
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1	–	1	–	1	–	ns	
13a	SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(4)
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	8	–	8	–	8	ns	(6)
14a	SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11	–	11	–	11	ns	(4)
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(6)
15	SYSCLK to output invalid (output hold)	1	–	1	–	1	–	ns	(3)
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	8.5	–	8	–	8	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(7)
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	8	–	7.5	–	7.5	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK}	–	ns	(3)(5) (8)
20	Maximum delay to $\overline{ARTRY}$ precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(8)
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	–	2	–	2	–	2	t_{SYSCLK}	(6)(8)

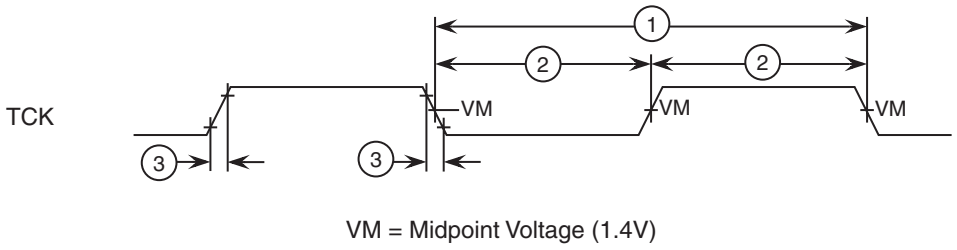
11.4 JTAG AC Timing Specifications

Table 11-5. JTAG AC Timing Specifications (independent of SYSCLK); $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $-55°C \le T_C \le 125°C$

Number	Characteristics	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	–	ns	
2	TCK clock pulse width measured at 1.4V	25	–	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{TRST}$ setup time to TCK rising edge	13	–	ns	(1)
5	$\overline{TRST}$ assert time	40	–	ns	
6	Boundary scan input data setup time	6	–	ns	(2)
7	Boundary scan input data hold time	27	–	ns	(2)
8	TCK to output data valid	4	25	ns	(3)
9	TCK to output high impedance	3	24	ns	(3)
10	TMS, TDI data setup time	0	–	ns	
11	TMS, TDI data hold time	25	–	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

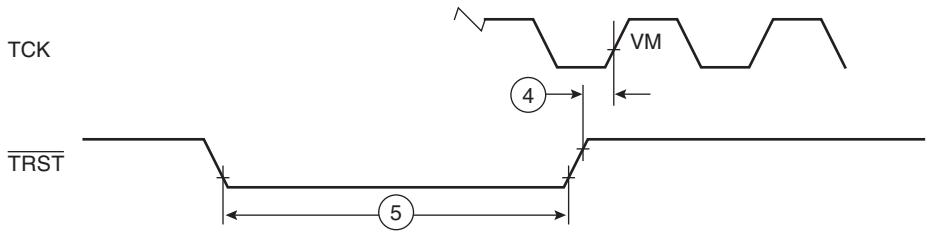
Notes: 1. $\overline{TRST}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 11-5. Clock Input Timing Diagram



VM = Midpoint Voltage (1.4V)

Figure 11-6. $\overline{TRST}$ Timing Diagram



Having access to privilege instructions, registers, and other resources allows the operating system to control the application environment (providing virtual memory and protecting operating system and critical machine resources). Instructions that control the state of the processor, the address translation mechanism, and supervisor registers can be executed only when the processor is operating in supervisor mode.

The following sections summarize the PowerPC registers that are implemented in the 603R.

12.1.1 General-purpose Registers (GPRs)

The PowerPC architecture defines 32 user-level, General-purpose Registers (GPRs). These registers are either 32 bits wide in 32-bit PowerPC microprocessors or 64 bits wide in 64-bit PowerPC microprocessors. The GPRs serve as the data source or destination for all integer instructions.

12.1.2 Floating-point Registers (FPRs)

The PowerPC architecture also defines 32 user-level, 64-bit Floating-point Registers (FPRs). The FPRs serve as the data source or destination for floating-point instructions. These registers can contain data objects of either single- or double-precision floating-point formats.

12.1.3 Condition Register (CR)

The CR is a 32-bit user-level register that consists of eight four-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

12.1.4 Floating-Point Status and Control Register (FPSCR)

The Floating-point Status and Control Register (FPSCR) is a user-level register that contains all exception signal bits, exception summary bits, exception enable bits, and rounding control bits needed for compliance with the IEEE 754 standard.

12.1.5 Machine State Register (MSR)

The Machine State Register (MSR) is a supervisor-level register that defines the state of the processor. The contents of this register are saved when an exception is taken and restored when the exception handling is completed. The 603R implements the MSR as a 32-bit register, 64-bit PowerPC processors implement a 64-bit MSR.

12.1.6 Segment Registers (SRs)

For memory management, 32-bit PowerPC microprocessors implement sixteen 32-bit Segment Registers (SRs). To speed access, the 603R implements the segment registers as two arrays; a main array (for data memory accesses) and a shadow array (for instruction memory accesses). Loading a segment entry with the Move to Segment Register (STSR) instruction loads both arrays.

– The Time Base register (TB) is a 64-bit register that maintains the time of day and operates interval timers. The TB consists of two 32-bit fields - Time Base Upper (TBU) and Time Base Lower (TBL).

– The Processor Version Register (PVR) is a 32-bit, read-only register that identifies the version (model) and revision level of the PowerPC processor.

– Block Address Translation (BAT) arrays - The PowerPC architecture defines 16 BAT registers, divided into four pairs of Data BATs (DBATs) and four pairs of instruction BATs (IBATs). See Figure 12-1 for a list of the SPR numbers for the BAT arrays.

The following supervisor-level SPRs are implementation-specific to the 603R:

– The DMISS and IMISS registers are read-only registers that are loaded automatically upon an instruction or data TLB miss.

– The HASH1 and HASH2 registers contain the physical addresses of the primary and secondary Page Table Entry Groups (PTEGs).

– The ICMP and DCMP registers contain a duplicate of the first word in the Page Table Entry (PTE) for which the table search is looking.

– The Required Physical Address (RPA) register is loaded by the processor with the second word of the correct PTE during a page table search.

– The hardware implementation (HID0 and HID1) registers provide the means for enabling the 603R's checkstops and features, and allows software to read the configuration of the PLL configuration signals.

– The Instruction Address Breakpoint Register (IABR) is loaded with an instruction address that is compared to instruction addresses in the dispatch queue. When an address match occurs, an instruction address breakpoint exception is generated.

Figure 12-1 shows all the 603R registers available at the user and supervisor level. The number to the right of the SPRs indicate the number that is used in the syntax of the instruction operands to access the register.

- **Memory Control Instructions** – these instructions provide control of caches, TLBs, and segment registers
  - Supervisor-level cache management instructions
  - User-level cache instructions
  - Segment register manipulation instructions
  - Translation lookaside buffer management instructions

Note that this grouping of the instructions does not indicate which execution unit executes a particular instruction or group of instructions.

Integer instructions operate on byte, half-word, and word operands. Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands. The PowerPC architecture uses instructions that are four bytes long and word-aligned. It provides for byte, half-word, and word operand loads and stores between the memory and a set of 32 GPRs. It also provides for word and double-word operand loads and stores between the memory and a set of 32 Floating-point Registers (FPRs).

Computational instructions do not modify the memory. To use a memory operand in a computation and then modify the same or another memory location, the memory contents must be loaded into a register, modified, and then written back to the target location with distinct instructions.

PowerPC processors follow the program flow when they are in the normal execution state. However, the flow of instructions can be interrupted directly by the execution of an instruction or by an asynchronous event. Either kind of exception may cause one of several components of the system software to be invoked.

- Calculating Effective Address

  The Effective Address (EA) is the 32-bit address computed by the processor when executing a memory access or branch instruction or when fetching the next sequential instruction.

  The PowerPC architecture supports two simple memory addressing modes:

  - EA = (RA|0) + offset (including offset = 0) (register indirect with immediate index)
  - EA = (RA|0) + rB (register indirect with index)

These simple addressing modes allow efficient address generation for memory accesses. Calculation of the effective address for aligned transfers occurs in a single clock cycle.

For a memory access instruction, if the sum of the effective address and the operand length exceeds the maximum effective address, the memory operand is considered to wrap around from the maximum effective address to effective address 0.

Effective address computations for both data and instruction accesses use 32-bit unsigned binary arithmetic. A carry over from bit 0 is ignored in 32-bit implementations.

Table 12-2. Exceptions and Conditions (Continued)

Exception Type	Vector Offset (hex)	Causing Conditions
Program	00700	A program exception is caused by one of the following exception conditions, which correspond to bit settings in SRR1 and arise during execution of an instruction: • Floating-point enabled exception – A floating-point enabled exception condition is generated when the following condition is met: (MSR[FE0] | MSR[FE1]) & FPSCR[FEX] is 1 FPSER[FEX] is set by the execution of a floating-point instruction that causes an enabled exception or by the execution of one of the "move to FPSCR" instructions that results in both an exception condition bit and its corresponding enable bit being set in the FPSCR • Illegal instruction – an illegal instruction program exception is generated when execution of an instruction is attempted with an illegal opcode or illegal combination of opcode and extended opcode fields (including PowerPC instructions not implemented in the 603e), or when execution of an optional instruction not provided in the 603e is attempted (these do not include those optional instructions that are treated as no-ops) • Privileged instruction – a privileged instruction type program exception is generated when the execution of a privileged instruction is attempted and the MSR register user privilege bit, MSR[PR], is set. In the 603e, this exception is generated for **mtspr** or **mfspr** with an invalid SPR field if SPR[0] = 1 and MSR[PR] = 1. This may not be true for all PowerPC processors • Trap – a trap type program exception is generated when any of the conditions specified in a trap instruction is met
Floating-point unavailable	00800	A floating-point unavailable exception is caused by an attempt to execute a floating-point instruction (including floating-point load, store, and more instructions) when the floating-point available bit is disabled, (MSR[FP] = 0)
Decrementer	00900	The decrementer exception occurs when the most significant bit of the decrementer (DEC) register transitions from 0 to 1. Must also be enabled with the MSR[EE] bit
Reserved	00A00–00BFF	–
System call	00C00	A system call exception occurs when a System Call (sc) instruction is executed
Trace	00D00	A trace execution is taken when MSR[SE] = 1 or when the currently completing instruction is a branch and MSR[BE] = 1
Reserved	00E00	The 603e does not generate an exception to this vector. Other PowerPC processors may use this vector for floating-point assist exceptions
Reserved	00E10–00FFF	–
Instruction translation miss	01000	An instruction translation miss exception is caused when an effective address for an instruction fetch cannot be translated by the ITLB
Data load translation miss	01100	A data load translation miss exception is caused when an effective address for a data load operation cannot be translated by the DTLB
Data store translation miss	01200	A data store translation miss exception is caused when an effective address for a data store operation cannot be translated by the DTLB; or where a DTLB hit occurs, and the change bit in the PTE must be set due to a data store operation

In Table 13-1, the horizontal scale represents the bus frequency (SYSCLK) and the vertical scale represents the PLL-CFG[0-3] signals.

For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation.

Table 13-1. CPU Frequencies for Common Bus Frequencies and Multipliers

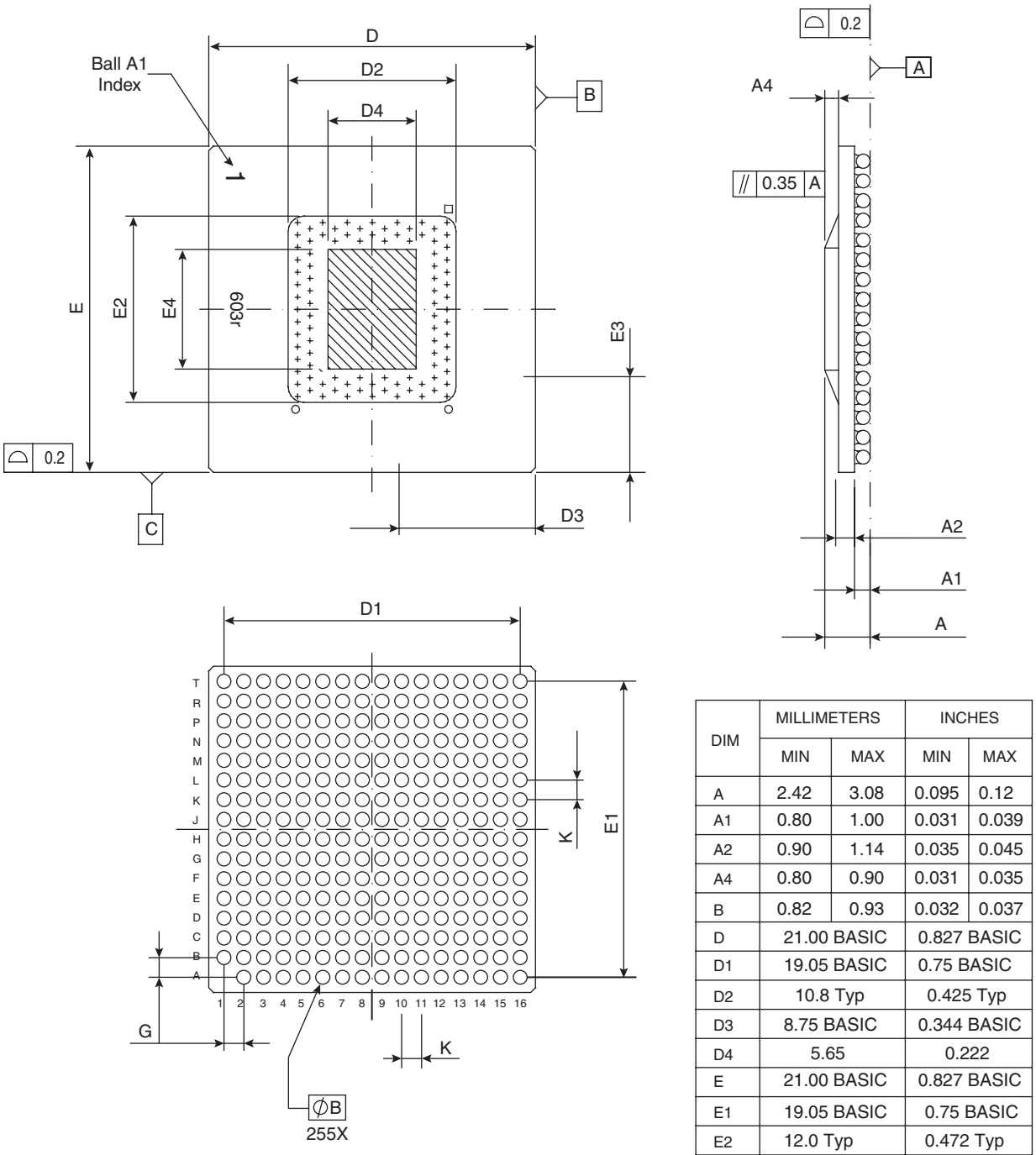
PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CBGA 255, HiTCE CBGA 255 and CI-CGA 255								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz	Bus 75 MHz
0100	2x	2x	-	-	-	-	-	-	150 (300)
0101	2x	4x	-	-	-	-	-	-	-
0110	2.5x	2x	-	-	-	-	150 (300)	166 (333)	187 (375)
1000	3x	2x	-	-	-	150 (300)	180 (360)	200 (400)	225 (450)
1110	3.5x	2x	-	-	-	175 (350)	210 (420)	233 (466)	263 (525)
1010	4x	2x	-	-	160 (320)	200 (400)	240 (480)	267 (533)	300 (600)
0111	4.5x	2x	-	150 (300)	180 (360)	225 (450)	270 (540)	300 (600)	-
1011	5x	2x	-	166 (333)	200 (400)	250 (500)	300 (600)	-	-
1001	5.5x	2x	-	183 (366)	220 (440)	275 (550)	-	-	-
1101	6x	2x	150 (300)	200 (400)	240 (480)	300 (600)	-	-	-
0011	PLL bypass								
1111	Clock off								

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz
0100	2x	2x	–	–	–	–	–	–
0101	2x	4x	–	–	–	–	–	–
0110	2.5x	2x	–	–	–	–	150 (300)	166 (333)
1000	3x	2x	–	–	–	150 (300)	180 (360)	200 (400)
1110	3.5x	2x	–	–	–	175 (350)	–	–

15.1.1 Mechanical Dimensions of the HiTCE CBGA Package

Figure 15-1 provides the mechanical dimensions and bottom surface nomenclature of the HiTCE CBGA package.

Figure 15-1. Mechanical Dimensions of the HiTCE CBGA Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.42	3.08	0.095	0.12
A1	0.80	1.00	0.031	0.039
A2	0.90	1.14	0.035	0.045
A4	0.80	0.90	0.031	0.035
B	0.82	0.93	0.032	0.037
D	21.00 BASIC		0.827 BASIC	
D1	19.05 BASIC		0.75 BASIC	
D2	10.8 Typ		0.425 Typ	
D3	8.75 BASIC		0.344 BASIC	
D4	5.65		0.222	
E	21.00 BASIC		0.827 BASIC	
E1	19.05 BASIC		0.75 BASIC	
E2	12.0 Typ		0.472 Typ	
E3	6.15 BASIC		0.242 BASIC	
E4	7.7		0.303	
G, K	1.27 BASIC		0.05 BASIC	

15.3 CI-CGA Package Parameters

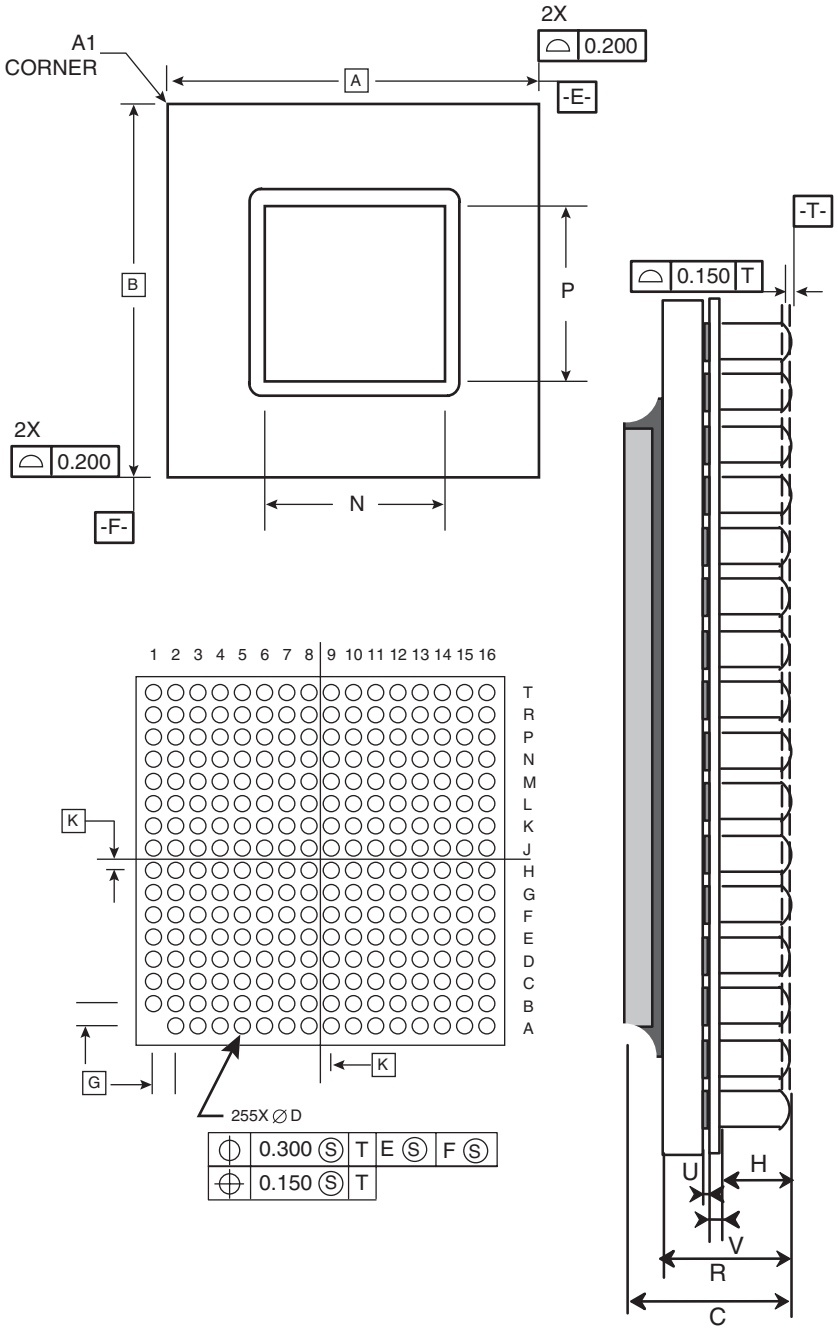
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead ceramic ball grid array (CI-CGA).

Package outline	21 mm × 21 mm
Interconnects	255
Pitch	1.27 mm
Typical module height	3.84 mm

15.3.1 Mechanical Dimensions of the CI-CGA Package

Figure 15-3 provides the mechanical dimensions and bottom surface nomenclature of the CI-CGA package.

Figure 15-3. Mechanical Dimensions and Bottom Surface Nomenclature of the CI-CGA Package

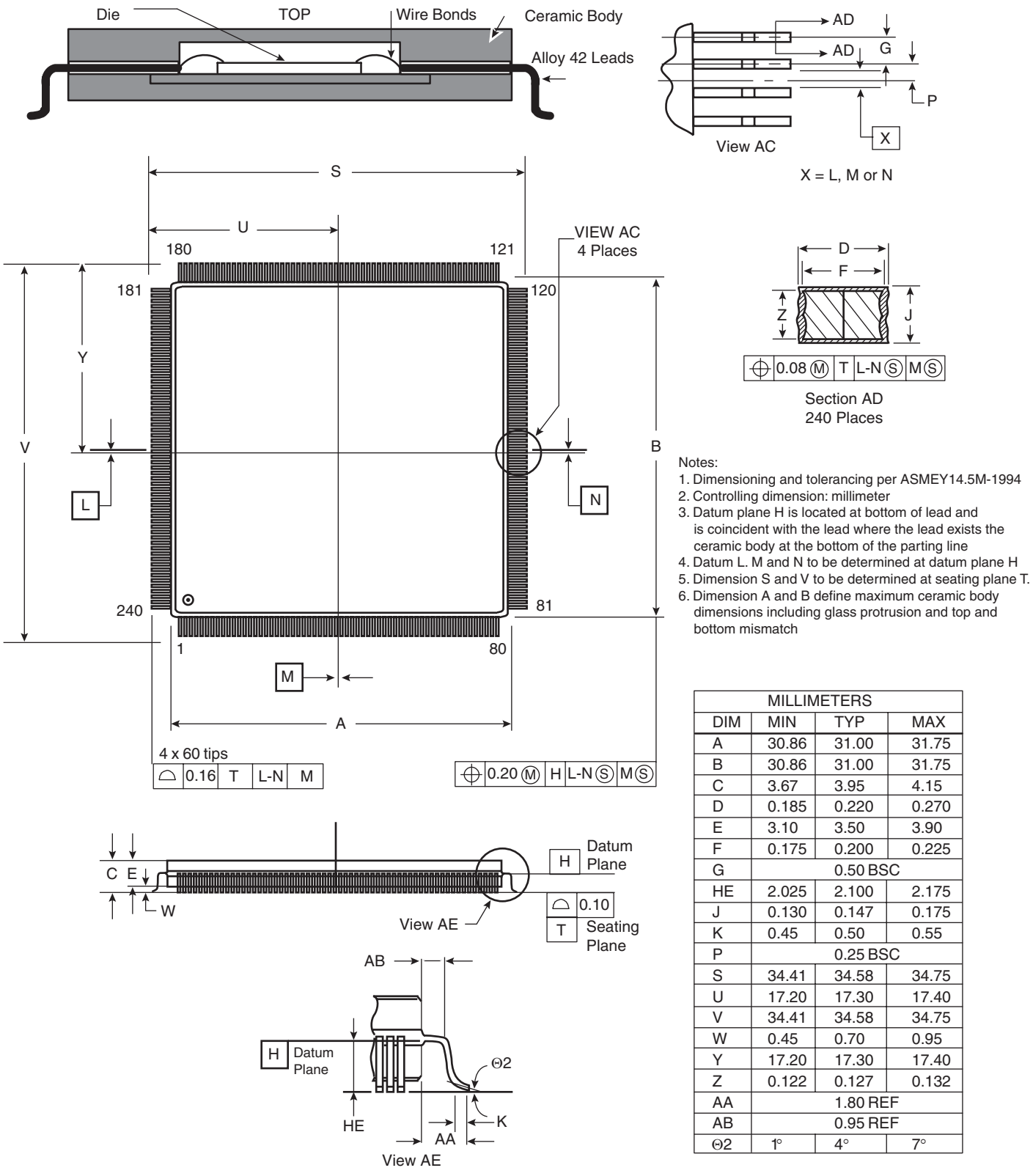


Notes: 1. Dimensioning and tolerancing per ASME Y14.5M—1994
2. Controlling dimension: millimeter

Dim	Millimeters	
	Min	Max
A	21.000 BSC	
B	21.000 BSC	
C	3.84 BSC	
D	0.790	0.990
G	1.270 BSC	
H	1.545	1.695
K	0.635 BSC	
N	5.000	
P	7.000	
R	3.02 BSC	
U	0.10 BSC	
V	0.25	0.35

15.4 CERQUAD 240 Package

Figure 15-4. Mechanical Dimensions of the Wire-bond CERQUAD Package

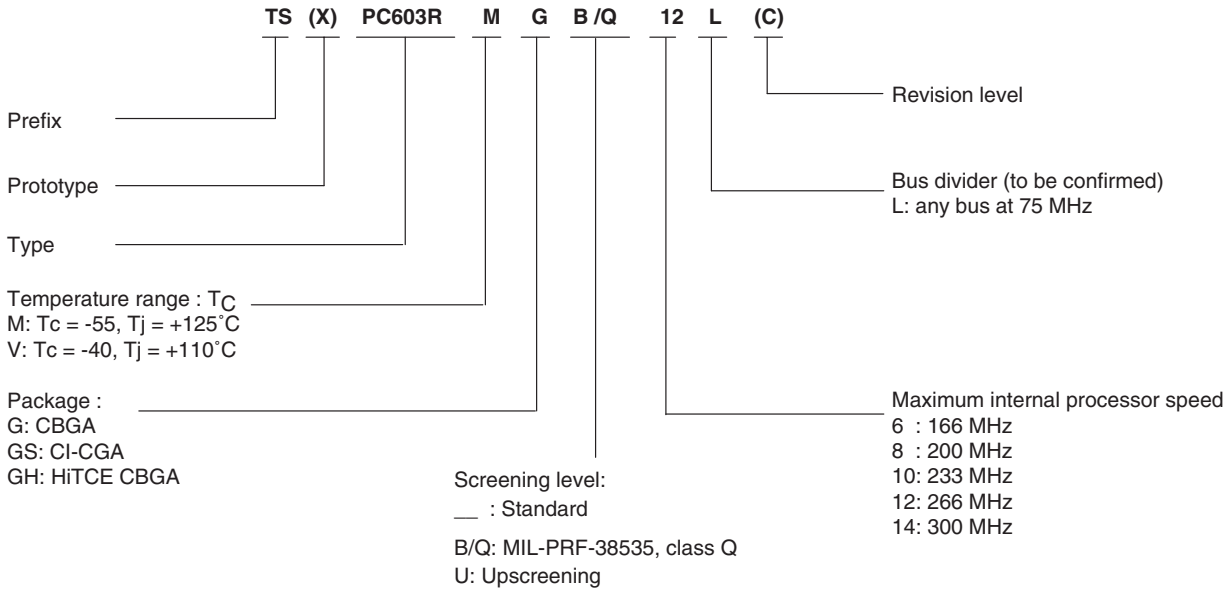


Notes:
1. Dimensioning and tolerancing per ASMEY14.5M-1994
2. Controlling dimension: millimeter
3. Datum plane H is located at bottom of lead and is coincident with the lead where the lead exists the ceramic body at the bottom of the parting line
4. Datum L. M and N to be determined at datum plane H
5. Dimension S and V to be determined at seating plane T.
6. Dimension A and B define maximum ceramic body dimensions including glass protrusion and top and bottom mismatch

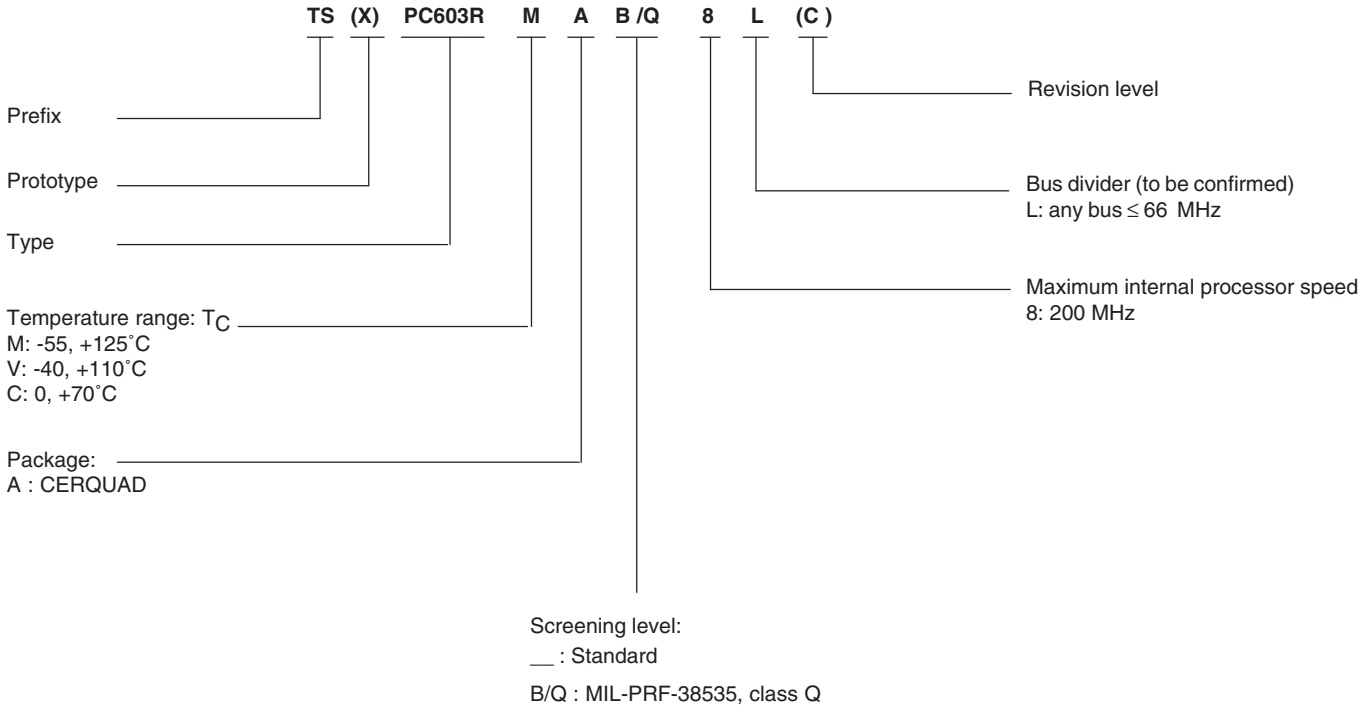
MILLIMETERS			
DIM	MIN	TYP	MAX
A	30.86	31.00	31.75
B	30.86	31.00	31.75
C	3.67	3.95	4.15
D	0.185	0.220	0.270
E	3.10	3.50	3.90
F	0.175	0.200	0.225
G		0.50 BSC	
HE	2.025	2.100	2.175
J	0.130	0.147	0.175
K	0.45	0.50	0.55
P		0.25 BSC	
S	34.41	34.58	34.75
U	17.20	17.30	17.40
V	34.41	34.58	34.75
W	0.45	0.70	0.95
Y	17.20	17.30	17.40
Z	0.122	0.127	0.132
AA		1.80 REF	
AB		0.95 REF	
Θ2	1°	4°	7°

16. Ordering Information

16.1 Ordering Information of the CBGA, CI-CGA and HiTCE Packages



16.2 Ordering Information of the CERQUAD 240 Package



Note: For availability of the different versions, contact your Atmel sales office.

17. Definitions

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with the customer and application validation	Before design phase
Target specification	This datasheet contains target or goal specifications for product development	Valid during the design phase
Preliminary specification α site	This datasheet contains preliminary data. Additional data may be published at a later date and could include simulation results	Valid before characterization phase
Preliminary specification β site	This datasheet also contains characterization results	Valid before the industrialization phase
Product specification	This datasheet contains final product specifications	Valid for production purpose
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stresses above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification		

17.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

18. Document Revision History

Table 18-1 provides a revision history for this hardware specification.

Table 18-1. Document Revision History

Revision Number	Date	Substantive Change(s)
B	07/2005	Added HiTCE package for PowerPC 603R
A	10/2004	This document is a merge of TSPC603R in CBGA255/CI-CGA 255 package (ref 2125B) and TSPC603R in Cerquad package (ref 2127A)