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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	255-BCBGA Exposed Pad
Supplier Device Package	255-HiTCE-CBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgh8lc

- a Load/Store Unit (LSU)
- a System Register Unit (SRU)

The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603R-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603R provides independent on-chip, 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data, as well as on-chip instruction and data Memory Management Units (MMUs). The MMUs contain 64-entry, two-way set-associative, Data and Instruction Translation Lookaside Buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a Least Recently Used (LRU) replacement algorithm. The 603R also supports block address translation through the use of two independent Instruction and Data Block Address Translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation has priority.

The 603R has a selectable 32- or 64-bit data bus and a 32-bit address bus. The 603R interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603R provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (Modified/Exclusive/Shared/Invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603R supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/Os.

The 603R uses an advanced, 0.29 µm 5-metal-layer CMOS process technology and maintains full interface compatibility with TTL devices.

5. Signal Description

Figure 5-1 on page 5, Table 10-5 and Table 10-6 on page 20 describe the signals on the TSPC603R and indicate signal functions. The test signals, $\overline{\text{TRST}}$, TMS, TCK, TDI and TDO, comply with the subset P-1149.1 of the IEEE testability bus standard.

The three signals $\overline{\text{LSSD\_MODE}}$, LI_TSTCLK and L2_TSTCLK are test signals for factory use only and must be pulled up to V_{DD} for normal machine operations.

8. Thermal Characteristics

8.1 CBGA 255 and CI-CGA 255 Packages

The data found in this section concerns 603R devices packaged in the 255-lead 21 mm multi-layer ceramic (MLC) and ceramic BGA package. Data is included for use with a Thermalloy #2328B heat sink.

The internal thermal resistance for this package is negligible due to the exposed die design. A thermal interface material is recommended at the package lid to heat sink interface to minimize the thermal contact resistance.

Additionally, the CBGA package offers an excellent thermal connection to the card and power planes. Heat generated at the chip is dissipated through the package, the heat sink (when used) and the card. The parallel heat flow paths result in the lowest overall thermal resistance as well as offer significantly better power dissipation capability if a heat sink is not used.

The thermal characteristics for the flip-chip CBGA and CI-CGA packages are as follows:

Thermal resistance (junction-to-case) = R_{jc} or
θ_{jc} = 0.095°C/Watt for the 2 packages.

Thermal resistance (junction-to-ball) = R_{jb} or
θ_{jb} = 3.5°C/Watt for the CBGA package.

Thermal resistance (junction-to-bottom SCI) = R_{js} or
θ_{js} = 3.7°C/Watt for the CI-CGA package.

The junction temperature can be calculated from the junction to ambient thermal resistance, as follow:

Junction temperature:

$$T_j = T_a + (R_{jc} + R_{cs} + R_{sa}) \times P$$

where: T_a is the ambient temperature in the vicinity of the device

R_{jc} is the die junction to case thermal resistance of the device

R_{cs} is the case to heat sink thermal resistance of the interface material

R_{sa} is the heat sink to ambient thermal resistance

P is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained at a lower value than the value specified in ”Recommended Operating Conditions” on page 6.

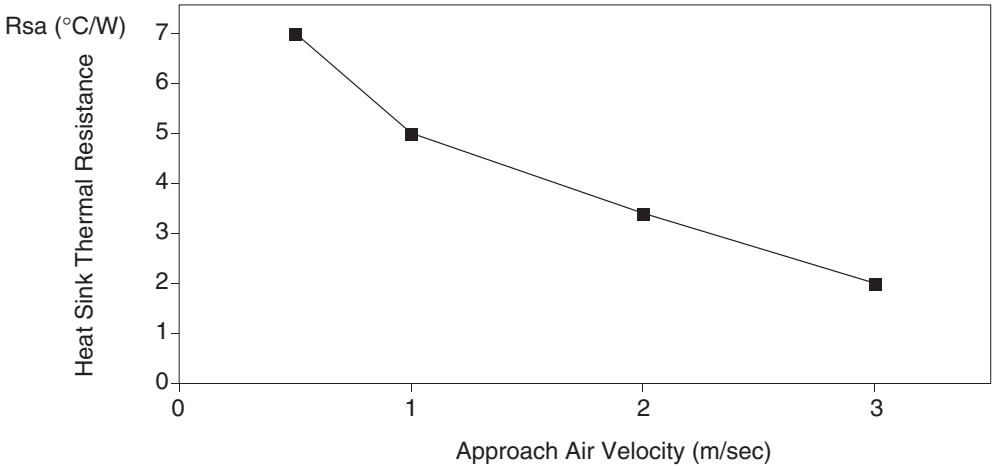
The thermal resistance of the thermal interface material (R_{cs}) is typically about 1°C/Watt.

Assuming a T_a of 85°C and a consumption (P) of 3.6 Watts, the junction temperature of the device would be as follow:

T_j = 85°C + (0.095°C/Watt + 1°C/Watt + R_{sa}) × 3.5 Watts.

For the Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (R_{sa}) versus airflow velocity is shown in Figure 8-1.

Figure 8-1. CBGA Thermal Management Example



Assuming an air velocity of 1 m/sec, the associated overall thermal resistance and junction temperature, found in Table 8-1 will result.

Table 8-1. Thermal Resistance and Junction Temperature

Configuration	R_{ja} (°C/W)	T_j (°C)
With 2328B heat sink	5	106

Vendors such as Aavid, Thermalloy®, and Wakefield Engineering can supply heat sinks with a wide range of thermal performance.

8.2 HiTCE CBGA Package

Table 8-2. HiTCE CBGA Package

Characteristic	Symbol	Value	Unit
Junction-to-bottom of balls(1)	$R\theta_J$	7.5	°C/W
Junction-to-ambient thermal resistance natural convection, four-layer (2s2p) board	$R\theta_{JMA}$	22.4(2)	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.7(3)	°C/W

Notes: 1. Simulation, no convection air flow.
2. Per JEDEC JESD51-2 with the board horizontal.
3. Per JEDEC JESD51-8 with the board horizontal.

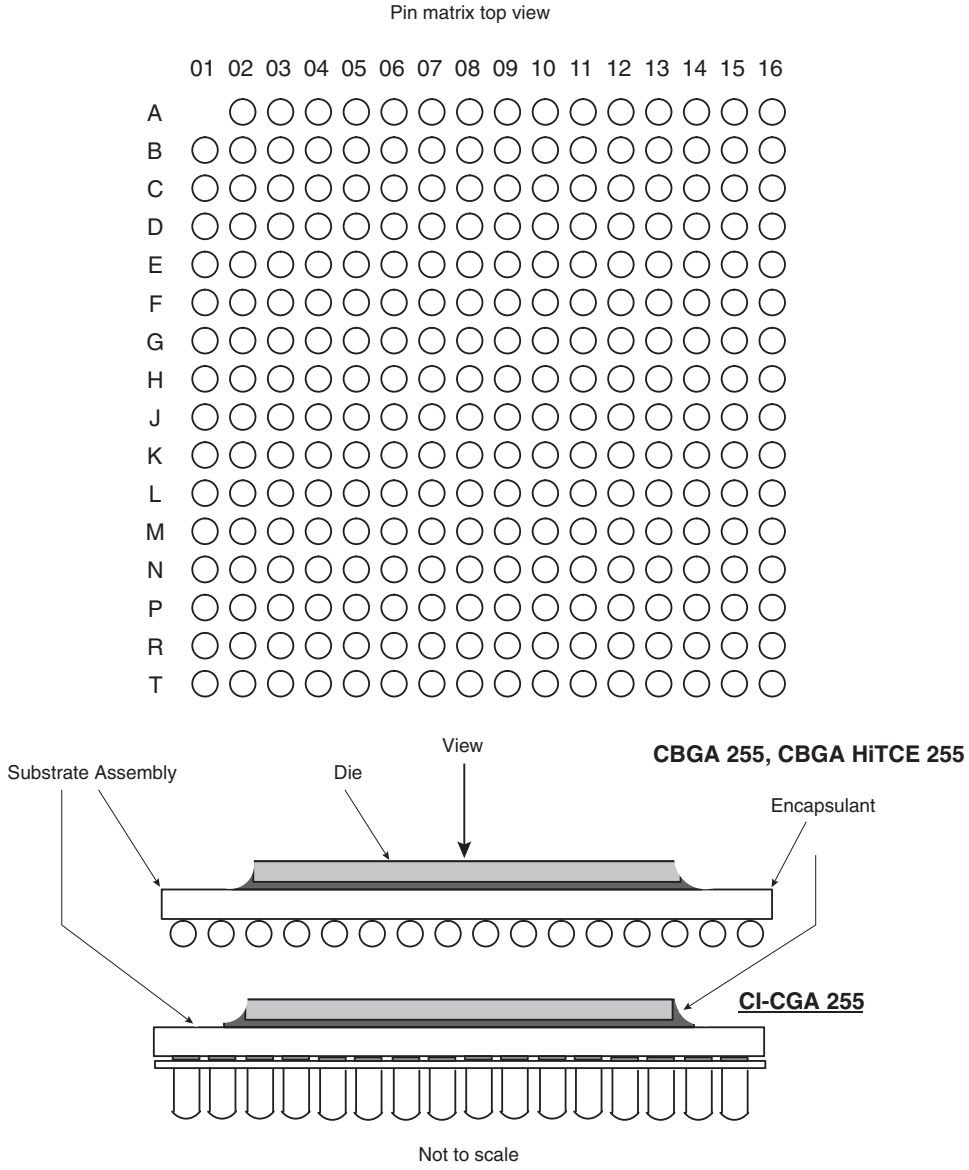
8.3 CERQUAD 240 Package

This section provides thermal management data for the 603R. This information is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, wire-bond CERQUAD package with the cavity up (the silicon die is attached to the bottom of the package). This configuration enables dissipation through the PCB.

The thermal characteristics for a wire-bond CERQUAD package are as follows:

- Thermal resistance (junction to bottom of the case) (typical) = $R_{\theta jc}$ or θ_{jc} = 2.5°C/Watt
- Thermal resistance (junction to top of the case) is typically 16°C/W

Figure 10-1. CBGA 255, HiTCE CBGA 255 and CI–CGA 255 Top View



10.1.1 Pinout Listing

Table 10-1. Power and Ground Pins

	CBGA, HiTCE CBGA and CI-CGA Pin Number	
	V_{DD}	**GND**
PLL (AV_{DD})	A10	
Internal Logic[1] (V_{DD})	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12
I/O Drivers[1] (OV_{DD})	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	

Notes: 1. OV_{DD} inputs apply power to the I/O drivers and V_{DD} inputs supply power to the processor core.

Table 10-2. Signal Pinout Listing

Signal Name	CBGA, HiTCE CBGA and CI-CGA Pin Number	Active	I/O
A[0-31]	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, G02, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP[0-3]	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
$\overline{\text{ARTRY}}$	J04	Low	I/O
$\overline{\text{BG}}$	L01	Low	Input
$\overline{\text{BR}}$	B06	Low	Output
$\overline{\text{CI}}$	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	A06	Low	Output
CLK_OUT	D07	-	Output
CSE[0-1]	B01, B05	High	Output
$\overline{\text{DBB}}$	J14	Low	I/O
$\overline{\text{DBG}}$	N01	Low	Input
$\overline{\text{DBDIS}}$	H15	Low	Input
$\overline{\text{DBWO}}$	G04	Low	Input
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP[0-7]	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	A05	Low	Output
$\overline{\text{DRTRY}}$	G16	Low	Input

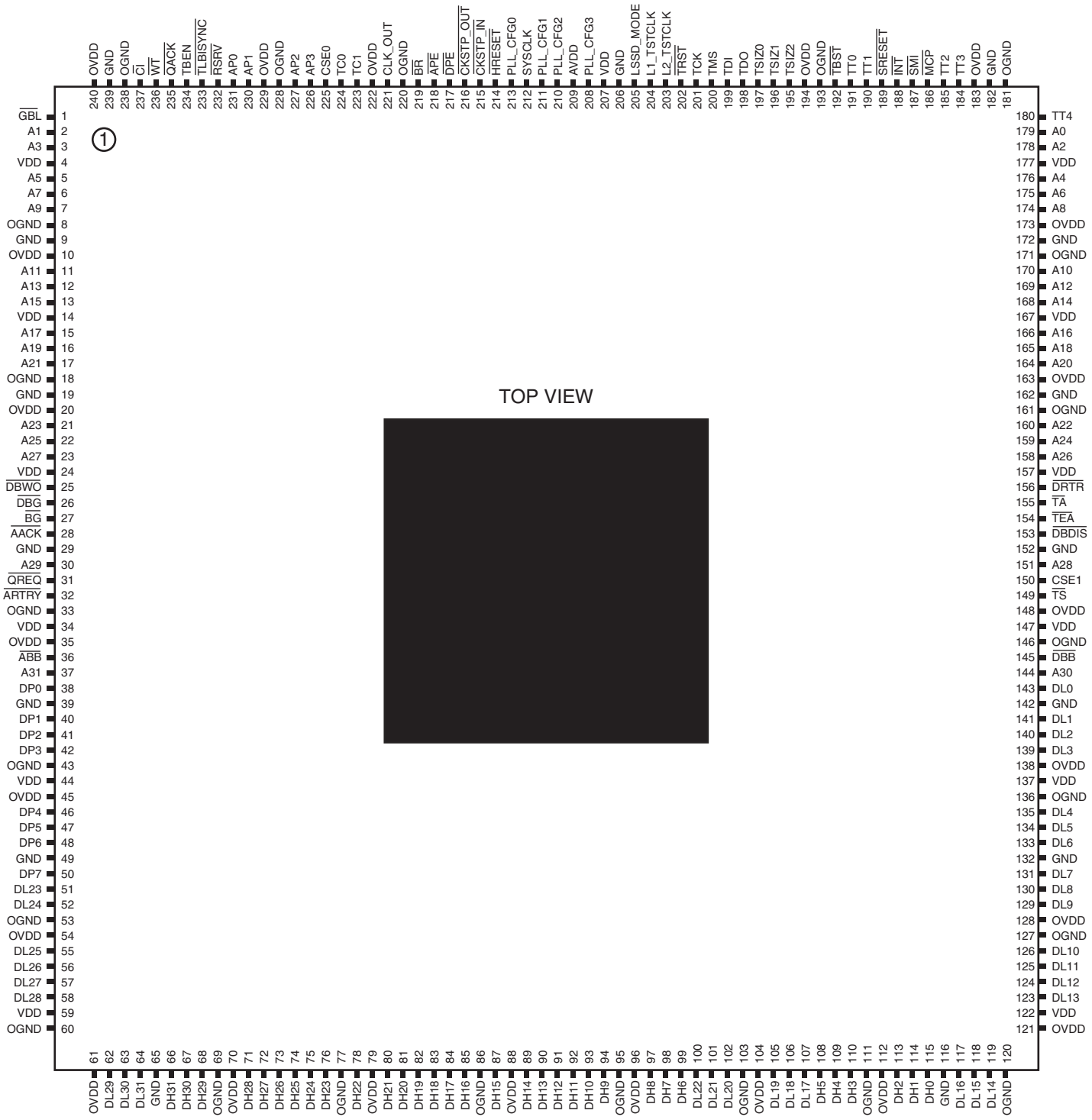
Table 10-2. Signal Pinout Listing (Continued)

Signal Name	CBGA, HiTCE CBGA and CI-CGA Pin Number	Active	I/O
$\overline{\text{GBL}}$	F01	Low	I/O
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TSTCLK(1)	D11	-	Input
L2_TSTCLK(1)	D12	-	Input
$\overline{\text{LSSD\_MODE}}$(1)	B10	Low	Input
$\overline{\text{MCP}}$	C13	Low	Input
PLL_CFG[0-3]	A08, B09, A09, D09	High	Input
$\overline{\text{QACK}}$	D03	Low	Input
$\overline{\text{QREQ}}$	J03	Low	Output
$\overline{\text{RSRV}}$	D01	Low	Output
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	-	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC[0-1]	A02, A03	High	Output
TCK	C11	-	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
$\overline{\text{TLBISYNC}}$	C04	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ[0-2]	A13, D10, B12	High	I/O
TT[0-4]	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
NC	B07, B08, C03, C06, C08, D05, D06, F03, H04, J16	Low	Input
VOLTDETGND(2)	F03	Low	Output

Notes: 1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. NC (not connected) in the 603e BGA package; internally tied to GND in the 603R BGA package to indicate to the power supply that a low-voltage processor is present.

10.2 CERQUAD 240 Package

Figure 10-2. CERQUAD 240: Top View



10.2.1 Pinout Listing

Table 10-3. Power and Ground Pins

	CERQUAD Pin Number	
	VCC	**GND**
PLL (AV_{DD})	209	
Internal Logic	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239
Output Drivers	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238

Table 10-4. Signal Pinout Listing

Signal Name	CERQUAD Pin Number
A[0-31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37
$\overline{\text{AACK}}$	28
$\overline{\text{ABB}}$	36
AP[0-3]	231,230,227,226
$\overline{\text{APE}}$	218
$\overline{\text{ARTRY}}$	32
$\overline{\text{BG}}$	27
$\overline{\text{BR}}$	219
$\overline{\text{CI}}$	237
$\overline{\text{CKSTP\_IN}}$	215
$\overline{\text{CKSTP\_OUT}}$	216
CLK_OUT	221
CSE[0-1]	225,150
$\overline{\text{DBB}}$	145
$\overline{\text{DBG}}$	26
$\overline{\text{DBDIS}}$	153
$\overline{\text{DBWO}}$	25
DH[0-31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66
DL[0-31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64
DP[0-7]	38, 40, 41, 42, 46, 47, 48, 50
$\overline{\text{DPE}}$	217
$\overline{\text{DRTRY}}$	156
$\overline{\text{GBL}}$	1
$\overline{\text{HRESET}}$	214

3. Leakage currents are measured for nominal OV_{DD} and V_{DD} or both OV_{DD} and V_{DD}. Same variation (for example, both V_{DD} and OV_{DD} vary by either +5% or -5%)

11.3 Dynamic Characteristics

11.3.1 Clock AC Specifications

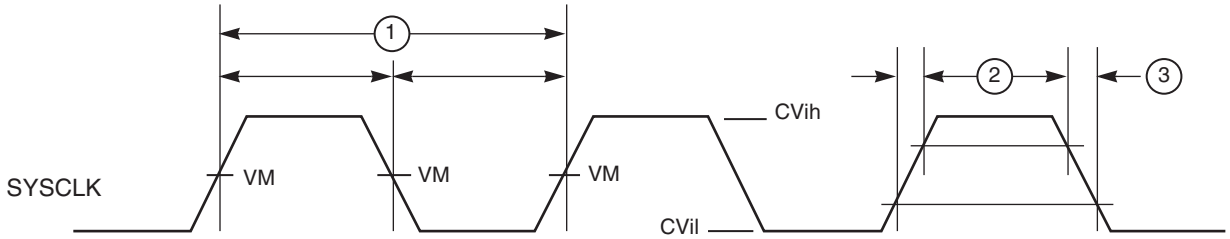
Table 11-2 provides the clock AC timing specifications as defined in Figure 11-1.

Table 11-2. Clock AC Timing Specifications[1][2][3][4] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Figure Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and CERQUAD				CBGA 255, HiTCE CBGA 255 and CI-CGA 255							
		166 MHz		200 MHz		233 MHz		266 MHz		300 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
	Processor Frequency	150	166	150	200	180	233	180	266	180	300	MHz	[5]
	VCO Frequency	300	332	300	400	360	466	360	532	360	600	MHz	[5]
	SYSCLK (bus) Frequency	25	66.7	33.3	66.7	33.3	75	33.3	75	33.3	75	MHz	[5]
1	SYSCLK Cycle Time	15	30	13.3	30	13.3	30	13.3	30	13.3	30	ns	
2,3	SYSCLK Rise and Fall Time	–	2	–	2	–	2	–	2	–	2	ns	[1]
4	SYSCLK Duty Cycle (1.4V measured)	40	60	40	60	40	60	40	60	40	60	%	[3]
	SYSCLK Jitter	–	±150	–	±150	–	±150	–	±150	–	±150	ps	[2]
	603R Internal PLL Relock Time	–	100	–	100	–	100	–	100	–	100	µs	[3][4]

Notes:
1. Rise and fall times for the SYSCLK input are measured from 0.4V to 2.4V.
2. Cycle-to-cycle jitter is guaranteed by design.
3. Timing is guaranteed by design and characterization and is not tested.
4. The PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD}, OV_{DD}, AV_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen so that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description for valid PLL_CFG[0-3] settings.

Figure 11-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage (1.4V)

11.3.2 Input AC Specifications

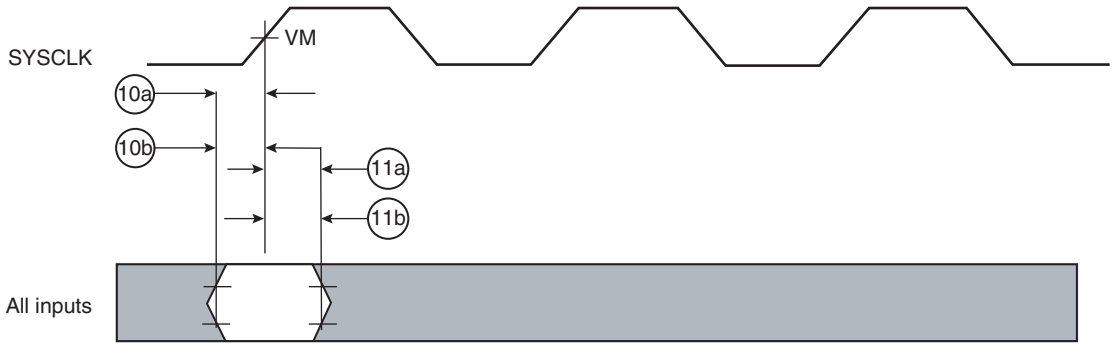
Table 11-3 provides the input AC timing specifications for the 603R as defined in Figure 11-2 and Figure 11-3.

Table 11-3. Input AC Timing Specifications[1] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Figure Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages		CBGA 255, HiTCE CBGA 255 and CI-CGA 255				Unit	Note
		166, 200 MHz		233, 266 MHz		300 MHz			
		Min	Max	Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	2.5	–	2.5	–	2.5	–	ns	(2)
10b	All other inputs valid to SYSCLK (input setup)	4	–	3.5	–	3.5	–	ns	(3)
10c	Mode select inputs valid to $\overline{HRESET}$ (input setup) (for $\overline{DRTRY}$, $\overline{QACK}$ and $\overline{TLBISYNC}$)	8	–	8	–	8	–	t_{sysclk}	(4)(5)(6)(7)
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1	–	1	–	1	–	ns	(2)
11b	SYSCLK to all other inputs invalid (input hold)	1	–	1	–	1	–	ns	(3)
11c	$\overline{HRESET}$ to mode select inputs invalid (input hold) (for $\overline{DRTRY}$, $\overline{QACK}$, and $\overline{TLBISYNC}$)	0	–	0	–	0	–	ns	(4)(6)(7)

Notes:
1. All input specifications are measured from the TTL level (0.8 or 2V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 11-3.
2. Address/data/transfer attribute input signals are composed of the following: A[0-31], AP[0-3], TT[0-4], TC[0-1], $\overline{TBST}$, TSIZ[0-2], $\overline{GBL}$, DH[0-31], DL[0-31], DP[9-7].
3. All other input signals are composed of the following: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{AACK}$, $\overline{DBG}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{DRTRY}$, $\overline{TEA}$, $\overline{DBDIS}$, $\overline{HRESET}$, $\overline{SRESET}$, $\overline{INT}$, $\overline{SMI}$, $\overline{MCP}$, TBEN, $\overline{QACK}$, $\overline{TLBISYNC}$.
4. The setup and hold time is with respect to the rising edge of $\overline{HRESET}$. See Figure 11-3.
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode only. Also note that $\overline{HRESET}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.

Figure 11-2. Input Timing Diagram



VM = Midpoint Voltage (1.4V)

Having access to privilege instructions, registers, and other resources allows the operating system to control the application environment (providing virtual memory and protecting operating system and critical machine resources). Instructions that control the state of the processor, the address translation mechanism, and supervisor registers can be executed only when the processor is operating in supervisor mode.

The following sections summarize the PowerPC registers that are implemented in the 603R.

12.1.1 General-purpose Registers (GPRs)

The PowerPC architecture defines 32 user-level, General-purpose Registers (GPRs). These registers are either 32 bits wide in 32-bit PowerPC microprocessors or 64 bits wide in 64-bit PowerPC microprocessors. The GPRs serve as the data source or destination for all integer instructions.

12.1.2 Floating-point Registers (FPRs)

The PowerPC architecture also defines 32 user-level, 64-bit Floating-point Registers (FPRs). The FPRs serve as the data source or destination for floating-point instructions. These registers can contain data objects of either single- or double-precision floating-point formats.

12.1.3 Condition Register (CR)

The CR is a 32-bit user-level register that consists of eight four-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

12.1.4 Floating-Point Status and Control Register (FPSCR)

The Floating-point Status and Control Register (FPSCR) is a user-level register that contains all exception signal bits, exception summary bits, exception enable bits, and rounding control bits needed for compliance with the IEEE 754 standard.

12.1.5 Machine State Register (MSR)

The Machine State Register (MSR) is a supervisor-level register that defines the state of the processor. The contents of this register are saved when an exception is taken and restored when the exception handling is completed. The 603R implements the MSR as a 32-bit register, 64-bit PowerPC processors implement a 64-bit MSR.

12.1.6 Segment Registers (SRs)

For memory management, 32-bit PowerPC microprocessors implement sixteen 32-bit Segment Registers (SRs). To speed access, the 603R implements the segment registers as two arrays; a main array (for data memory accesses) and a shadow array (for instruction memory accesses). Loading a segment entry with the Move to Segment Register (STSR) instruction loads both arrays.

– The Time Base register (TB) is a 64-bit register that maintains the time of day and operates interval timers. The TB consists of two 32-bit fields - Time Base Upper (TBU) and Time Base Lower (TBL).

– The Processor Version Register (PVR) is a 32-bit, read-only register that identifies the version (model) and revision level of the PowerPC processor.

– Block Address Translation (BAT) arrays - The PowerPC architecture defines 16 BAT registers, divided into four pairs of Data BATs (DBATs) and four pairs of instruction BATs (IBATs). See Figure 12-1 for a list of the SPR numbers for the BAT arrays.

The following supervisor-level SPRs are implementation-specific to the 603R:

– The DMISS and IMISS registers are read-only registers that are loaded automatically upon an instruction or data TLB miss.

– The HASH1 and HASH2 registers contain the physical addresses of the primary and secondary Page Table Entry Groups (PTEGs).

– The ICMP and DCMP registers contain a duplicate of the first word in the Page Table Entry (PTE) for which the table search is looking.

– The Required Physical Address (RPA) register is loaded by the processor with the second word of the correct PTE during a page table search.

– The hardware implementation (HID0 and HID1) registers provide the means for enabling the 603R's checkstops and features, and allows software to read the configuration of the PLL configuration signals.

– The Instruction Address Breakpoint Register (IABR) is loaded with an instruction address that is compared to instruction addresses in the dispatch queue. When an address match occurs, an instruction address breakpoint exception is generated.

Figure 12-1 shows all the 603R registers available at the user and supervisor level. The number to the right of the SPRs indicate the number that is used in the syntax of the instruction operands to access the register.

- **Memory Control Instructions** – these instructions provide control of caches, TLBs, and segment registers
  - Supervisor-level cache management instructions
  - User-level cache instructions
  - Segment register manipulation instructions
  - Translation lookaside buffer management instructions

Note that this grouping of the instructions does not indicate which execution unit executes a particular instruction or group of instructions.

Integer instructions operate on byte, half-word, and word operands. Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands. The PowerPC architecture uses instructions that are four bytes long and word-aligned. It provides for byte, half-word, and word operand loads and stores between the memory and a set of 32 GPRs. It also provides for word and double-word operand loads and stores between the memory and a set of 32 Floating-point Registers (FPRs).

Computational instructions do not modify the memory. To use a memory operand in a computation and then modify the same or another memory location, the memory contents must be loaded into a register, modified, and then written back to the target location with distinct instructions.

PowerPC processors follow the program flow when they are in the normal execution state. However, the flow of instructions can be interrupted directly by the execution of an instruction or by an asynchronous event. Either kind of exception may cause one of several components of the system software to be invoked.

- Calculating Effective Address

  The Effective Address (EA) is the 32-bit address computed by the processor when executing a memory access or branch instruction or when fetching the next sequential instruction.

  The PowerPC architecture supports two simple memory addressing modes:

  - EA = (RA|0) + offset (including offset = 0) (register indirect with immediate index)
  - EA = (RA|0) + rB (register indirect with index)

These simple addressing modes allow efficient address generation for memory accesses. Calculation of the effective address for aligned transfers occurs in a single clock cycle.

For a memory access instruction, if the sum of the effective address and the operand length exceeds the maximum effective address, the memory operand is considered to wrap around from the maximum effective address to effective address 0.

Effective address computations for both data and instruction accesses use 32-bit unsigned binary arithmetic. A carry over from bit 0 is ignored in 32-bit implementations.

12.3.3 Exception Model

The following subsections describe the PowerPC exception model and the 603R implementation.

12.3.4 PowerPC Exception Model

The PowerPC exception mechanism allows the processor to change to supervisor state as a result of external singles, errors, or unusual conditions arising in the execution of instructions, and differ from the arithmetic exceptions defined by the IEEE for floating-point operations. When exceptions occur, information about the state of the processor is saved to certain registers and the processor begins execution at an address (exception vector) predetermined for each exception. Processing of exceptions occurs in supervisor mode.

Although multiple exception conditions can map to a single exception vector, a more specific condition may be determined by examining a register associated with the exception - for example, the DSISR and the FPSCR. Additionally, some exception conditions can be explicitly enabled or disabled by software.

The PowerPC architecture requires that exceptions be handled in program order; therefore, although a particular implementation may recognize exception conditions out of order, they are presented strictly in order. When an instruction-caused exception is recognized, any unexecuted instructions that appear earlier in the instruction stream, including any that have not yet entered the execute state, must be completed before the exception is taken. Any exceptions caused by such instructions are handled first. Likewise, exceptions that are asynchronous and precise are recognized when they occur, but are not handled until the instruction currently in the completion state successfully completes execution or generates an exception, and the completed store queue is emptied.

Unless a catastrophe event causes a system reset or machine check exception, only one exception is handled at a time. If, for example, a single instruction encounters multiple exception conditions, those conditions are encountered sequentially.

After the exception handler handles an exception, the instruction execution continues until the next exception condition is encountered. However, in many cases there is no attempt to re-execute the instruction. This method of recognizing and handling exception conditions sequentially guarantees that exceptions are recoverable.

Exception handlers should save the information stored in SRR0 and SRR1 early to prevent the program state from being lost due to a system reset and machine check exception or to an instruction-caused exception in the exception handler, and before enabling external interrupts.

The PowerPC architecture supports four types of exceptions:

- **Synchronous, Precise** – these are caused by instructions. All instruction-caused exceptions are handled precisely; that is, the machine state at the time the exception occurs is known and can be completely restored. This means that (excluding the trap and system call exceptions) the address of the faulting instruction is provided to the exception handler and that neither the faulting instruction nor subsequent instructions in the code stream will complete execution before the exception is taken. Once the exception is processed, execution resumes at the address of the faulting instruction (or at an alternate address provided by the exception handler). When an exception is taken due to a trap or system call instruction, execution resumes at an address provided by the handler.

The 603R's TLBs are 64-entry, 2-way set-associative caches that contain instruction and data address translations. The 603R provides hardware assistance for software table search operations through the ashed page table on the TLB misses. The supervisor software can invalidate TLB entries selectively.

The 603R also provides independent four-entry BAT arrays for instructions and data that maintain address translations for blocks of memory. These entries define blocks that can vary from 128 Kbytes to 256 Mbytes. The BAT arrays are maintained by system software.

As specified by the PowerPC architecture, the hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

Also as specified by the PowerPC architecture, the page table contains a number of Page Table Entry Groups (PTEGs). A PTEG contains eight Page Table Entries (PTEs) of eight bytes each; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

12.4.3 Instruction Timing

The 603R is a pipelined superscalar processor. A pipelined processor is one in which the processing of an instruction is reduced into discrete stages. Because the processing of an instruction is broken into a series of stages, an instruction does not require the entire resources of an execution unit. For example, after an instruction completes the decode stage, it can pass on to the next stage, while the subsequent instruction can advance into the decode stage. This improves the throughput of the instruction flow. For example, it may take three cycles for a floating-point instruction to complete, but if there are no stalls in the floating-point pipeline, a series of floating-point instructions can have a throughput of one instruction per cycle.

The instruction pipeline in the 603R has four major pipeline stages, described as follows:

- The fetch pipeline stage primarily involves retrieving instructions from the memory system and determining the location of the next instruction retrieval. Additionally, the BPU decodes branches during the fetch stage and folds out branch instructions before the dispatch stage if possible.
- The dispatch pipeline stage is responsible for decoding the instructions supplied by the instruction retrieval stage, and determining which of the instructions are eligible to be dispatched in the current cycle. In addition, the source operands of the instructions are read from the appropriate register file and dispatched with the instruction to the execute pipeline stage. At the end of the dispatch pipeline stage, the dispatched instructions and their operands are latched by the appropriate execution unit.
- During the execute pipeline stage each execution unit that has an executable instruction executes the selected instruction (perhaps over multiple cycles), writes the instruction's result into the appropriate rename register, and notifies the completion stage when the instruction has finished execution. In the case of an internal exception, the execution unit reports the exception to the completion/writeback pipeline stage and discontinues instruction execution until the exception is handled. The exception is not signaled until that instruction is the next to be completed. Execution of most floating-point instructions is pipelined within the FPU allowing up to three instructions to be executing in the FPU concurrently. The pipeline stages for the floating-point unit are multiply, add, and round-convert. Execution of most load/store instructions is also pipelined. The load/store unit has two pipeline stages. The first stage is for effective address calculation and MMU translation and the second stage is for accessing the data in the cache.

15. Package Mechanical Data

The following sections provide the package parameters and mechanical dimensions for the CBGA, HiTCE CBGA and the Cerquad packages.

15.1 HiTCE CBGA Package Parameters

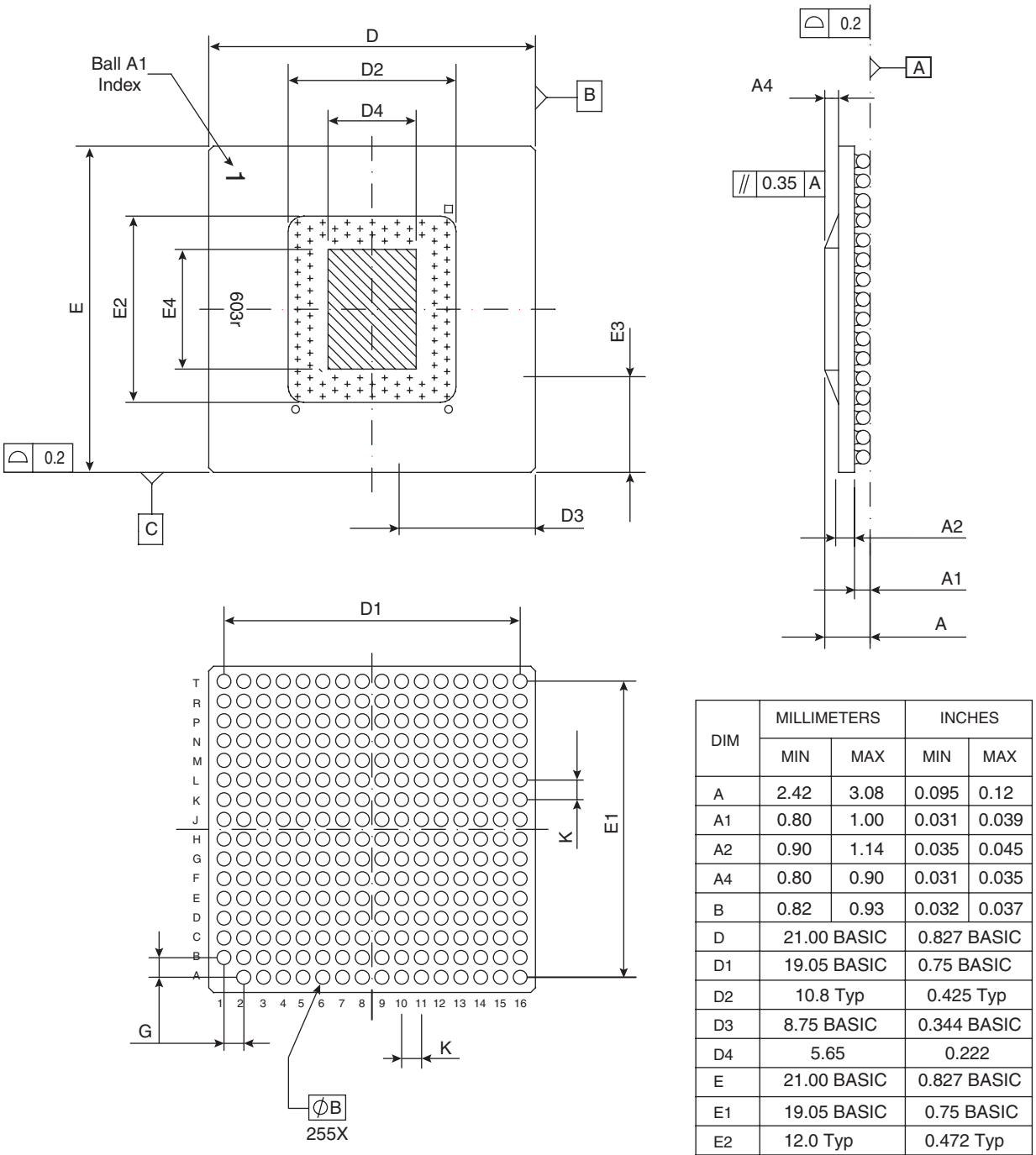
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead HiTCE Ceramic Ball Array (HiTCE CBGA).

Package outline	21 mm × 21 mm
Interconnects	255
Pitch	1.27 mm
Maximum module height	3.08 mm

15.1.1 Mechanical Dimensions of the HiTCE CBGA Package

Figure 15-1 provides the mechanical dimensions and bottom surface nomenclature of the HiTCE CBGA package.

Figure 15-1. Mechanical Dimensions of the HiTCE CBGA Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.42	3.08	0.095	0.12
A1	0.80	1.00	0.031	0.039
A2	0.90	1.14	0.035	0.045
A4	0.80	0.90	0.031	0.035
B	0.82	0.93	0.032	0.037
D	21.00 BASIC		0.827 BASIC	
D1	19.05 BASIC		0.75 BASIC	
D2	10.8 Typ		0.425 Typ	
D3	8.75 BASIC		0.344 BASIC	
D4	5.65		0.222	
E	21.00 BASIC		0.827 BASIC	
E1	19.05 BASIC		0.75 BASIC	
E2	12.0 Typ		0.472 Typ	
E3	6.15 BASIC		0.242 BASIC	
E4	7.7		0.303	
G, K	1.27 BASIC		0.05 BASIC	

15.3 CI-CGA Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm, 255-lead ceramic ball grid array (CI-CGA).

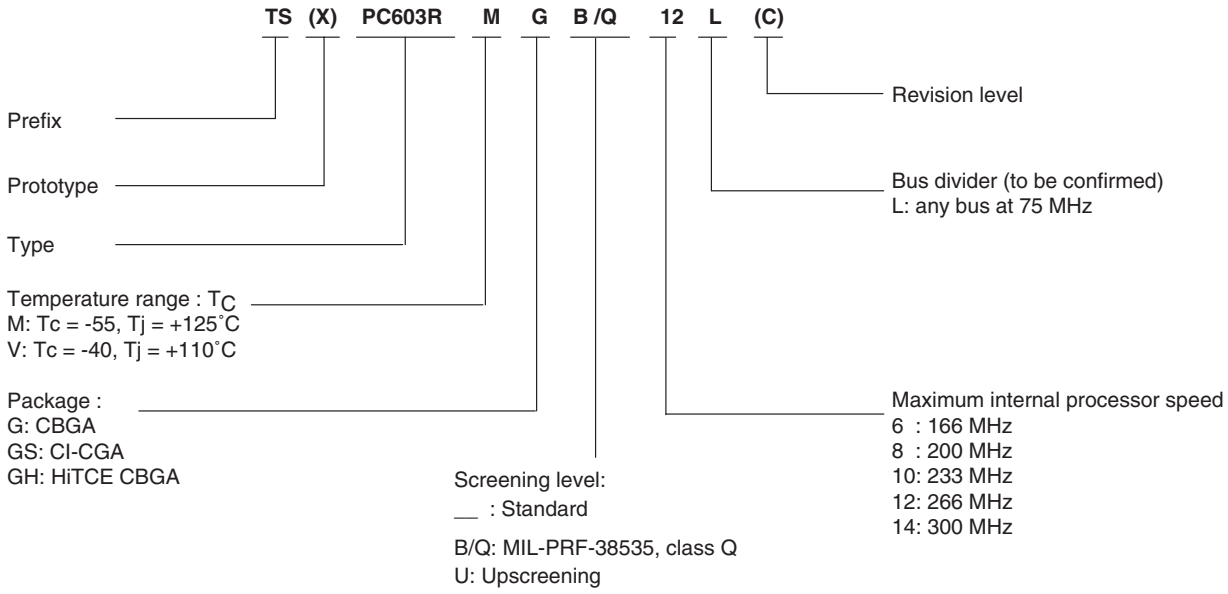
Package outline	21 mm × 21 mm
Interconnects	255
Pitch	1.27 mm
Typical module height	3.84 mm

15.3.1 Mechanical Dimensions of the CI-CGA Package

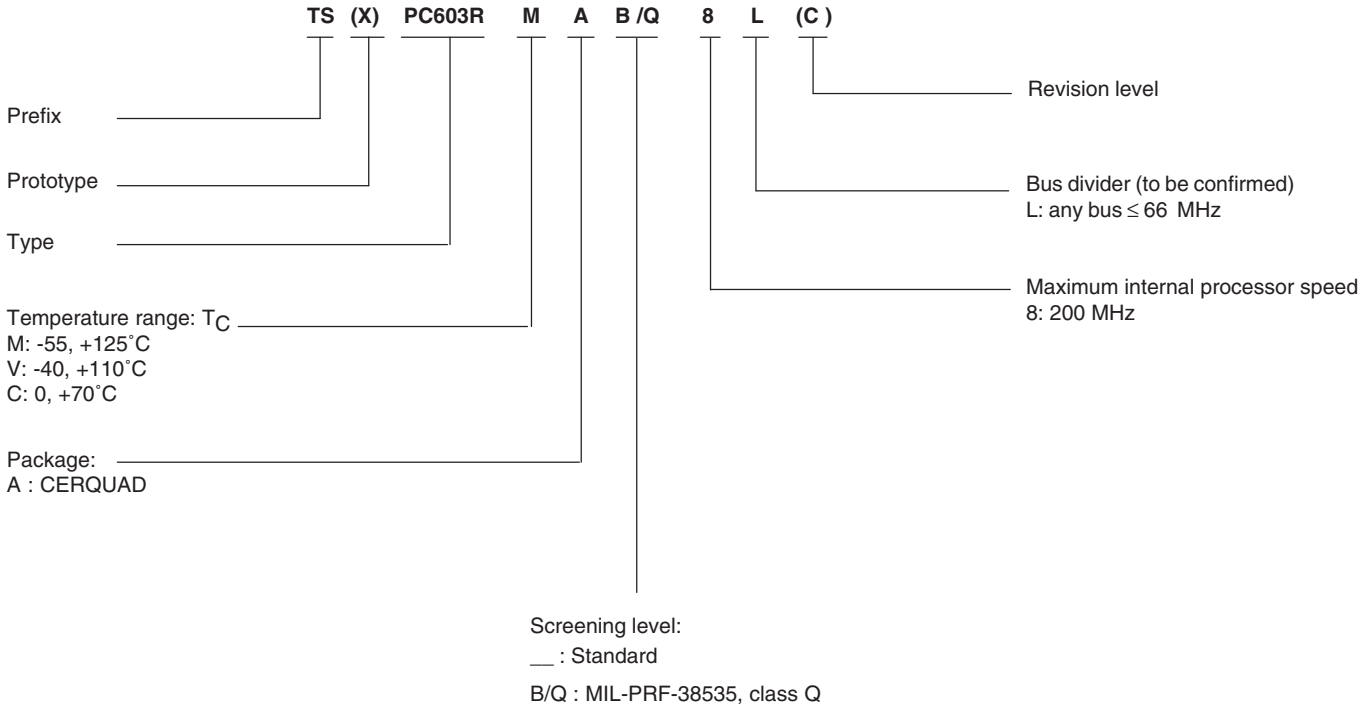
Figure 15-3 provides the mechanical dimensions and bottom surface nomenclature of the CI-CGA package.

16. Ordering Information

16.1 Ordering Information of the CBGA, CI-CGA and HiTCE Packages



16.2 Ordering Information of the CERQUAD 240 Package



Note: For availability of the different versions, contact your Atmel sales office.

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