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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	233MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	255-BCBGA Exposed Pad
Supplier Device Package	255-CI-CBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgs10lc

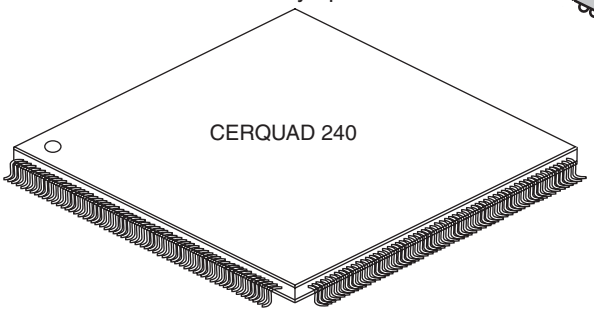
The 603R uses an advanced, 2.5/3.3V CMOS process technology and maintains full interface compatibility with TTL devices. It also integrates in-system testability and debugging features through JTAG boundary-scan capabilities.

2. Screening/Quality/Packaging

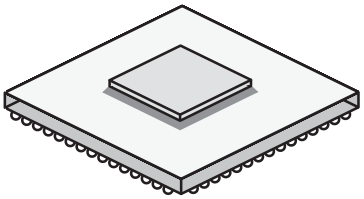
This product is manufactured in full compliance with:

- HiTCE CBGA according to Atmel Standards
- CI-CGA 255 and Cerquad: MIL-PRF-38535 class Q or according to Atmel standards
- CBGA 255: Upscreenings based upon Atmel standards
- CBGA, CI-CGA, HiTCE packages:
  - Full military temperature range (T_C = -55°C, T_j = +125°C)
  - Industrial temperature range (T_C = -40°C, T_j = +110°C)
- Cerquad:
  - Full military temperature range (T_C = -55°C, T_c = +125°C)
  - Industrial temperature range (T_C = -40°C, T_c = +110°C)
  - Commercial temperature ranges (T_C = 0°C, T_C = +70°C)
- Internal I/O Power Supply = 2.5 ±5% // 3.3V ±5%

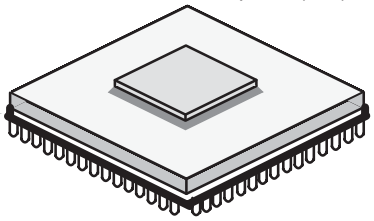
A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier
Cavity up



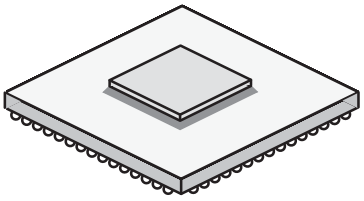
G suffix
CBGA 255
Ceramic Ball Grid Array



GS suffix
CI-CGA 255
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)



GH suffix
HiTCE 255
Ceramic Ball Grid Array



7.1 Design and Construction

7.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 10-2 on page 15, Table 10-4 on page 18, "Recommended Operating Conditions" on page 6, Figure 15-2 on page 49, Figure 15-4 on page 52 and Figure 5-1 on page 5.

7.1.2 *Lead Material and Finish*

Lead material and finish shall be as specified in MIL-STD-1835. (See "Package Mechanical Data" on page 47.)

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only and functional operation at the maximum is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

7.2.1 Absolute Maximum Ratings for the 603R(1)(2)(3)

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	-0.3	2.75	V
PLL supply voltage	AV_{DD}	-0.3	2.75	V
I/O supply voltage	OV_{DD}	-0.3	3.6	V
Input voltage	V_{IN}	-0.3	5.5	V
Storage temperature range	T_{STG}	-55	+150	°C

Notes:
1. **Caution**: The input voltage must not be greater than OV_{DD} by more than 2.5V at any time, including during power-on reset.
2. **Caution**: The OV_{DD} voltage must not be greater than V_{DD}/AV_{DD} by more than 1.2V at any time, including during power-on reset.
3. **Caution**: The V_{DD}/AV_{DD} voltage must not be greater than OV_{DD} by more than 0.4V at any time, including during power-on reset.

Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

7.2.2 Recommended Operating Conditions

The following are the recommended and tested operating conditions. Proper device operation outside of these ranges is not guaranteed.

7.2.3 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	2.375	2.625	V
PLL supply voltage	AV_{DD}	2.375	2.625	V
I/O supply voltage	OV_{DD}	3.135	3.465	V
Input voltage	V_{IN}	GND	5.5	V
Operating temperature	T_c	-55	+125	°C
Junction operating temperature specific to Cerquad	T_j	–	+135	°C

9.2 Programmable Power Modes

The 603R provides four programmable power states, full power, doze, nap and sleep. The software selects these modes by setting one (and only one) of the three power saving mode bits. The hardware can enable a power management state through external asynchronous interrupts. The hardware interrupt causes the transfer of program flow to interrupt the handler code. The appropriate mode is then set by the software. The 603R provides a separate interrupt and interrupt vector for power management, the System Management Interrupt (SMI). The 603R also contains a decrement timer which allows it to enter the nap or doze mode for a predetermined amount of time and then return to full power operation through the Decrementer Interrupt (DI). Note that the 603R cannot switch from power-on management mode to another without first returning to full on mode. The nap and sleep modes disable bus snooping; therefore, a hardware handshake is provided to ensure coherency before the 603R enters these power management modes.

Table 9-1 summarizes the four power states.

Table 9-1. Power PC 603R Microprocessor Programmable Power Modes

PM Mode	Functioning Units	Activation Method	Full-power Wake-up Method
Full Power	All units active	–	–
Full Power (with DPM)	Requested logic by demand	By instruction dispatch	–
Doze	- Bus snooping - Data cache as needed - Decrementer timer	Controlled by SW	External asynchronous exceptions(1) Decrementer interrupt Reset
Nap	Decrementer timer	Controlled by hardware and software	External asynchronous exceptions Decrementer interrupt Reset
Sleep	None	Controlled by hardware and software	External asynchronous exceptions Reset

Note: 1. Exceptions are referred to as interrupts in the architecture specification.

9.3 Power Management Modes

The following describes the characteristics of the 603R's power management modes, the requirements for entering and exiting the various modes, and the system capabilities provided by the 603R while the power management modes are active.

Full Power Mode with DPM Disabled

Full power mode with DPM disabled; power mode is selected when the DPM enable bit (bit 11) in HID0 is cleared

- Default state following power-up and $\overline{\text{HRESET}}$
- All functional units are operating at full processor speed at all times

Full Power Mode with DPM Enabled

Full power mode with DPM enabled (HID0[11] = 1); provides on-chip power management without affecting the functionality or performance of the 603R

- Required functional units are operating at full processor speed

- Functional units are clocked only when needed
- No software or hardware intervention required after mode is set
- Software/hardware and performance are transparent

Doze Mode

The doze mode disables most functional units but maintains cache coherency by enabling the bus interface unit and snooping. A snoop hit will cause the 603R to enable the data cache, copy the data back to the memory, disable the cache, and fully return to the doze state. In this mode:

- Most functional units are disabled
- Bus snooping and time base/decrementer are still enabled
- Dose mode sequence:
  - Set doze bit (HID0[8] = 1)
  - 603R enters doze mode after several processor clocks
- There are several methods for returning to full-power mode
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- The Transition to full-power state takes no more than a few processor cycles
- Phase Locked Loop (PLL) running and locked to SYSCLK

Nap Mode

The nap mode disables the 603R but still maintains the phase locked loop (PLL) and the time base/decrementer. The time base can be used to restore the 603R to full-on state after a programmed amount of time. Because bus snooping is disabled for nap and sleep modes, a hardware handshake using the quiesce request ($\overline{\text{QREQ}}$) and quiesce acknowledge ($\overline{\text{QACK}}$) signals is required to maintain data coherency. The 603R will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603R will enter the sleep or nap mode. In this mode:

- The time base/decrementer is still enabled
- Most functional units are disabled (including bus snooping)
- All non-essential input receivers are disabled
- Nap mode sequence:
  - Set nap bit (HID0[9] = 1)
  - 603R asserts quiesce request ($\overline{\text{QREQ}}$) signal
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$) signal
  - 603R enters sleep mode after several processor clocks
- There are several methods for returning to full-power mode:
  - Assert $\overline{\text{INT}}$, $\overline{\text{SPI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- Transition to full-power takes no more than a few processor cycles
- The PLL is running and locked to SYSCLK

9.5 Power Dissipation

Table 9-2. Power Dissipation[1][2][3][4] with V_{DD}/AV_{DD} = 2.5 ±5%V, OV_{DD} = 3.3 ±5%V, GND = 0V, 0°C ≤ T_C ≤ 125°C

	Cerquad 240 Package		CBGA 255, HiTCE CBGA 255 and CI-CGA 255					
CPU Clock Frequency	**166 MHz**	**200 MHz**	**166 MHz**	**200 MHz**	**233 MHz**	**266 MHz**	**300 MHz**	**Units**
Full-on Mode (DPM Enabled)								
Typical	2.1	2.5	2.1	2.5	3	3.5	4	W
Max	3.2	4	3.2	4	4.6	5.3	6	W
Doze Mode								
Typical	1.5	1.7	1.5	1.7	1.8	2	2.1	W
Nap Mode								
Typical	100	120	100	120	140	160	180	mW
Sleep Mode								
Typical	96	110	96	110	123	135	150	mW
Sleep Mode-PLL Disabled								
Typical	60	60	60	60	60	60	60	mW
Sleep Mode-PLL and SYSCLK Disabled								
Typical	25	25	25	25	25	25	25	mW
Maximum	60	60	60	60	60	80	100	mW

Notes:
1. These values apply for all valid PLL_CFG[0-3] settings and do not include output driver power (OV_{DD}) or analog supply power (AV_{DD}). OV_{DD} power is system dependent but is typically ≤ 10% of V_{DD}. Worst case AV_{DD} = 15 mW.
2. Typical power is an average value measured at $V_{DD} = AV_{DD}$ = 2.5V, OV_{DD} = 3.3V, in a system executing typical applications and benchmark sequences.
3. Maximum power is measured at V_{DD} = 2.625V using a worst-case instruction mix.
4. To calculate the power consumption at low temperature (-55°C), **use a factor of 1.25.**

9.6 Marking

Each microcircuit is legible and permanently marked with at least the following information:

- Atmel logo
- Manufacturer's part number
- Class B identification if applicable
- Date code of inspection lot
- ESD identifier if available
- Country of manufacture

10. Pin Assignments

10.1 CBGA 255 and CI-CGA 255 Packages

Figure 10-1 (pin matrix) shows the pinout as viewed from the top of the CBGA and CI-CGA packages. The direction of the top surface view is shown by the side profile of the packages.

Table 10-2. Signal Pinout Listing (Continued)

Signal Name	CBGA, HiTCE CBGA and CI-CGA Pin Number	Active	I/O
$\overline{\text{GBL}}$	F01	Low	I/O
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TSTCLK(1)	D11	-	Input
L2_TSTCLK(1)	D12	-	Input
$\overline{\text{LSSD\_MODE}}$(1)	B10	Low	Input
$\overline{\text{MCP}}$	C13	Low	Input
PLL_CFG[0-3]	A08, B09, A09, D09	High	Input
$\overline{\text{QACK}}$	D03	Low	Input
$\overline{\text{QREQ}}$	J03	Low	Output
$\overline{\text{RSRV}}$	D01	Low	Output
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	-	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC[0-1]	A02, A03	High	Output
TCK	C11	-	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
$\overline{\text{TLBISYNC}}$	C04	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ[0-2]	A13, D10, B12	High	I/O
TT[0-4]	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
NC	B07, B08, C03, C06, C08, D05, D06, F03, H04, J16	Low	Input
VOLTDETGND(2)	F03	Low	Output

Notes: 1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. NC (not connected) in the 603e BGA package; internally tied to GND in the 603R BGA package to indicate to the power supply that a low-voltage processor is present.

Table 10-4. Signal Pinout Listing (Continued)

Signal Name	CERQUAD Pin Number
$\overline{\text{INT}}$	188
L1_TSTCLK[1]	204
L2_TSTCLK[1]	203
$\overline{\text{LSSD\_MODE}}$[1]	205
$\overline{\text{MCP}}$	186
PLL_CFG[0-3]	213, 211, 210, 208
$\overline{\text{QACK}}$	235
$\overline{\text{QREQ}}$	31
$\overline{\text{RSRV}}$	232
$\overline{\text{SMI}}$	187
$\overline{\text{SRESET}}$	189
SYSCLK	212
$\overline{\text{TA}}$	155
TBEN	234
$\overline{\text{TBST}}$	192
TC[0-1]	224, 223
TCK	201
TDI	199
TDO	198
$\overline{\text{TEA}}$	154
$\overline{\text{TLBISYNC}}$	233
TMS	200
$\overline{\text{TRST}}$	202
$\overline{\text{TS}}$	149
TSIZ[0-2]	197, 196, 195
TT[0-4]	191, 190, 185, 184, 180
$\overline{\text{WT}}$	236
NC	

Notes: 1. These are test signals for factory use only and must be pulled up to V_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core. Future members of the 603 family may use different OV_{DD} and V_{DD} input levels.

3. Leakage currents are measured for nominal OV_{DD} and V_{DD} or both OV_{DD} and V_{DD}. Same variation (for example, both V_{DD} and OV_{DD} vary by either +5% or -5%)

11.3 Dynamic Characteristics

11.3.1 Clock AC Specifications

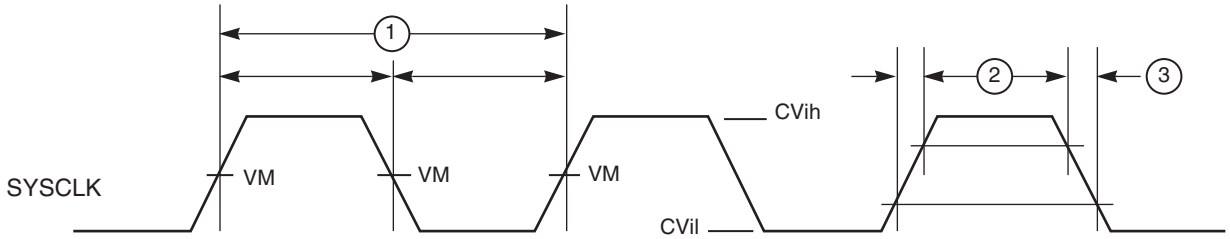
Table 11-2 provides the clock AC timing specifications as defined in Figure 11-1.

Table 11-2. Clock AC Timing Specifications[1][2][3][4] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Figure Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and CERQUAD				CBGA 255, HiTCE CBGA 255 and CI-CGA 255							
		166 MHz		200 MHz		233 MHz		266 MHz		300 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
	Processor Frequency	150	166	150	200	180	233	180	266	180	300	MHz	[5]
	VCO Frequency	300	332	300	400	360	466	360	532	360	600	MHz	[5]
	SYSCLK (bus) Frequency	25	66.7	33.3	66.7	33.3	75	33.3	75	33.3	75	MHz	[5]
1	SYSCLK Cycle Time	15	30	13.3	30	13.3	30	13.3	30	13.3	30	ns	
2,3	SYSCLK Rise and Fall Time	–	2	–	2	–	2	–	2	–	2	ns	[1]
4	SYSCLK Duty Cycle (1.4V measured)	40	60	40	60	40	60	40	60	40	60	%	[3]
	SYSCLK Jitter	–	±150	–	±150	–	±150	–	±150	–	±150	ps	[2]
	603R Internal PLL Relock Time	–	100	–	100	–	100	–	100	–	100	µs	[3][4]

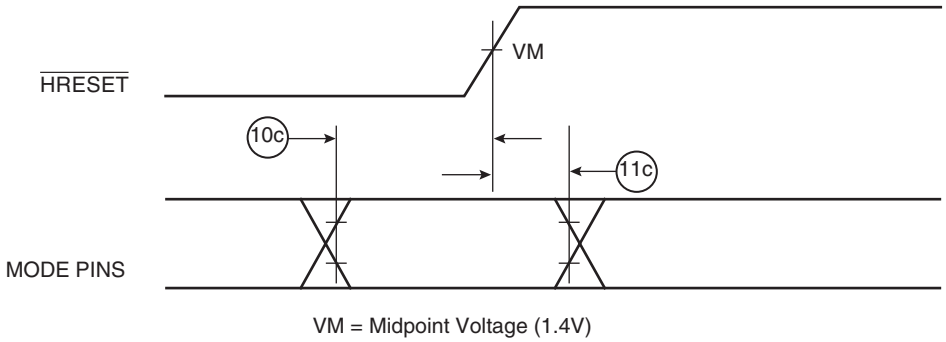
Notes:
1. Rise and fall times for the SYSCLK input are measured from 0.4V to 2.4V.
2. Cycle-to-cycle jitter is guaranteed by design.
3. Timing is guaranteed by design and characterization and is not tested.
4. The PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD}, OV_{DD}, AV_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen so that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description for valid PLL_CFG[0-3] settings.

Figure 11-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage (1.4V)

Figure 11-3. Mode Select Input Timing Diagram



11.3.3 Output AC Specifications

Table 11-4 provides the output AC timing specifications for the 603R (shown in Figure 11-4).

Table 11-4. Output AC Timing Specifications[1][2] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $55°C \le T_C \le 125°C$

Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages		CBGA 255, HiTCE CBGA 255 and CI-CGA 255				Unit	Note
		166, 200 MHz		233, 266 MHz		300 MHz			
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1	–	1	–	1	–	ns	
13a	SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(4)
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	8	–	8	–	8	ns	(6)
14a	SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11	–	11	–	11	ns	(4)
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(6)
15	SYSCLK to output invalid (output hold)	1	–	1	–	1	–	ns	(3)
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	8.5	–	8	–	8	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(7)
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	8	–	7.5	–	7.5	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK}	–	ns	(3)(5) (8)
20	Maximum delay to $\overline{ARTRY}$ precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(8)
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	–	2	–	2	–	2	t_{SYSCLK}	(6)(8)

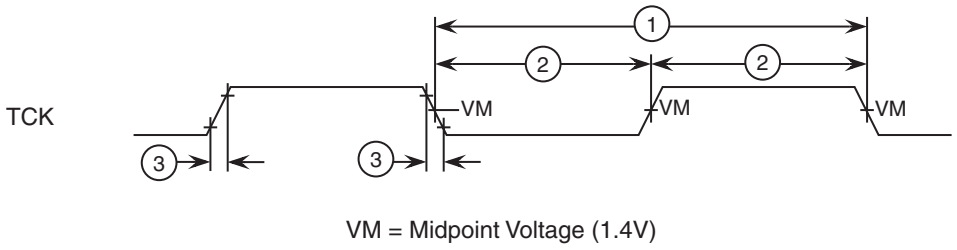
11.4 JTAG AC Timing Specifications

Table 11-5. JTAG AC Timing Specifications (independent of SYSCLK); $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $-55°C \le T_C \le 125°C$

Number	Characteristics	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	–	ns	
2	TCK clock pulse width measured at 1.4V	25	–	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{TRST}$ setup time to TCK rising edge	13	–	ns	(1)
5	$\overline{TRST}$ assert time	40	–	ns	
6	Boundary scan input data setup time	6	–	ns	(2)
7	Boundary scan input data hold time	27	–	ns	(2)
8	TCK to output data valid	4	25	ns	(3)
9	TCK to output high impedance	3	24	ns	(3)
10	TMS, TDI data setup time	0	–	ns	
11	TMS, TDI data hold time	25	–	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

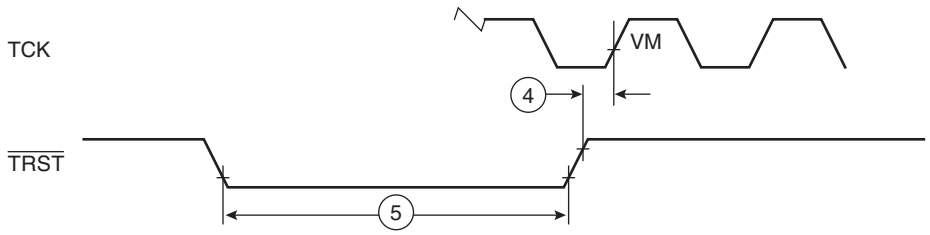
Notes: 1. $\overline{TRST}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 11-5. Clock Input Timing Diagram



VM = Midpoint Voltage (1.4V)

Figure 11-6. $\overline{TRST}$ Timing Diagram



– The Time Base register (TB) is a 64-bit register that maintains the time of day and operates interval timers. The TB consists of two 32-bit fields - Time Base Upper (TBU) and Time Base Lower (TBL).

– The Processor Version Register (PVR) is a 32-bit, read-only register that identifies the version (model) and revision level of the PowerPC processor.

– Block Address Translation (BAT) arrays - The PowerPC architecture defines 16 BAT registers, divided into four pairs of Data BATs (DBATs) and four pairs of instruction BATs (IBATs). See Figure 12-1 for a list of the SPR numbers for the BAT arrays.

The following supervisor-level SPRs are implementation-specific to the 603R:

– The DMISS and IMISS registers are read-only registers that are loaded automatically upon an instruction or data TLB miss.

– The HASH1 and HASH2 registers contain the physical addresses of the primary and secondary Page Table Entry Groups (PTEGs).

– The ICMP and DCMP registers contain a duplicate of the first word in the Page Table Entry (PTE) for which the table search is looking.

– The Required Physical Address (RPA) register is loaded by the processor with the second word of the correct PTE during a page table search.

– The hardware implementation (HID0 and HID1) registers provide the means for enabling the 603R's checkstops and features, and allows software to read the configuration of the PLL configuration signals.

– The Instruction Address Breakpoint Register (IABR) is loaded with an instruction address that is compared to instruction addresses in the dispatch queue. When an address match occurs, an instruction address breakpoint exception is generated.

Figure 12-1 shows all the 603R registers available at the user and supervisor level. The number to the right of the SPRs indicate the number that is used in the syntax of the instruction operands to access the register.

12.2 Instruction Set and Addressing Modes

The following subsections describe the PowerPC instruction set and addressing modes in general.

12.2.1 PowerPC Instruction Set and Addressing Modes

All PowerPC instructions are encoded as single-word (32-bit) opcodes. Instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses. This fixed instruction length and consistent format greatly simplifies instruction pipelining.

PowerPC Instruction Set

The PowerPC instructions are divided into the following categories:

- **Integer Instructions** – these include computational and logical instructions
  - Integer arithmetic instructions
  - Integer compare instructions
  - Integer logical instructions
  - Integer rotate and shift instructions
- **Floating-point Instructions** – these include floating-point computational instructions, as well as instructions that affect the FPSCR
  - Floating-point arithmetic instructions
  - Floating-point multiply/add instructions
  - Floating-point rounding and conversion instructions
  - Floating-point compare instructions
  - Floating-point status and control instructions
- **Load/Store Instructions** – these include integer and floating-point load and store instructions
  - Integer load and store instruction
  - Integer load and store multiple instructions
  - Floating-point load and store
  - Primitives used to construct atomic memory operations (**lwarx** and **stwcx** instructions)
- **Flow Control Instructions** – these include branching instructions, condition register logical instructions, trap instructions, and other instructions that affect the instruction flow
  - Branch and trap instructions
  - Condition register logical instructions
- **Processor Control Instructions** – these instructions are used for synchronizing memory accesses and management of caches, TLBs, and the segment registers
  - Move to/from SPR instructions
  - Move to/from MSR
  - Synchronize
  - Instruction synchronize

- **Memory Control Instructions** – these instructions provide control of caches, TLBs, and segment registers
  - Supervisor-level cache management instructions
  - User-level cache instructions
  - Segment register manipulation instructions
  - Translation lookaside buffer management instructions

Note that this grouping of the instructions does not indicate which execution unit executes a particular instruction or group of instructions.

Integer instructions operate on byte, half-word, and word operands. Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands. The PowerPC architecture uses instructions that are four bytes long and word-aligned. It provides for byte, half-word, and word operand loads and stores between the memory and a set of 32 GPRs. It also provides for word and double-word operand loads and stores between the memory and a set of 32 Floating-point Registers (FPRs).

Computational instructions do not modify the memory. To use a memory operand in a computation and then modify the same or another memory location, the memory contents must be loaded into a register, modified, and then written back to the target location with distinct instructions.

PowerPC processors follow the program flow when they are in the normal execution state. However, the flow of instructions can be interrupted directly by the execution of an instruction or by an asynchronous event. Either kind of exception may cause one of several components of the system software to be invoked.

- Calculating Effective Address

  The Effective Address (EA) is the 32-bit address computed by the processor when executing a memory access or branch instruction or when fetching the next sequential instruction.

  The PowerPC architecture supports two simple memory addressing modes:

  - EA = (RA|0) + offset (including offset = 0) (register indirect with immediate index)
  - EA = (RA|0) + rB (register indirect with index)

These simple addressing modes allow efficient address generation for memory accesses. Calculation of the effective address for aligned transfers occurs in a single clock cycle.

For a memory access instruction, if the sum of the effective address and the operand length exceeds the maximum effective address, the memory operand is considered to wrap around from the maximum effective address to effective address 0.

Effective address computations for both data and instruction accesses use 32-bit unsigned binary arithmetic. A carry over from bit 0 is ignored in 32-bit implementations.

14.2 Decoupling Recommendations

Due to the 603e's dynamic power management feature, large address and data buses, and high operating frequencies, the 603e can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 603e system, and the 603e itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} and OV_{DD} pin of the 603e. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 µF to provide both high and low frequency filtering, and should be placed as close as possible to their associated V_{DD} or OV_{DD} pin. The suggested values for the V_{DD} pins are 220 pF (ceramic), 0.01 µF (ceramic) and 0.1 µf (ceramic). The suggested values for the OV_{DD} pins are 0.01 µF (ceramic), 0.1 µF (ceramic), and 10 µF (tantalum). Only SMT (Surface Mount Technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should also have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. The suggested bulk capacitors are 100 µF (AVX TPS tantalum) or 330 µf (AVX TPS tantalum).

14.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD}. Unused active high inputs should be connected to GND. All NC (non-connected) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins of the 603e.

14.4 Pull-up Resistor Requirements

The 603e requires high-resistive (weak: 10 kΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the 603e or other bus master. These signals are: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$.

In addition, the 603e has three open-drain style outputs that require pull-up resistors (weak or stronger: 4.7 kΩ - 10 kΩ) if they are used by the system. These signals are: $\overline{APE}$, $\overline{DPE}$, and $\overline{CKSTP\_OUT}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the 603e must continually monitor these signals for snooping, this floating condition may cause excessive power to be drawn by the input revivers on the 603e. It is recommended that these signals be pulled up through weak (10 kΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are: A[0-3], AP[0-3], TT[0-4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

15. Package Mechanical Data

The following sections provide the package parameters and mechanical dimensions for the CBGA, HiTCE CBGA and the Cerquad packages.

15.1 HiTCE CBGA Package Parameters

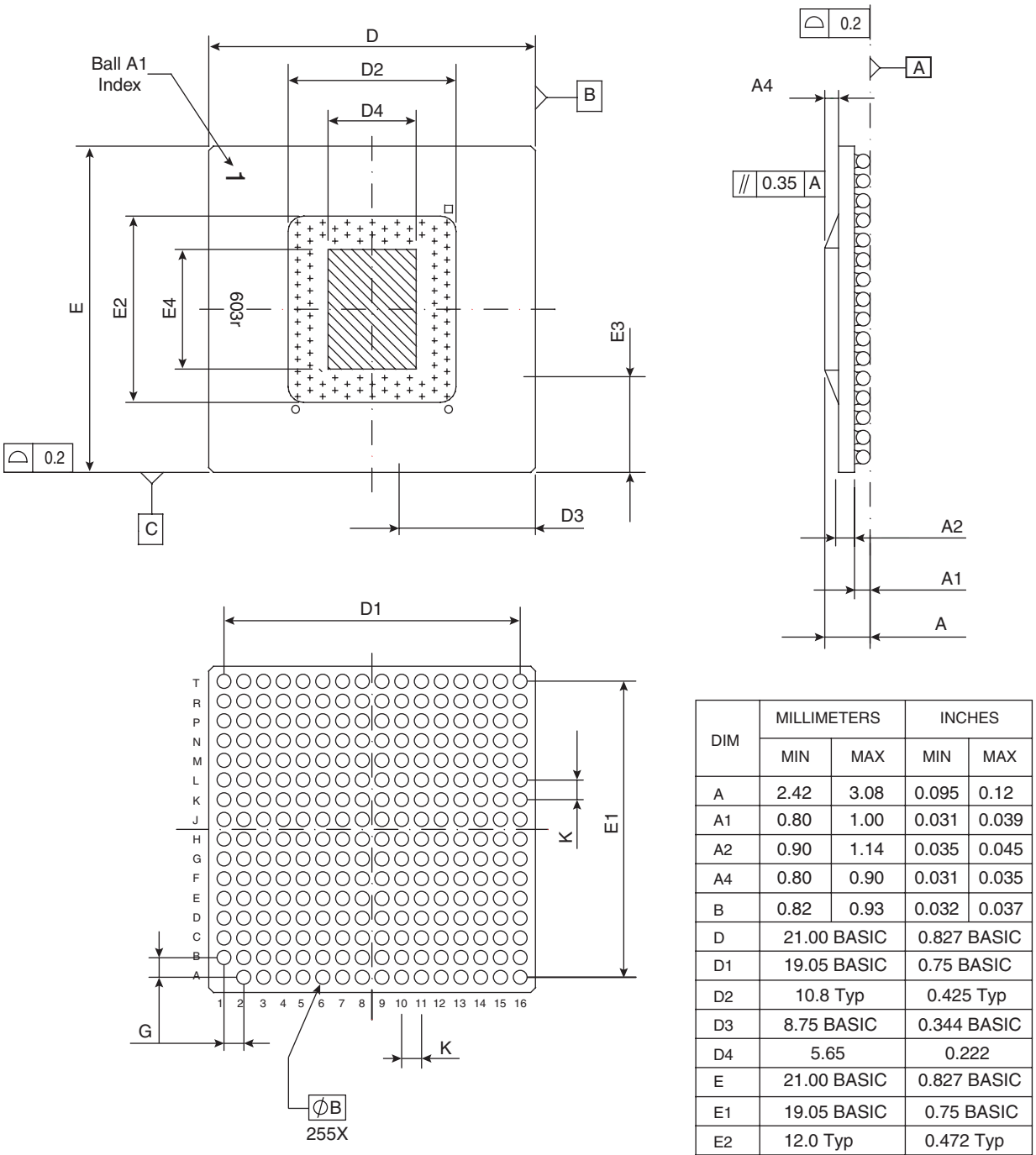
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead HiTCE Ceramic Ball Array (HiTCE CBGA).

Package outline	21 mm × 21 mm
Interconnects	255
Pitch	1.27 mm
Maximum module height	3.08 mm

15.1.1 Mechanical Dimensions of the HiTCE CBGA Package

Figure 15-1 provides the mechanical dimensions and bottom surface nomenclature of the HiTCE CBGA package.

Figure 15-1. Mechanical Dimensions of the HiTCE CBGA Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.42	3.08	0.095	0.12
A1	0.80	1.00	0.031	0.039
A2	0.90	1.14	0.035	0.045
A4	0.80	0.90	0.031	0.035
B	0.82	0.93	0.032	0.037
D	21.00 BASIC		0.827 BASIC	
D1	19.05 BASIC		0.75 BASIC	
D2	10.8 Typ		0.425 Typ	
D3	8.75 BASIC		0.344 BASIC	
D4	5.65		0.222	
E	21.00 BASIC		0.827 BASIC	
E1	19.05 BASIC		0.75 BASIC	
E2	12.0 Typ		0.472 Typ	
E3	6.15 BASIC		0.242 BASIC	
E4	7.7		0.303	
G, K	1.27 BASIC		0.05 BASIC	

15.2 CBGA Package Parameters

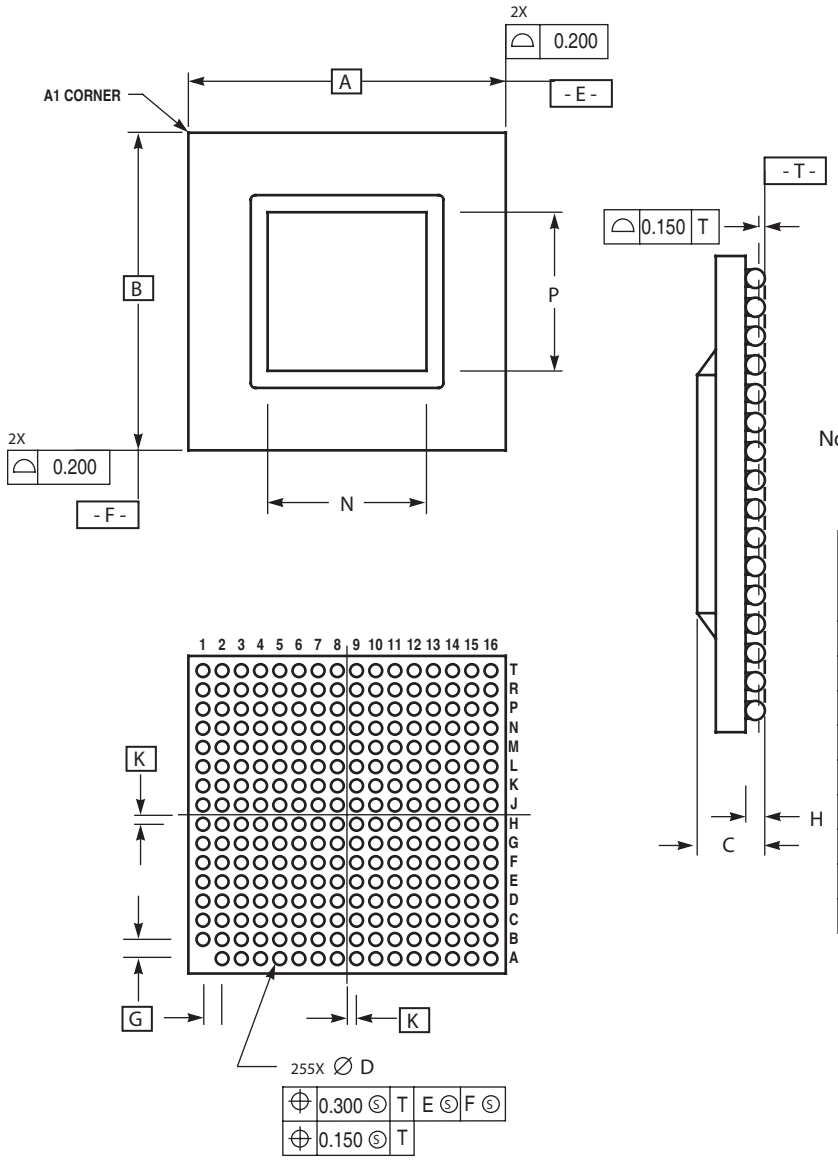
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead Ceramic Ball Grid Array (CBGA).

Package outline	21 mm × 21 mm
Interconnects	255
Pitch	1.27 mm
Maximum module height	3 mm

15.2.1 Mechanical Dimensions of the CBGA Package

Figure 15-2 provides the mechanical dimensions and bottom surface nomenclature of the CBGA package.

Figure 15-2. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package



Notes: 1. Dimensioning and tolerancing per ASME Y14.5M - 1994
2. controlling dimension: millimeter

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.450	3.000	0.097	0.118
D	0.820	0.930	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

15.3 CI-CGA Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm, 255-lead ceramic ball grid array (CI-CGA).

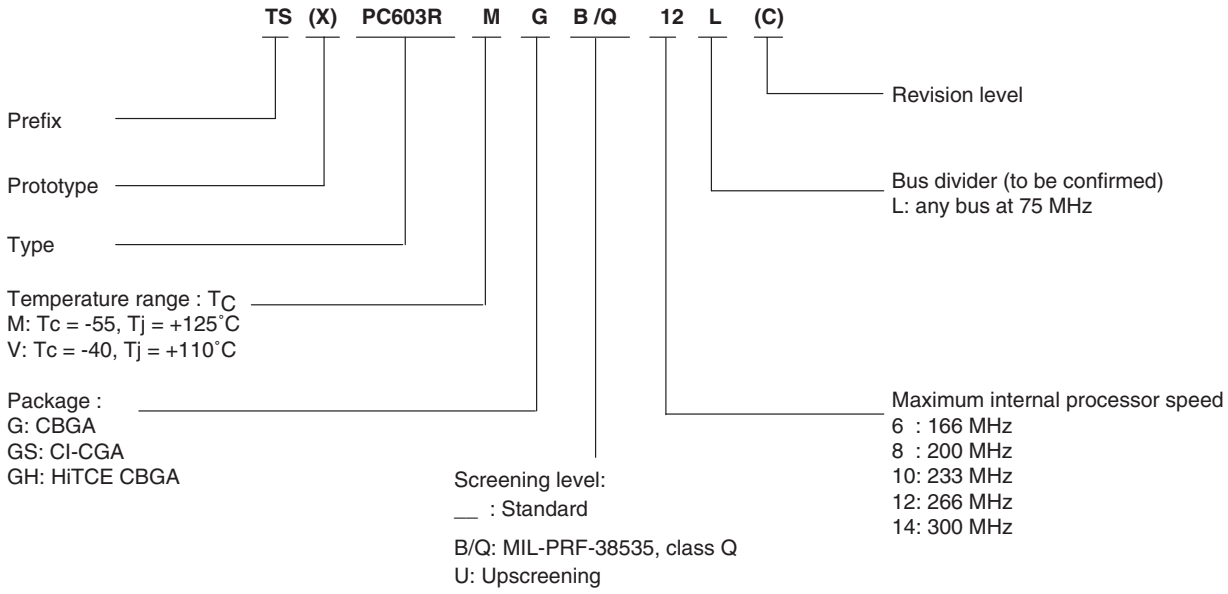
Package outline	21 mm × 21 mm
Interconnects	255
Pitch	1.27 mm
Typical module height	3.84 mm

15.3.1 Mechanical Dimensions of the CI-CGA Package

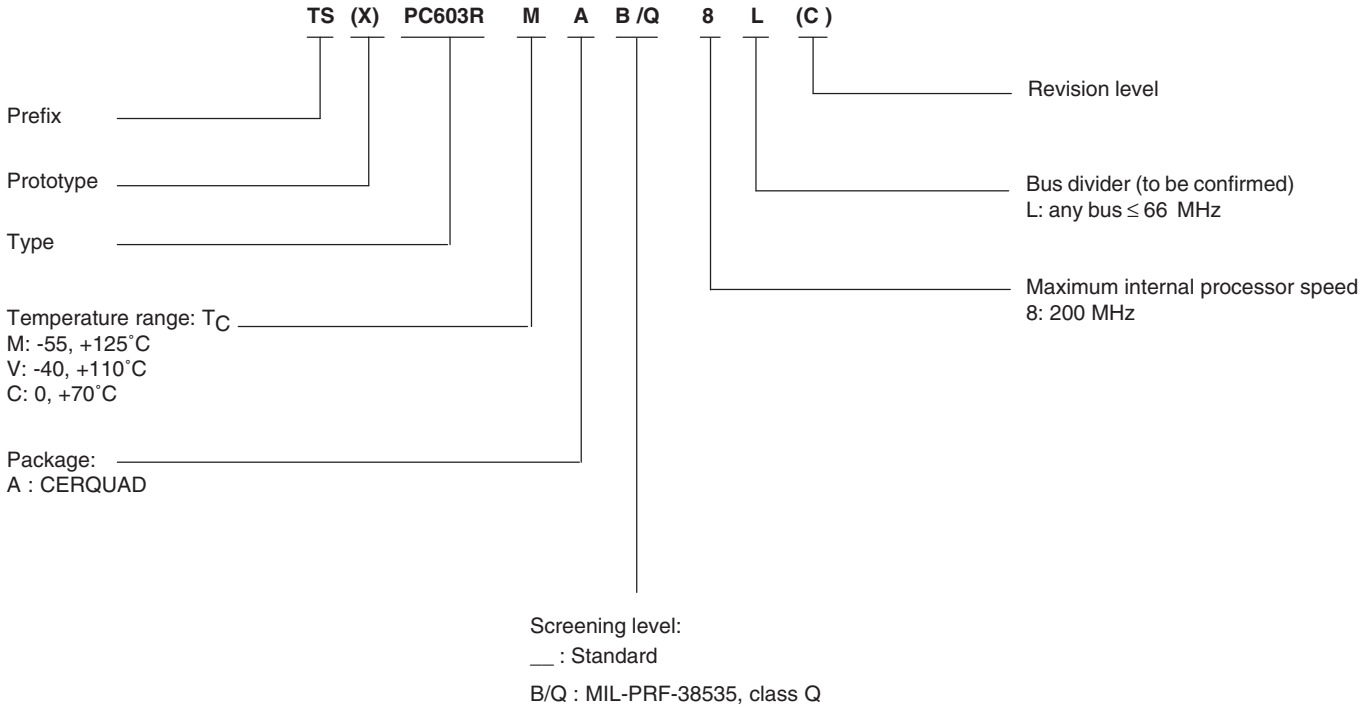
Figure 15-3 provides the mechanical dimensions and bottom surface nomenclature of the CI-CGA package.

16. Ordering Information

16.1 Ordering Information of the CBGA, CI-CGA and HiTCE Packages



16.2 Ordering Information of the CERQUAD 240 Package



Note: For availability of the different versions, contact your Atmel sales office.