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## Understanding Embedded - Microprocessors

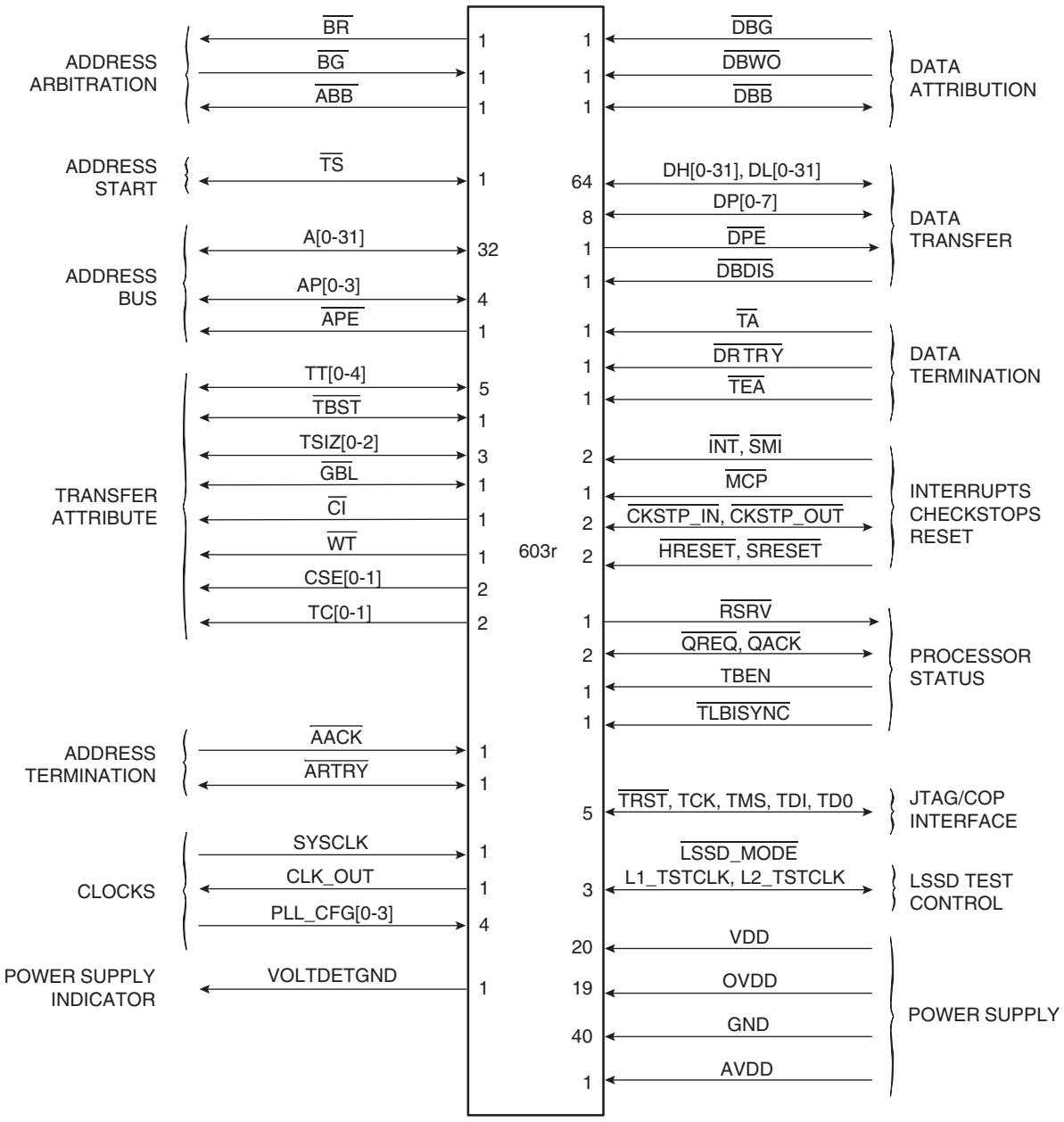
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC 603e |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 166MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 110°C (TC) |
| Security Features | - |
| Package / Case | 255-BCBGA Exposed Pad |
| Supplier Device Package | 255-CI-CBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgs6lc |

**Figure 5-1.** Functional Signal Groups




## 6. Detailed Specifications

This specification describes the specific requirements for the microprocessor TSPC603R, in compliance with MIL-STD-883 class B or Atmel standard screening.

## 7. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

# 8. Thermal Characteristics

## 8.1 CBGA 255 and CI-CGA 255 Packages

The data found in this section concerns 603R devices packaged in the 255-lead 21 mm multi-layer ceramic (MLC) and ceramic BGA package. Data is included for use with a Thermalloy #2328B heat sink.

The internal thermal resistance for this package is negligible due to the exposed die design. A thermal interface material is recommended at the package lid to heat sink interface to minimize the thermal contact resistance.

Additionally, the CBGA package offers an excellent thermal connection to the card and power planes. Heat generated at the chip is dissipated through the package, the heat sink (when used) and the card. The parallel heat flow paths result in the lowest overall thermal resistance as well as offer significantly better power dissipation capability if a heat sink is not used.

The thermal characteristics for the flip-chip CBGA and CI-CGA packages are as follows:

Thermal resistance (junction-to-case) = $R_{jc}$ or
$\theta_{jc}$ = 0.095°C/Watt for the 2 packages.

Thermal resistance (junction-to-ball) = $R_{jb}$ or
$\theta_{jb}$ = 3.5°C/Watt for the CBGA package.

Thermal resistance (junction-to-bottom SCI) = $R_{js}$ or
$\theta_{js}$ = 3.7°C/Watt for the CI-CGA package.

The junction temperature can be calculated from the junction to ambient thermal resistance, as follow:

Junction temperature:

$$T_j = T_a + (R_{jc} + R_{cs} + R_{sa}) \times P$$

where: $T_a$ is the ambient temperature in the vicinity of the device

$R_{jc}$ is the die junction to case thermal resistance of the device

$R_{cs}$ is the case to heat sink thermal resistance of the interface material

$R_{sa}$ is the heat sink to ambient thermal resistance

P is the power dissipated by the device

During operation, the die-junction temperatures ($T_j$) should be maintained at a lower value than the value specified in ”Recommended Operating Conditions” on page 6.

The thermal resistance of the thermal interface material ($R_{cs}$) is typically about 1°C/Watt.

Assuming a $T_a$ of 85°C and a consumption (P) of 3.6 Watts, the junction temperature of the device would be as follow:

$T_j$ = 85°C + (0.095°C/Watt + 1°C/Watt + $R_{sa}$) × 3.5 Watts.

For the Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance ($R_{sa}$) versus airflow velocity is shown in Figure 8-1.

**Table 10-5.** Address and Data Bus Signal Index for Cerquad, CBGA 255 and CI-CGA 255 Packages

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Address Bus | A[0-31] | If output, physical address of data to be transferred<br>If input, represents the physical address of a snoop operation | I/O |
| Data Bus | DH[0-31] | Represents the state of data, during a data write operation if output, or during a data read operation if input | I/O |
| Data Bus | DL[0-31] | Represents the state of data, during a data write operation if output, or during a data read operation if input | I/O |

**Table 10-6.** Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Address Acknowledge | $\overline{\text{AACK}}$ | The address phase of a transaction is complete | Input |
| Address Bus Busy | $\overline{\text{ABB}}$ | If output, the 603R is the address bus master<br>If input, the address bus is in use | I/O |
| Address Bus Parity | AP[0-3] | If output, represents odd parity for each of 4 bytes of the physical address for a transaction<br>If input, represents odd parity for each of 4 bytes of the physical address for snooping operations | I/O |
| Address Parity Error | $\overline{\text{APE}}$ | Incorrect address bus parity detected on a snoop | Output |
| Address Retry | $\overline{\text{ARTRY}}$ | If output, detects a condition in which a snooped address tenure must be retried<br>If input, must retry the preceding address tenure | I/O |
| Bus Grant | $\overline{\text{BG}}$ | May, with the proper qualification, assume mastership of the address bus | Input |
| Bus Request | $\overline{\text{BR}}$ | Request mastership of the address bus | Output |
| Cache Inhibit | $\overline{\text{CI}}$ | A single-beat transfer will not be cached | Output |
| Checkstop Input | $\overline{\text{CKSTP\_IN}}$ | Must terminate operation by internally gating off all clocks, and release all outputs | Input |
| Checkstop Output | $\overline{\text{CKSTP\_OUT}}$ | Has detected a checkstop condition and has ceased operation | Output |
| Cache Set Entry | CSE[0-1] | Cache replacement set element for the current transaction reloading into or writing out of the cache | Output |
| Data Bus Busy | $\overline{\text{DBB}}$ | If output, the 603R is the data bus master<br>If input, another device is bus master | I/O |
| Data Bus Disable | $\overline{\text{DBDIS}}$ | (For a write transaction) must release data bus and the data bus parity to high impedance during the following cycle | Input |
| Data Bus Grant | $\overline{\text{DBG}}$ | May, with the proper qualification, assume mastership of the data bus | Input |
| Data Bus Write Only | $\overline{\text{DBW0}}$ | May run the data bus tenure | Input |
| Data Bus Parity | DP[0-7] | If output, odd parity for each of 8 bytes of data write transactions<br>If input, odd parity for each byte of read data | I/O |
| Data Parity Error | $\overline{\text{DPE}}$ | Incorrect data bus parity | Output |
| Data Retry | $\overline{\text{DRTRY}}$ | Must invalidate the data from the previous read operation | Input |

**Table 10-6.** Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Transfer Start | $\overline{TS}$ | If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid<br>If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$) | I/O |
| Transfer Type | TT[0-4] | Type of transfer in progress | I/O |
| Write-through | $\overline{WT}$ | A single-beat transaction is write-through | Output |

# 11. Electrical Characteristics

## 11.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 11-1: Static electrical characteristics for the electrical variants
- Table 11-2: Dynamic electrical characteristics for the 603R

The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0 to PLL_CFG3 signals. All timings are respectively specified to the rising edge of SYSCLK.

These specifications are for 166 MHz to 300 MHz processor core frequencies for CBGA 255, HiTCE CBGA 255 and CI-CGA 255 packages and 166 MHz to 200 MHz processor core frequencies for the Cerquad 240 package.

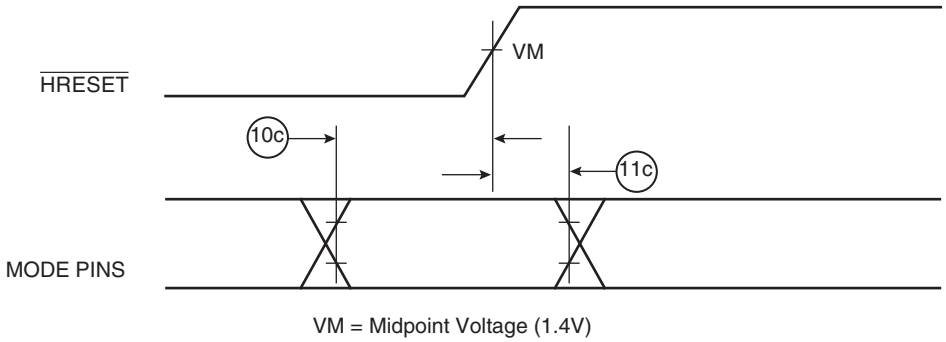
## 11.2 Static Characteristics

**Table 11-1.** Electrical Characteristics with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

| Characteristics | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage (all inputs except SYSCLK) | | $V_{IH}$ | 2 | 5.5 | V |
| Input Low Voltage (all inputs except SYSCLK) | | $V_{IL}$ | GND | 0.8 | V |
| SYSCLK Input High Voltage | | $CV_{IH}$ | 2.4 | 5.5 | V |
| SYSCLK Input Low Voltage | | $CV_{IL}$ | GND | 0.4 | V |
| Input Leakage Current | $V_{IN}$ = 3.465V(1)(3) | $I_{IN}$ | - | 30 | µA |
| | $V_{IN}$ = 5.5V(1)(3) | $I_{IN}$ | - | 300 | µA |
| Hi-Z (off-state) Leakage Current | $V_{IN}$ = 3.465V(1)(3) | $I_{TSI}$ | - | 30 | µA |
| | $V_{IN}$ = 5.5V(1)(3) | $I_{TSI}$ | - | 300 | µA |
| Output High Voltage | $I_{OH}$ = -7 mA | $V_{OH}$ | 2.4 | - | V |
| Output Low Voltage | $I_{OL}$ = +7 mA | $V_{OL}$ | - | 0.4 | V |
| Capacitance, $V_{IN}$ = 0V, f = 1 MHz(2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | | $C_{IN}$ | - | 10 | pF |
| Capacitance, $V_{IN}$ = 0V, f = 1 MHz(2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | | $C_{IN}$ | - | 15 | pF |

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100% tested.

**Figure 11-3.** Mode Select Input Timing Diagram




### 11.3.3 Output AC Specifications

Table 11-4 provides the output AC timing specifications for the 603R (shown in Figure 11-4).

**Table 11-4.** Output AC Timing Specifications[1][2] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $55°C \le T_C \le 125°C$

| Number | Characteristics | CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 166, 200 MHz | | 233, 266 MHz | | 300 MHz | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| 12 | SYSCLK to output driven (output enable time) | 1 | – | 1 | – | 1 | – | ns | |
| 13a | SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 9 | – | 9 | – | 9 | ns | (4) |
| 13b | SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 8 | – | 8 | – | 8 | ns | (6) |
| 14a | SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 11 | – | 11 | – | 11 | ns | (4) |
| 14b | SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 9 | – | 9 | – | 9 | ns | (6) |
| 15 | SYSCLK to output invalid (output hold) | 1 | – | 1 | – | 1 | – | ns | (3) |
| 16 | SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$) | – | 8.5 | – | 8 | – | 8 | ns | |
| 17 | SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge | – | 1 | – | 1 | – | 1 | $t_{SYSCLK}$ | (5)(7) |
| 18 | SYSCLK to $\overline{ARTRY}$ high impedance before precharge | – | 8 | – | 7.5 | – | 7.5 | ns | |
| 19 | SYSCLK to $\overline{ARTRY}$ precharge enable | 0.2 × $t_{SYSCLK}$ + 1 | – | 0.2 × $t_{SYSCLK}$ + 1 | – | 0.2 × $t_{SYSCLK}$ | – | ns | (3)(5) (8) |
| 20 | Maximum delay to $\overline{ARTRY}$ precharge | – | 1 | – | 1 | – | 1 | $t_{SYSCLK}$ | (5)(8) |
| 21 | SYSCLK to $\overline{ARTRY}$ high impedance after precharge | – | 2 | – | 2 | – | 2 | $t_{SYSCLK}$ | (6)(8) |

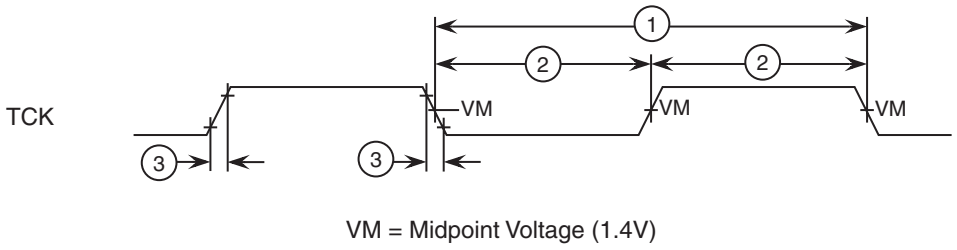
## 11.4 JTAG AC Timing Specifications

**Table 11-5.** JTAG AC Timing Specifications (independent of SYSCLK); $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $-55°C \le T_C \le 125°C$

| Number | Characteristics | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| | TCK frequency of operation | 0 | 16 | MHz | |
| 1 | TCK cycle time | 62.5 | – | ns | |
| 2 | TCK clock pulse width measured at 1.4V | 25 | – | ns | |
| 3 | TCK rise and fall times | 0 | 3 | ns | |
| 4 | $\overline{TRST}$ setup time to TCK rising edge | 13 | – | ns | (1) |
| 5 | $\overline{TRST}$ assert time | 40 | – | ns | |
| 6 | Boundary scan input data setup time | 6 | – | ns | (2) |
| 7 | Boundary scan input data hold time | 27 | – | ns | (2) |
| 8 | TCK to output data valid | 4 | 25 | ns | (3) |
| 9 | TCK to output high impedance | 3 | 24 | ns | (3) |
| 10 | TMS, TDI data setup time | 0 | – | ns | |
| 11 | TMS, TDI data hold time | 25 | – | ns | |
| 12 | TCK to TDO data valid | 4 | 24 | ns | |
| 13 | TCK to TDO high impedance | 3 | 15 | ns | |

Notes: 1. $\overline{TRST}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

**Figure 11-5.** Clock Input Timing Diagram




VM = Midpoint Voltage (1.4V)

**Figure 11-6.** $\overline{TRST}$ Timing Diagram

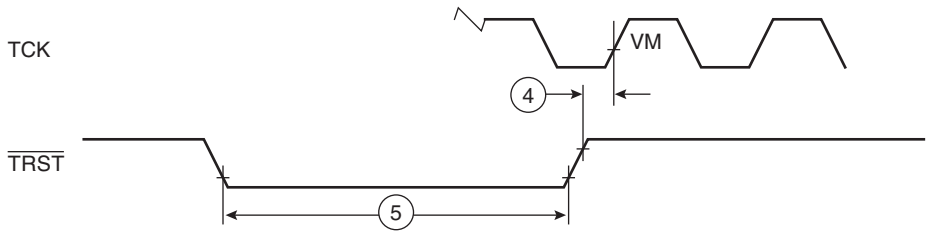


**Figure 11-7.** Boundary-scan Timing Diagram

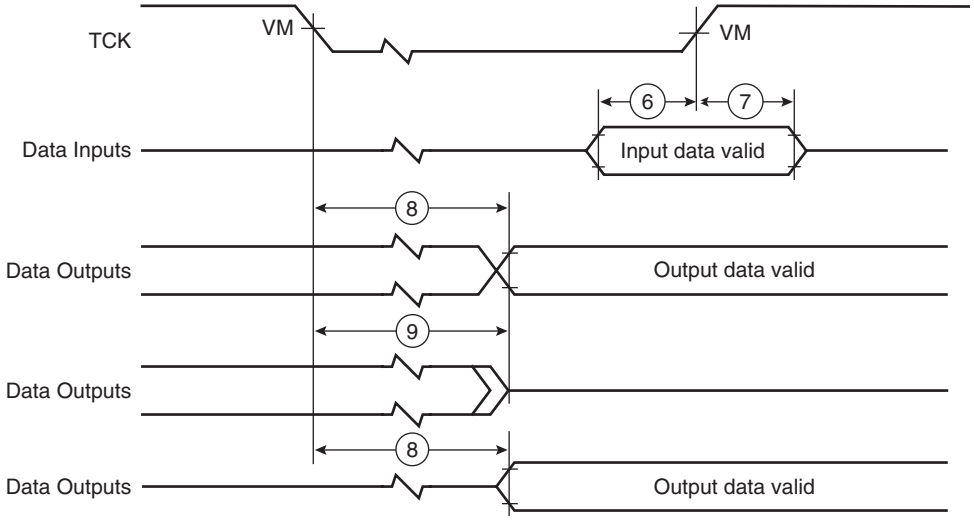
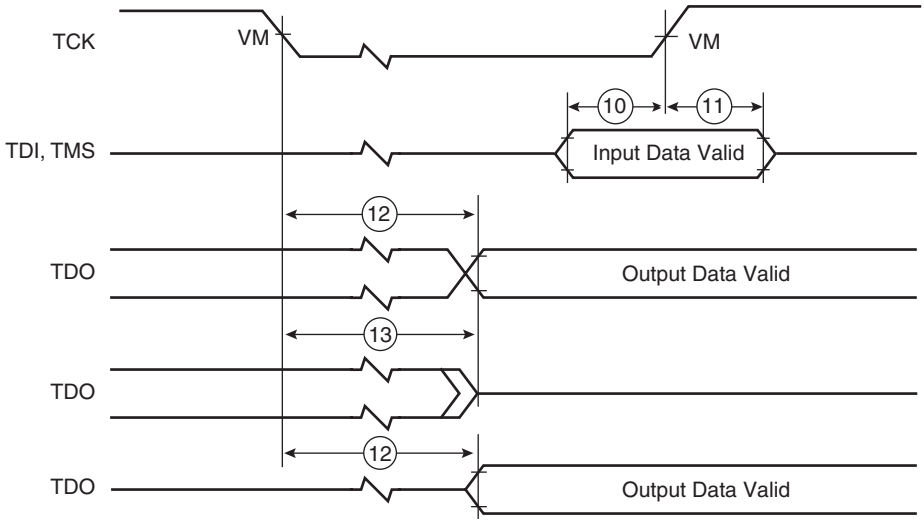



**Figure 11-8.** Test Access Port Timing Diagram




# 12. Functional Description

## 12.1 PowerPC Registers and Programming Model

The PowerPC architecture defines register-to-register operations for most computational instructions. Source operands for these instructions are accessed from the registers or are provided as immediate values embedded in the instruction opcode. The three-register instruction format allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory.

PowerPC processors have two levels of privilege—supervisor mode of operation (typically used by the operating system) and user mode of operation (used by the application software). The programming models incorporate 32 GPRs, 32 FPRs, Special-purpose Registers (SPRs) and several miscellaneous registers. Each PowerPC microprocessor also has its own unique set of Hardware Implementation (HID) registers.

Having access to privilege instructions, registers, and other resources allows the operating system to control the application environment (providing virtual memory and protecting operating system and critical machine resources). Instructions that control the state of the processor, the address translation mechanism, and supervisor registers can be executed only when the processor is operating in supervisor mode.

The following sections summarize the PowerPC registers that are implemented in the 603R.

### 12.1.1 General-purpose Registers (GPRs)

The PowerPC architecture defines 32 user-level, General-purpose Registers (GPRs). These registers are either 32 bits wide in 32-bit PowerPC microprocessors or 64 bits wide in 64-bit PowerPC microprocessors. The GPRs serve as the data source or destination for all integer instructions.

### 12.1.2 Floating-point Registers (FPRs)

The PowerPC architecture also defines 32 user-level, 64-bit Floating-point Registers (FPRs). The FPRs serve as the data source or destination for floating-point instructions. These registers can contain data objects of either single- or double-precision floating-point formats.

### 12.1.3 Condition Register (CR)

The CR is a 32-bit user-level register that consists of eight four-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

### 12.1.4 Floating-Point Status and Control Register (FPSCR)

The Floating-point Status and Control Register (FPSCR) is a user-level register that contains all exception signal bits, exception summary bits, exception enable bits, and rounding control bits needed for compliance with the IEEE 754 standard.

### 12.1.5 Machine State Register (MSR)

The Machine State Register (MSR) is a supervisor-level register that defines the state of the processor. The contents of this register are saved when an exception is taken and restored when the exception handling is completed. The 603R implements the MSR as a 32-bit register, 64-bit PowerPC processors implement a 64-bit MSR.

### 12.1.6 Segment Registers (SRs)

For memory management, 32-bit PowerPC microprocessors implement sixteen 32-bit Segment Registers (SRs). To speed access, the 603R implements the segment registers as two arrays; a main array (for data memory accesses) and a shadow array (for instruction memory accesses). Loading a segment entry with the Move to Segment Register (STSR) instruction loads both arrays.

### 12.1.7 Special-purpose Registers (SPRs)

The powerPC operating environment architecture defines numerous special-purpose registers that serve a variety of functions, such as providing controls, indicating status, configuring the processor, and performing special operations. During normal execution, a program can access the registers, shown in Figure 12-1 on page 32, depending on the program's access privilege (supervisor or user, determined by the privilege-level (PR) bit in the MSR. Note that registers such as the GPRs and FPRs are accessed through operands that are part of the instructions. Access to registers can be explicit (that is, through the use of specific instructions for that purpose such as Move to special-purpose register (**mtspr**) and move from special-purpose register (**mfspr**) instructions or implicit, as the part of the execution of an instruction. Some registers are accessed both explicitly and implicitly.

In the 603R, all SPRs are 32 bits wide.

- User-level SPRs:

  The following 603R SPRs are accessible by user-level software:

  – Link Register (LR) - The link register can be used to provide the branch target address and to hold the return address after branch and link instructions. The LR is 32 bits wide in 32-bit implementations.

  – Count Register (CTR) - The CRT is decremented and tested automatically as a result of branch-and-count instructions. The CTR is 32 bits wide in 32-bit implementations.

  – Integer Exception Register (XER) - The 32-bit XER contains the summary overflow bit, integer carry bit, overflow bit, and a field specifying the number of bytes to be transferred by a Load String Word Indexed (LSWX) or Store String Word Indexed (STSWX) instruction.

- Supervisor-level SPRs:

The 603R also contains SPRs that can be accessed only by supervisor-level software. These registers consist of the following:

  – The 32-bit DSISR defines the cause of data access and alignment exceptions.

  – The Data Address Register (DAR) is a 32-bit register that holds the address of an access after an alignment or DSI exception.

  – Decrementer register (DEC) is a 32-bit decrementing counter that provides a mechanism for causing a decrementer exception after a programmable delay.

  – The 32-bit SDR1 specifies the page table format used in virtual-to-physical address translation for pages. (Note that physical address is referred to as real address in the architecture specification).

  – The machine status Save/Restore Register 0 (SRR0) is a 32-bit register that is used by the 603R for saving the address of the instruction that caused the exception, and the address to return to when a Return from Interrupt (**RFI**) instruction is executed.

  – The machine status Save/Restore Register 1 (SRR1) is a 32-bit register used to save machine status on exceptions and to restore machine status when an **RFI** instruction is executed.

  – The 32-bit SPRG0-SPRG3 registers are provided for operating system use.

  – The External Access Register (EAR) is a 32-bit register that controls access to the external control facility through the External Control In Word Indexed (**ECIWX**) and External Control Out Word Indexed (**ECOWX**) instructions.

### 12.2.2 PowerPC 603R Microprocessor Instruction Set

The 603R instruction set is defined as follows:

- The 603R provides hardware support for all 32-bit PowerPC instructions.
- The 603R provides two implementation-specific instructions used for software table search operations following TLB misses:
  - Load Data TLB Entry (**tlbld**)
  - Load Instruction TLB Entry (**tlbli**)
- The 603R implements the following instructions which are defined as optional by the PowerPC architecture :
  - External Control in Word Indexed (**eciwx**)
  - External Control Out Word Indexed (**ecowx**)
  - Floating Select (**fsed**)
  - Floating Reciprocal Estimate Single-Precision (**fres**)
  - Floating Reciprocal Square Root Estimate (**frsqrte**)
  - Store Floating-Point as Integer Word (**stfiwx**)

## 12.3 Cache Implementation

The following subsections describe the way the PowerPC architecture deals with cache in general, and the 603R's specific implementation.

### 12.3.1 PowerPC Cache Characteristics

The PowerPC architecture does not define hardware aspects of cache implementations. For example, some PowerPC processors, including the 603R, have separate instruction and data caches (harvard architecture).

The PowerPC microprocessor controls the following memory access modes on a page or block basis:

- Write-back/write-through mode
- Cache-inhibited mode
- Memory coherency

Note that in the 603R, a cache line is defined as eight words. The VEA defines cache management instructions that provide a means by which the application programmer can affect the cache contents.

### 12.3.2 PowerPC 603R Microprocessor Cache Implementation

The 603R has two 16-Kbyte, four-way set-associative (instruction and data) caches. The caches are physically addressed, and the data cache can operate in either write-back or write-through modes as specified by the PowerPC architecture.

The data cache is configured as 128 sets of four lines each. Each line consists of 32 bytes, two state bits, and an address tag. The two state bits implement the three-state MEI (Modified/Exclusive/Invalid) protocol. Each line contains eight 32-bit words. Note that the PowerPC architecture defines the term block as the cacheable unit. For the 603R, the block size is equivalent to a cache line. A block diagram of the data cache organization is shown in Figure 12-2 on page 36.

**Table 12-2.** Exceptions and Conditions (Continued)

| Exception Type | Vector Offset (hex) | Causing Conditions |
|---|---|---|
| Instruction address breakpoint | 01300 | An instruction address breakpoint exception occurs when the address (bits 0-29) in the IABR matches the next instruction to complete in the completion unit, and the IABR enable bit (bit 30) is set to 1 |
| System management interrupt | 01400 | A system management interrupt is caused when MSR[EE] = 1 and the $\overline{\text{SMI}}$ input signal is asserted |
| Reserved | 01500–02FFF | – |

## 12.4 Memory Management

The following subsections describe the memory management features of the PowerPC architecture, and the 603R implementation, respectively.

### 12.4.1 PowerPC Memory Management

The primary functions of the MMU are to translate logical (effective) addresses to physical addresses for memory accesses, and to provide access protection on blocks and pages of memory.

There are two types of accesses generated by the 603R that require address translation — instruction accesses, and data accesses to memory generated by load and store instructions.

The PowerPC MMU and exception model support demand-paged virtual memory. Virtual memory management permits execution of programs larger than the size of physical memory; demand-paged implies that individual pages are loaded into physical memory from system memory only when they are first accessed by an executing program.

The hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

The page table contains a number of Page Table Entry Groups (PTEGs). A PTEG contains eight Page Table Entries (PTEs) of eight bytes each; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

Address translations are enabled by setting bits in the MSR-MSR[IR] enables instruction address translations and MSR[DR] enables data address translations.

### 12.4.2 PowerPC 603R Microprocessor Memory Management

The instruction and data memory management units in the 603R provide 4 Gbytes of logical address space accessible to the supervisor and user programs with a 4 Kbyte page size and 256M byte segment size. Block sizes range from 128 Kbytes to 256 Mbytes and are software selectable. In addition, the 603R uses an interim 52-bit virtual address and hashed page tables for generating 32-bit physical addresses. The MMUs in the 603R rely on the exception processing mechanism for the implementation of the paged virtual memory environment and for enforcing protection of designated memory areas.

Instruction and data TLBs provide address translation in parallel with the on-chip cache access, incurring no additional time penalty in the event of a TLB hit. A TLB is a cache of the most recently used page table entries. The software is responsible for maintaining the consistency of the TLB with memory.

The 603R's TLBs are 64-entry, 2-way set-associative caches that contain instruction and data address translations. The 603R provides hardware assistance for software table search operations through the ashed page table on the TLB misses. The supervisor software can invalidate TLB entries selectively.

The 603R also provides independent four-entry BAT arrays for instructions and data that maintain address translations for blocks of memory. These entries define blocks that can vary from 128 Kbytes to 256 Mbytes. The BAT arrays are maintained by system software.

As specified by the PowerPC architecture, the hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

Also as specified by the PowerPC architecture, the page table contains a number of Page Table Entry Groups (PTEGs). A PTEG contains eight Page Table Entries (PTEs) of eight bytes each; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

### 12.4.3 Instruction Timing

The 603R is a pipelined superscalar processor. A pipelined processor is one in which the processing of an instruction is reduced into discrete stages. Because the processing of an instruction is broken into a series of stages, an instruction does not require the entire resources of an execution unit. For example, after an instruction completes the decode stage, it can pass on to the next stage, while the subsequent instruction can advance into the decode stage. This improves the throughput of the instruction flow. For example, it may take three cycles for a floating-point instruction to complete, but if there are no stalls in the floating-point pipeline, a series of floating-point instructions can have a throughput of one instruction per cycle.

The instruction pipeline in the 603R has four major pipeline stages, described as follows:

- The fetch pipeline stage primarily involves retrieving instructions from the memory system and determining the location of the next instruction retrieval. Additionally, the BPU decodes branches during the fetch stage and folds out branch instructions before the dispatch stage if possible.
- The dispatch pipeline stage is responsible for decoding the instructions supplied by the instruction retrieval stage, and determining which of the instructions are eligible to be dispatched in the current cycle. In addition, the source operands of the instructions are read from the appropriate register file and dispatched with the instruction to the execute pipeline stage. At the end of the dispatch pipeline stage, the dispatched instructions and their operands are latched by the appropriate execution unit.
- During the execute pipeline stage each execution unit that has an executable instruction executes the selected instruction (perhaps over multiple cycles), writes the instruction's result into the appropriate rename register, and notifies the completion stage when the instruction has finished execution. In the case of an internal exception, the execution unit reports the exception to the completion/writeback pipeline stage and discontinues instruction execution until the exception is handled. The exception is not signaled until that instruction is the next to be completed. Execution of most floating-point instructions is pipelined within the FPU allowing up to three instructions to be executing in the FPU concurrently. The pipeline stages for the floating-point unit are multiply, add, and round-convert. Execution of most load/store instructions is also pipelined. The load/store unit has two pipeline stages. The first stage is for effective address calculation and MMU translation and the second stage is for accessing the data in the cache.

In Table 13-1, the horizontal scale represents the bus frequency (SYSCLK) and the vertical scale represents the PLL-CFG[0-3] signals.

For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation.

**Table 13-1.** CPU Frequencies for Common Bus Frequencies and Multipliers

| PLL_CFG[0-3] | CPU Frequency in MHZ (VCO Frequency in MHz) specific to CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Bus-to-Core Multiplier | Core-to VCO Multiplier | Bus 25 MHz | Bus 33.33 MHz | Bus 40 MHz | Bus 50 MHz | Bus 60 MHz | Bus 66.67 MHz | Bus 75 MHz |
| 0100 | 2x | 2x | - | - | - | - | - | - | 150 (300) |
| 0101 | 2x | 4x | - | - | - | - | - | - | - |
| 0110 | 2.5x | 2x | - | - | - | - | 150 (300) | 166 (333) | 187 (375) |
| 1000 | 3x | 2x | - | - | - | 150 (300) | 180 (360) | 200 (400) | 225 (450) |
| 1110 | 3.5x | 2x | - | - | - | 175 (350) | 210 (420) | 233 (466) | 263 (525) |
| 1010 | 4x | 2x | - | - | 160 (320) | 200 (400) | 240 (480) | 267 (533) | 300 (600) |
| 0111 | 4.5x | 2x | - | 150 (300) | 180 (360) | 225 (450) | 270 (540) | 300 (600) | - |
| 1011 | 5x | 2x | - | 166 (333) | 200 (400) | 250 (500) | 300 (600) | - | - |
| 1001 | 5.5x | 2x | - | 183 (366) | 220 (440) | 275 (550) | - | - | - |
| 1101 | 6x | 2x | 150 (300) | 200 (400) | 240 (480) | 300 (600) | - | - | - |
| 0011 | PLL bypass | | | | | | | | |
| 1111 | Clock off | | | | | | | | |

| PLL_CFG[0-3] | CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Bus-to-Core Multiplier | Core-to VCO Multiplier | Bus 25 MHz | Bus 33.33 MHz | Bus 40 MHz | Bus 50 MHz | Bus 60 MHz | Bus 66.67 MHz |
| 0100 | 2x | 2x | – | – | – | – | – | – |
| 0101 | 2x | 4x | – | – | – | – | – | – |
| 0110 | 2.5x | 2x | – | – | – | – | 150 (300) | 166 (333) |
| 1000 | 3x | 2x | – | – | – | 150 (300) | 180 (360) | 200 (400) |
| 1110 | 3.5x | 2x | – | – | – | 175 (350) | – | – |

| PLL_CFG[0-3] | CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Bus-to-Core Multiplier | Core-to VCO Multiplier | Bus 25 MHz | Bus 33.33 MHz | Bus 40 MHz | Bus 50 MHz | Bus 60 MHz | Bus 66.67 MHz |
| 1010 | 4x | 2x | – | – | 160 (320) | 200 (400) | – | – |
| 0111 | 4.5x | 2x | – | 150 (300) | 180 (360) | – | – | – |
| 1011 | 5x | 2x | – | 166 (333) | 200 (400) | – | – | – |
| 1001 | 5.5x | 2x | – | 183 (366) | – | – | – | – |
| 1101 | 6x | 2x | 150 (300) | 200 (400) | – | – | – | – |
| 0011 | PLL bypass | | | | | | | |
| 1111 | Clock off | | | | | | | |

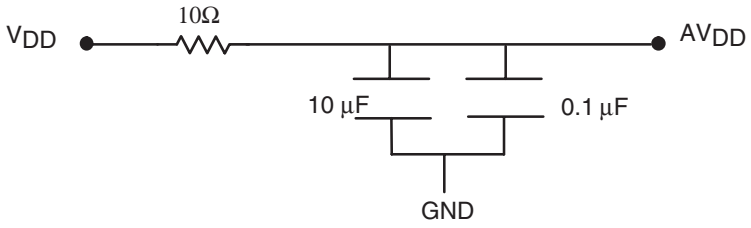
Notes: 1. Some PLL configurations may select bus, CPU or VCO frequencies which are not supported.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
The AC timing specifications given in this document do not apply in PLL-bypass mode.
3. In clock-off mode, no clocking occurs inside the 603e regardless of the SYSCLK input.

# 14. System Design Information

## 14.1 PLL Power Supply Filtering

The $AV_{DD}$ power signal is implemented on the 603e to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the $AV_{DD}$ input signal should be filtered using a circuit similar to the one shown in Figure 14-1. The circuit should be placed as close as possible to the $AV_{DD}$ pin to ensure it filters out as much noise as possible. The 0.1 µF capacitor should be closest to the $AV_{DD}$ pin, followed by the 10 µF capacitor, and finally the 10Ω resistor to $V_{DD}$. These traces should be kept short and direct.

**Figure 14-1.** PLL Power Supply Filter Circuit



## 14.2 Decoupling Recommendations

Due to the 603e's dynamic power management feature, large address and data buses, and high operating frequencies, the 603e can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 603e system, and the 603e itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$ and $OV_{DD}$ pin of the 603e. It is also recommended that these decoupling capacitors receive their power from separate $V_{DD}$, $OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 µF to provide both high and low frequency filtering, and should be placed as close as possible to their associated $V_{DD}$ or $OV_{DD}$ pin. The suggested values for the $V_{DD}$ pins are 220 pF (ceramic), 0.01 µF (ceramic) and 0.1 µf (ceramic). The suggested values for the $OV_{DD}$ pins are 0.01 µF (ceramic), 0.1 µF (ceramic), and 10 µF (tantalum). Only SMT (Surface Mount Technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $V_{DD}$ and $OV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should also have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. The suggested bulk capacitors are 100 µF (AVX TPS tantalum) or 330 µf (AVX TPS tantalum).

## 14.3 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to $V_{DD}$. Unused active high inputs should be connected to GND. All NC (non-connected) signals must remain unconnected.

Power and ground connections must be made to all external $V_{DD}$, $OV_{DD}$, and GND pins of the 603e.

## 14.4 Pull-up Resistor Requirements

The 603e requires high-resistive (weak: 10 kΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the 603e or other bus master. These signals are: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$.

In addition, the 603e has three open-drain style outputs that require pull-up resistors (weak or stronger: 4.7 kΩ - 10 kΩ) if they are used by the system. These signals are: $\overline{APE}$, $\overline{DPE}$, and $\overline{CKSTP\_OUT}$.

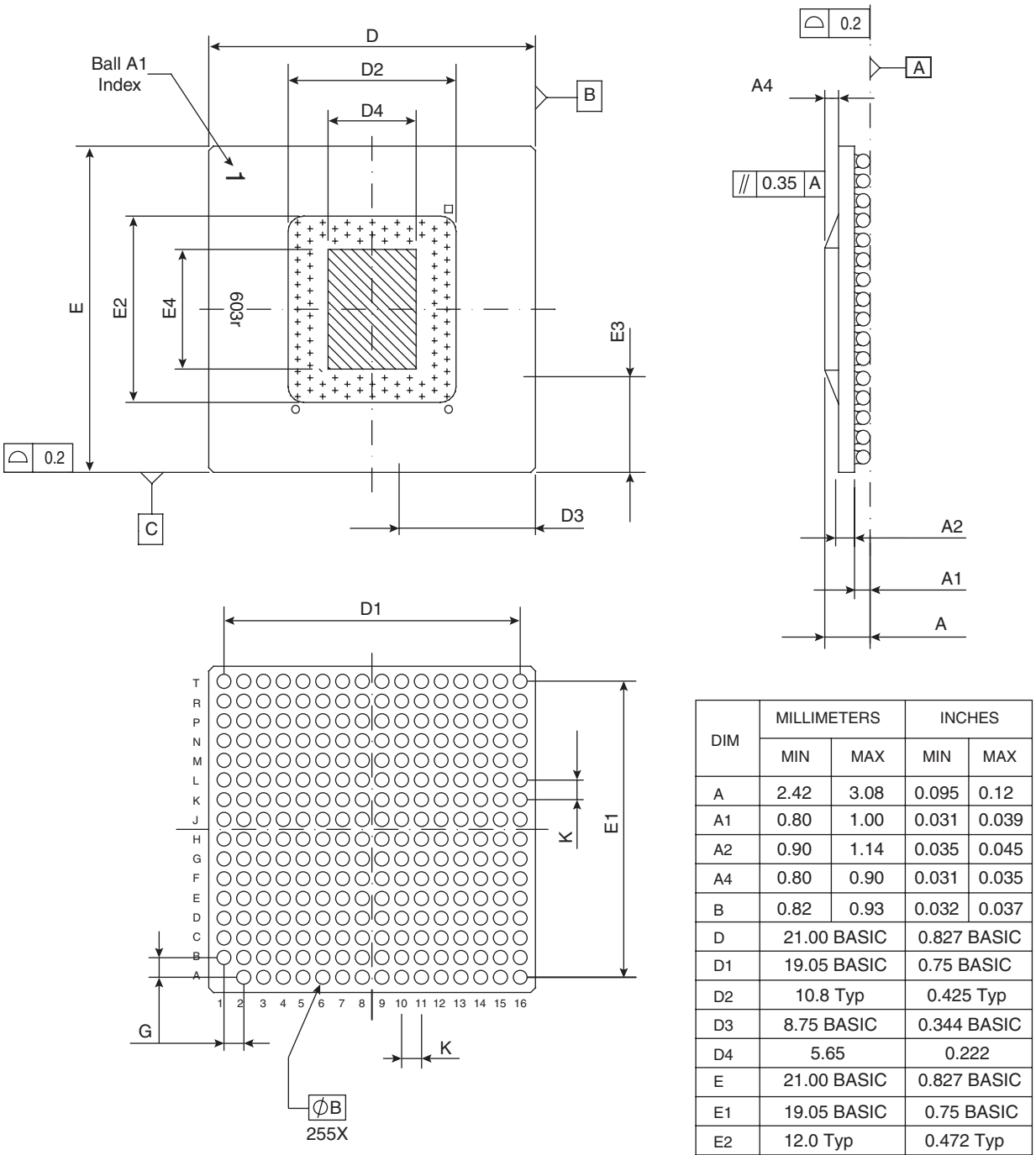
During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the 603e must continually monitor these signals for snooping, this floating condition may cause excessive power to be drawn by the input revivers on the 603e. It is recommended that these signals be pulled up through weak (10 kΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are: A[0-3], AP[0-3], TT[0-4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

### 15.1.1 Mechanical Dimensions of the HiTCE CBGA Package

Figure 15-1 provides the mechanical dimensions and bottom surface nomenclature of the HiTCE CBGA package.

**Figure 15-1.** Mechanical Dimensions of the HiTCE CBGA Package




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.42 | 3.08 | 0.095 | 0.12 |
| A1 | 0.80 | 1.00 | 0.031 | 0.039 |
| A2 | 0.90 | 1.14 | 0.035 | 0.045 |
| A4 | 0.80 | 0.90 | 0.031 | 0.035 |
| B | 0.82 | 0.93 | 0.032 | 0.037 |
| D | 21.00 BASIC | | 0.827 BASIC | |
| D1 | 19.05 BASIC | | 0.75 BASIC | |
| D2 | 10.8 Typ | | 0.425 Typ | |
| D3 | 8.75 BASIC | | 0.344 BASIC | |
| D4 | 5.65 | | 0.222 | |
| E | 21.00 BASIC | | 0.827 BASIC | |
| E1 | 19.05 BASIC | | 0.75 BASIC | |
| E2 | 12.0 Typ | | 0.472 Typ | |
| E3 | 6.15 BASIC | | 0.242 BASIC | |
| E4 | 7.7 | | 0.303 | |
| G, K | 1.27 BASIC | | 0.05 BASIC | |

## 15.2 CBGA Package Parameters

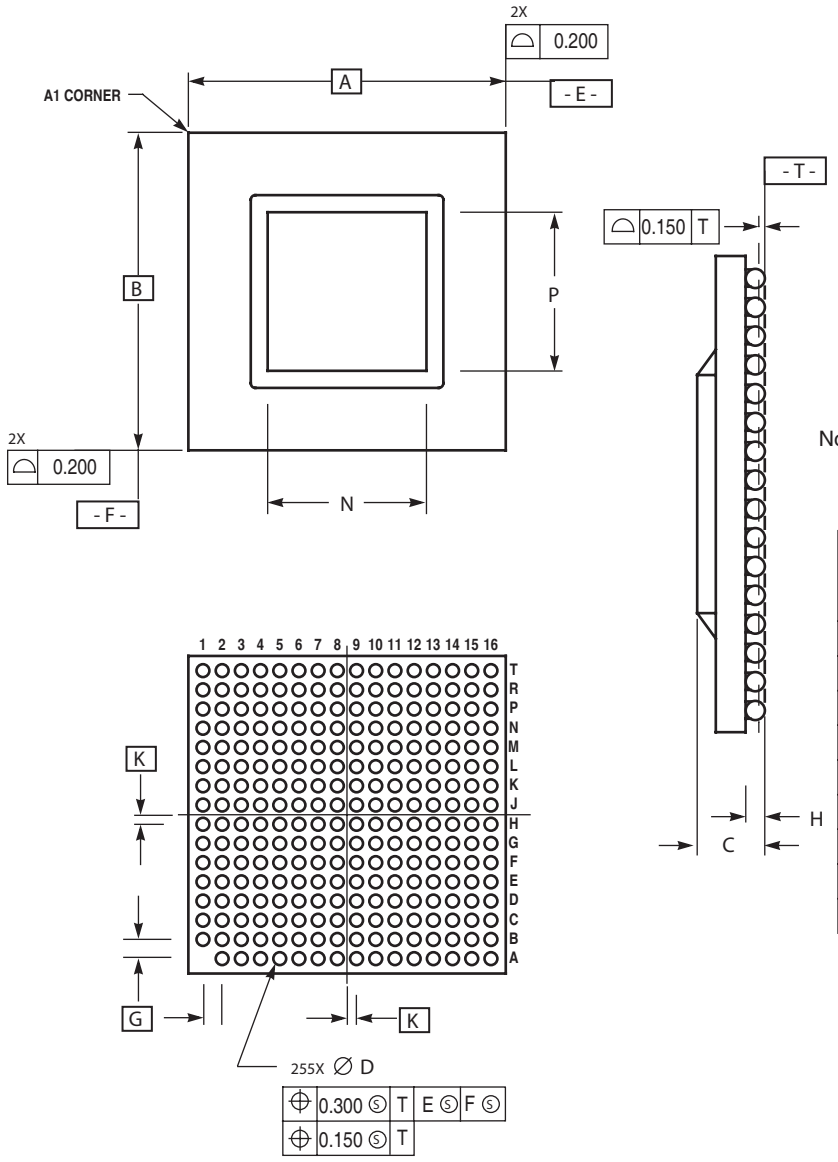
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead Ceramic Ball Grid Array (CBGA).

| | |
|---|---|
| Package outline | 21 mm × 21 mm |
| Interconnects | 255 |
| Pitch | 1.27 mm |
| Maximum module height | 3 mm |

### 15.2.1 Mechanical Dimensions of the CBGA Package

Figure 15-2 provides the mechanical dimensions and bottom surface nomenclature of the CBGA package.

**Figure 15-2.** Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package




Notes: 1. Dimensioning and tolerancing per ASME Y14.5M - 1994
2. controlling dimension: millimeter

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 21.000 BSC | | 0.827 BSC | |
| B | 21.000 BSC | | 0.827 BSC | |
| C | 2.450 | 3.000 | 0.097 | 0.118 |
| D | 0.820 | 0.930 | 0.032 | 0.036 |
| G | 1.270 BSC | | 0.050 BSC | |
| H | 0.790 | 0.990 | 0.031 | 0.039 |
| K | 0.635 BSC | | 0.025 BSC | |
| N | 5.000 | 16.000 | 0.197 | 0.630 |
| P | 5.000 | 16.000 | 0.197 | 0.630 |

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