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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	255-BCBGA Exposed Pad
Supplier Device Package	255-CI-CBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgs8lc

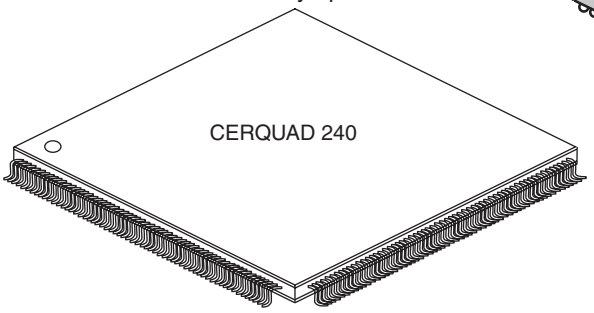
The 603R uses an advanced, 2.5/3.3V CMOS process technology and maintains full interface compatibility with TTL devices. It also integrates in-system testability and debugging features through JTAG boundary-scan capabilities.

2. Screening/Quality/Packaging

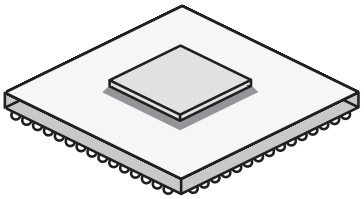
This product is manufactured in full compliance with:

- HiTCE CBGA according to Atmel Standards
- CI-CGA 255 and Cerquad: MIL-PRF-38535 class Q or according to Atmel standards
- CBGA 255: Upscreenings based upon Atmel standards
- CBGA, CI-CGA, HiTCE packages:
  - Full military temperature range (T_C = -55°C, T_j = +125°C)
  - Industrial temperature range (T_C = -40°C, T_j = +110°C)
- Cerquad:
  - Full military temperature range (T_C = -55°C, T_c = +125°C)
  - Industrial temperature range (T_C = -40°C, T_c = +110°C)
  - Commercial temperature ranges (T_C = 0°C, T_C = +70°C)
- Internal I/O Power Supply = 2.5 ±5% // 3.3V ±5%

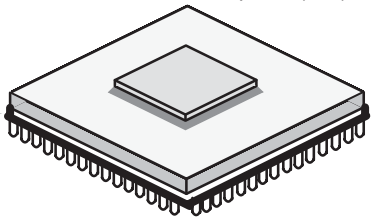
A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier
Cavity up



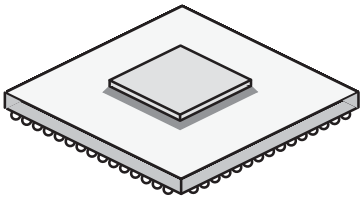
G suffix
CBGA 255
Ceramic Ball Grid Array



GS suffix
CI-CGA 255
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)



GH suffix
HiTCE 255
Ceramic Ball Grid Array



- a Load/Store Unit (LSU)
- a System Register Unit (SRU)

The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603R-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603R provides independent on-chip, 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data, as well as on-chip instruction and data Memory Management Units (MMUs). The MMUs contain 64-entry, two-way set-associative, Data and Instruction Translation Lookaside Buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a Least Recently Used (LRU) replacement algorithm. The 603R also supports block address translation through the use of two independent Instruction and Data Block Address Translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation has priority.

The 603R has a selectable 32- or 64-bit data bus and a 32-bit address bus. The 603R interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603R provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (Modified/Exclusive/Shared/Invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603R supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/Os.

The 603R uses an advanced, 0.29 µm 5-metal-layer CMOS process technology and maintains full interface compatibility with TTL devices.

5. Signal Description

Figure 5-1 on page 5, Table 10-5 and Table 10-6 on page 20 describe the signals on the TSPC603R and indicate signal functions. The test signals, $\overline{\text{TRST}}$, TMS, TCK, TDI and TDO, comply with the subset P-1149.1 of the IEEE testability bus standard.

The three signals $\overline{\text{LSSD\_MODE}}$, LI_TSTCLK and L2_TSTCLK are test signals for factory use only and must be pulled up to V_{DD} for normal machine operations.

7.1 Design and Construction

7.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 10-2 on page 15, Table 10-4 on page 18, "Recommended Operating Conditions" on page 6, Figure 15-2 on page 49, Figure 15-4 on page 52 and Figure 5-1 on page 5.

7.1.2 *Lead Material and Finish*

Lead material and finish shall be as specified in MIL-STD-1835. (See "Package Mechanical Data" on page 47.)

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only and functional operation at the maximum is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

7.2.1 Absolute Maximum Ratings for the 603R(1)(2)(3)

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	-0.3	2.75	V
PLL supply voltage	AV_{DD}	-0.3	2.75	V
I/O supply voltage	OV_{DD}	-0.3	3.6	V
Input voltage	V_{IN}	-0.3	5.5	V
Storage temperature range	T_{STG}	-55	+150	°C

Notes:
1. **Caution**: The input voltage must not be greater than OV_{DD} by more than 2.5V at any time, including during power-on reset.
2. **Caution**: The OV_{DD} voltage must not be greater than V_{DD}/AV_{DD} by more than 1.2V at any time, including during power-on reset.
3. **Caution**: The V_{DD}/AV_{DD} voltage must not be greater than OV_{DD} by more than 0.4V at any time, including during power-on reset.

Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

7.2.2 Recommended Operating Conditions

The following are the recommended and tested operating conditions. Proper device operation outside of these ranges is not guaranteed.

7.2.3 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	2.375	2.625	V
PLL supply voltage	AV_{DD}	2.375	2.625	V
I/O supply voltage	OV_{DD}	3.135	3.465	V
Input voltage	V_{IN}	GND	5.5	V
Operating temperature	T_c	-55	+125	°C
Junction operating temperature specific to Cerquad	T_j	–	+135	°C

10.2.1 Pinout Listing

Table 10-3. Power and Ground Pins

	CERQUAD Pin Number	
	VCC	**GND**
PLL (AV_{DD})	209	
Internal Logic	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239
Output Drivers	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238

Table 10-4. Signal Pinout Listing

Signal Name	CERQUAD Pin Number
A[0-31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37
$\overline{\text{AACK}}$	28
$\overline{\text{ABB}}$	36
AP[0-3]	231,230,227,226
$\overline{\text{APE}}$	218
$\overline{\text{ARTRY}}$	32
$\overline{\text{BG}}$	27
$\overline{\text{BR}}$	219
$\overline{\text{CI}}$	237
$\overline{\text{CKSTP\_IN}}$	215
$\overline{\text{CKSTP\_OUT}}$	216
CLK_OUT	221
CSE[0-1]	225,150
$\overline{\text{DBB}}$	145
$\overline{\text{DBG}}$	26
$\overline{\text{DBDIS}}$	153
$\overline{\text{DBWO}}$	25
DH[0-31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66
DL[0-31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64
DP[0-7]	38, 40, 41, 42, 46, 47, 48, 50
$\overline{\text{DPE}}$	217
$\overline{\text{DRTRY}}$	156
$\overline{\text{GBL}}$	1
$\overline{\text{HRESET}}$	214

Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

Signal Name	Abbreviation	Signal Function	Signal Type
Global	$\overline{\text{GBL}}$	If output, a transaction is global If input, a transaction must be snooped by the 603R	I/O
Hard Reset	$\overline{\text{HRESET}}$	Initiates a complete hard reset operation	Input
Interrupt	$\overline{\text{INT}}$	Initiates an interrupt if bit EE of MSR register is set	Input
Factory Test	$\overline{\text{LSSD\_MODE}}$	LSSD test control signal for factory use only	Input
	L1_TSTCLK	LSSD test control signal for factory use only	Input
	L2_TSTCLK	LSSD test control signal for factory use only	Input
Machine Check Interrupt	$\overline{\text{MCP}}$	Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set	Input
PLL Configuration	PLL_CFG[0-3]	Configures the operation of the PLL and the internal processor clock frequency	Input
Power supply indicator	VOLTDETGND	Available only on BGA package Indicates to the power supply that a low-voltage processor is present.	Output
Quiescent Acknowledge	$\overline{\text{QACK}}$	All bus activity has terminated and the 603R may enter a quiescent (or low power) state	Input
Quiescent Request	$\overline{\text{QREQ}}$	Is requesting all bus activity normally to enter a quiescent (low power) state	Output
Reservation	$\overline{\text{RSRV}}$	Represents the state of the reservation coherency bit in the reservation address register	Output
System Management Interrupt	$\overline{\text{SMI}}$	Initiates a system management interrupt operation if the bit EE of MSR register is set	Input
Soft Reset	$\overline{\text{SRESET}}$	Initiates processing for a reset exception	Input
System Clock	SYSCLK	Represents the primary clock input for the 603R, and the bus clock frequency for 603R bus operation	Input
Test Clock	CLK_OUT	Provides PLL clock output for PLL testing and monitoring	Output
Transfer Acknowledge	$\overline{\text{TA}}$	A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully	Input
Timebase Enable	TBEN	The timebase should continue clocking	Input
Transfer Burst	$\overline{\text{TBST}}$	If output, a burst transfer is in progress If input, when snooping for single-beat reads	I/O
Transfer Code	TC[0-1]	Special encoding for the transfer in progress	Output
Test Clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)	Input
Test Data Input	TDI	Serial data input for the TAP	Input
Test Data Output	TDO	Serial data output for the TAP	Output
Transfer Error Acknowledge	$\overline{\text{TEA}}$	A bus error occurred	Input
TLBI Sync	$\overline{\text{TLBISYNC}}$	Instruction execution should stop after execution of a **tlbsync** instruction	Input
Test Mode Select	TMS	Selects the principal operations of the test-support circuitry	Input
Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset of the TAP controller	Input
Transfer Size	TSIZ[0-2]	For memory accesses, these signals along with $\overline{\text{TBST}}$ indicate the data transfer size for the current bus operation	I/O

Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

Signal Name	Abbreviation	Signal Function	Signal Type
Transfer Start	$\overline{TS}$	If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$)	I/O
Transfer Type	TT[0-4]	Type of transfer in progress	I/O
Write-through	$\overline{WT}$	A single-beat transaction is write-through	Output

11. Electrical Characteristics

11.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 11-1: Static electrical characteristics for the electrical variants
- Table 11-2: Dynamic electrical characteristics for the 603R

The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0 to PLL_CFG3 signals. All timings are respectively specified to the rising edge of SYSCLK.

These specifications are for 166 MHz to 300 MHz processor core frequencies for CBGA 255, HiTCE CBGA 255 and CI-CGA 255 packages and 166 MHz to 200 MHz processor core frequencies for the Cerquad 240 package.

11.2 Static Characteristics

Table 11-1. Electrical Characteristics with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Characteristics		Symbol	Min	Max	Unit
Input High Voltage (all inputs except SYSCLK)		V_{IH}	2	5.5	V
Input Low Voltage (all inputs except SYSCLK)		V_{IL}	GND	0.8	V
SYSCLK Input High Voltage		CV_{IH}	2.4	5.5	V
SYSCLK Input Low Voltage		CV_{IL}	GND	0.4	V
Input Leakage Current	V_{IN} = 3.465V(1)(3)	I_{IN}	-	30	µA
	V_{IN} = 5.5V(1)(3)	I_{IN}	-	300	µA
Hi-Z (off-state) Leakage Current	V_{IN} = 3.465V(1)(3)	I_{TSI}	-	30	µA
	V_{IN} = 5.5V(1)(3)	I_{TSI}	-	300	µA
Output High Voltage	I_{OH} = -7 mA	V_{OH}	2.4	-	V
Output Low Voltage	I_{OL} = +7 mA	V_{OL}	-	0.4	V
Capacitance, V_{IN} = 0V, f = 1 MHz(2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{IN}	-	10	pF
Capacitance, V_{IN} = 0V, f = 1 MHz(2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{IN}	-	15	pF

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100% tested.

3. Leakage currents are measured for nominal OV_{DD} and V_{DD} or both OV_{DD} and V_{DD}. Same variation (for example, both V_{DD} and OV_{DD} vary by either +5% or -5%)

11.3 Dynamic Characteristics

11.3.1 Clock AC Specifications

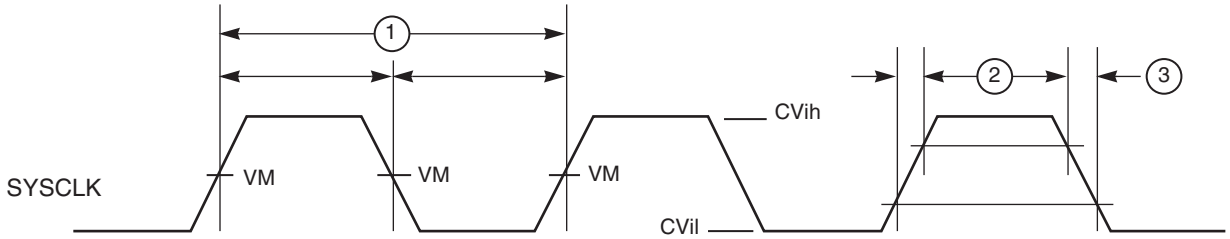
Table 11-2 provides the clock AC timing specifications as defined in Figure 11-1.

Table 11-2. Clock AC Timing Specifications[1][2][3][4] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Figure Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and CERQUAD				CBGA 255, HiTCE CBGA 255 and CI-CGA 255							
		166 MHz		200 MHz		233 MHz		266 MHz		300 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
	Processor Frequency	150	166	150	200	180	233	180	266	180	300	MHz	[5]
	VCO Frequency	300	332	300	400	360	466	360	532	360	600	MHz	[5]
	SYSCLK (bus) Frequency	25	66.7	33.3	66.7	33.3	75	33.3	75	33.3	75	MHz	[5]
1	SYSCLK Cycle Time	15	30	13.3	30	13.3	30	13.3	30	13.3	30	ns	
2,3	SYSCLK Rise and Fall Time	–	2	–	2	–	2	–	2	–	2	ns	[1]
4	SYSCLK Duty Cycle (1.4V measured)	40	60	40	60	40	60	40	60	40	60	%	[3]
	SYSCLK Jitter	–	±150	–	±150	–	±150	–	±150	–	±150	ps	[2]
	603R Internal PLL Relock Time	–	100	–	100	–	100	–	100	–	100	µs	[3][4]

Notes:
1. Rise and fall times for the SYSCLK input are measured from 0.4V to 2.4V.
2. Cycle-to-cycle jitter is guaranteed by design.
3. Timing is guaranteed by design and characterization and is not tested.
4. The PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD}, OV_{DD}, AV_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen so that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description for valid PLL_CFG[0-3] settings.

Figure 11-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage (1.4V)

11.3.2 Input AC Specifications

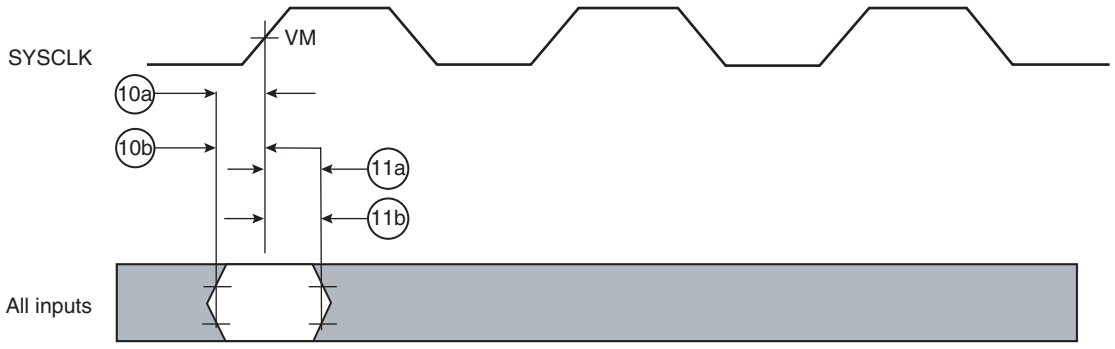
Table 11-3 provides the input AC timing specifications for the 603R as defined in Figure 11-2 and Figure 11-3.

Table 11-3. Input AC Timing Specifications[1] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Figure Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages		CBGA 255, HiTCE CBGA 255 and CI-CGA 255				Unit	Note
		166, 200 MHz		233, 266 MHz		300 MHz			
		Min	Max	Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	2.5	–	2.5	–	2.5	–	ns	(2)
10b	All other inputs valid to SYSCLK (input setup)	4	–	3.5	–	3.5	–	ns	(3)
10c	Mode select inputs valid to $\overline{HRESET}$ (input setup) (for $\overline{DRTRY}$, $\overline{QACK}$ and $\overline{TLBISYNC}$)	8	–	8	–	8	–	t_{sysclk}	(4)(5)(6)(7)
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1	–	1	–	1	–	ns	(2)
11b	SYSCLK to all other inputs invalid (input hold)	1	–	1	–	1	–	ns	(3)
11c	$\overline{HRESET}$ to mode select inputs invalid (input hold) (for $\overline{DRTRY}$, $\overline{QACK}$, and $\overline{TLBISYNC}$)	0	–	0	–	0	–	ns	(4)(6)(7)

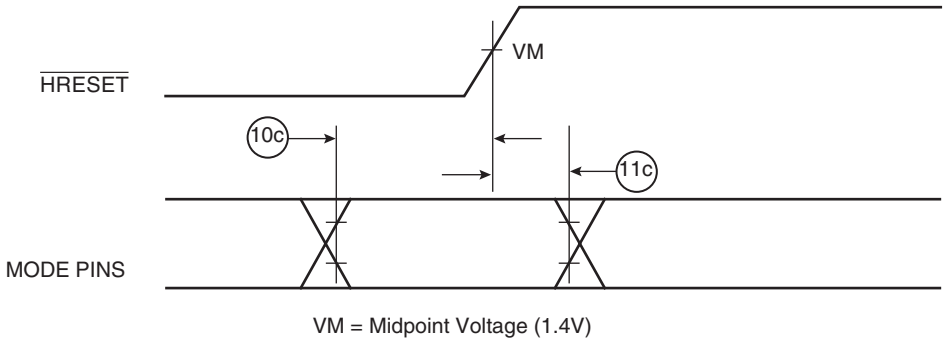
Notes:
1. All input specifications are measured from the TTL level (0.8 or 2V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 11-3.
2. Address/data/transfer attribute input signals are composed of the following: A[0-31], AP[0-3], TT[0-4], TC[0-1], $\overline{TBST}$, TSIZ[0-2], $\overline{GBL}$, DH[0-31], DL[0-31], DP[9-7].
3. All other input signals are composed of the following: $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{AACK}$, $\overline{DBG}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{DRTRY}$, $\overline{TEA}$, $\overline{DBDIS}$, $\overline{HRESET}$, $\overline{SRESET}$, $\overline{INT}$, $\overline{SMI}$, $\overline{MCP}$, TBEN, $\overline{QACK}$, $\overline{TLBISYNC}$.
4. The setup and hold time is with respect to the rising edge of $\overline{HRESET}$. See Figure 11-3.
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode only. Also note that $\overline{HRESET}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.

Figure 11-2. Input Timing Diagram



VM = Midpoint Voltage (1.4V)

Figure 11-3. Mode Select Input Timing Diagram



11.3.3 Output AC Specifications

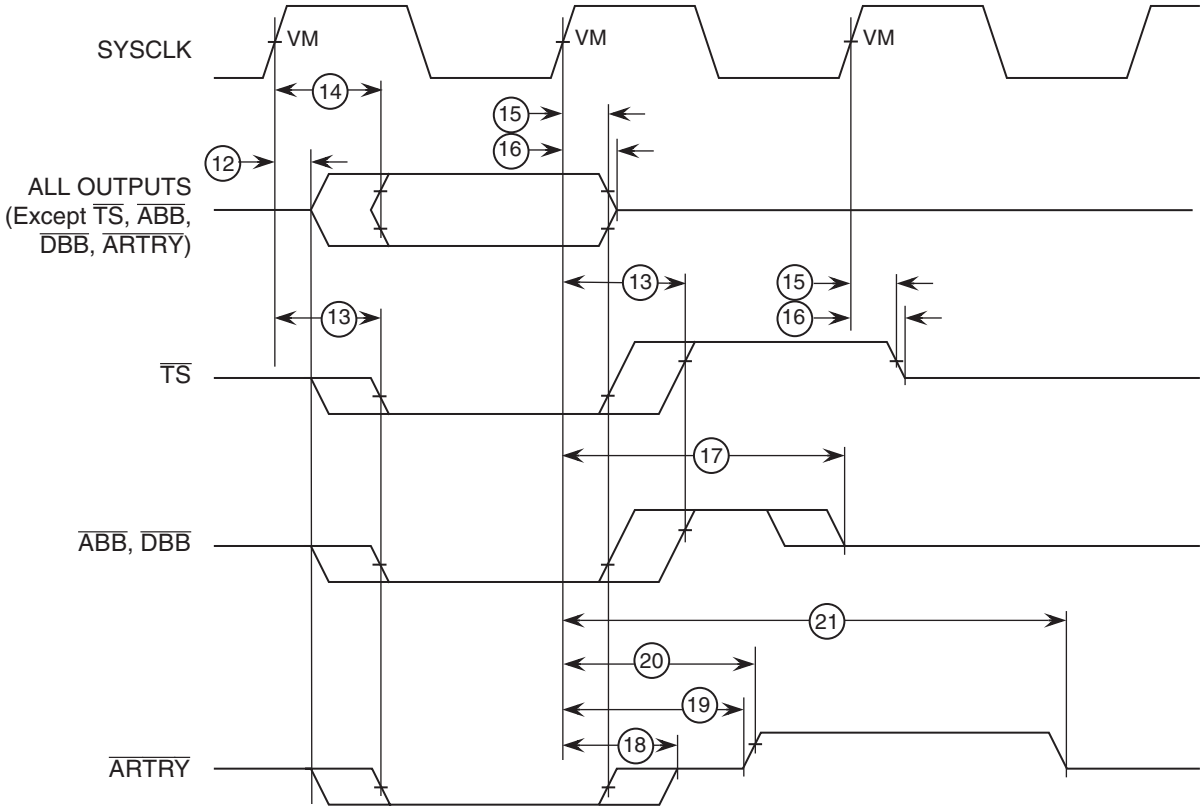
Table 11-4 provides the output AC timing specifications for the 603R (shown in Figure 11-4).

Table 11-4. Output AC Timing Specifications[1][2] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $55°C \le T_C \le 125°C$

Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages		CBGA 255, HiTCE CBGA 255 and CI-CGA 255				Unit	Note
		166, 200 MHz		233, 266 MHz		300 MHz			
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1	–	1	–	1	–	ns	
13a	SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(4)
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	8	–	8	–	8	ns	(6)
14a	SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11	–	11	–	11	ns	(4)
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	9	–	9	–	9	ns	(6)
15	SYSCLK to output invalid (output hold)	1	–	1	–	1	–	ns	(3)
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	8.5	–	8	–	8	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(7)
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	8	–	7.5	–	7.5	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK} + 1	–	0.2 × t_{SYSCLK}	–	ns	(3)(5) (8)
20	Maximum delay to $\overline{ARTRY}$ precharge	–	1	–	1	–	1	t_{SYSCLK}	(5)(8)
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	–	2	–	2	–	2	t_{SYSCLK}	(6)(8)

Notes:
1. All output specifications are measured from the 1.4V of the rising edge of SYSCLK to the TTL level (0.8V or 2V) of the signal in question. Both input and output timings are measured at the pin. See Figure 11-4.
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes C_L = 0 pF.
4. SYSCLK to output valid (5.5V to 0.8V) includes the extra delay associated with discharging the external voltage from 5.5V to 0.8V instead of from V_{DD} to 0.8V (5V CMOS levels instead of 3.3V CMOS levels).
5. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (ns) of the parameter in question.
6. The output signal transitions from GND to 2V or V_{DD} to 0.8V.
7. The nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 × tsysclk.
8. The nominal precharge width for $\overline{ARTRY}$ is 1 × tsysclk.

Figure 11-4. Output Timing Diagram



VM = Midpoint Voltage (1.4V)

Figure 11-7. Boundary-scan Timing Diagram

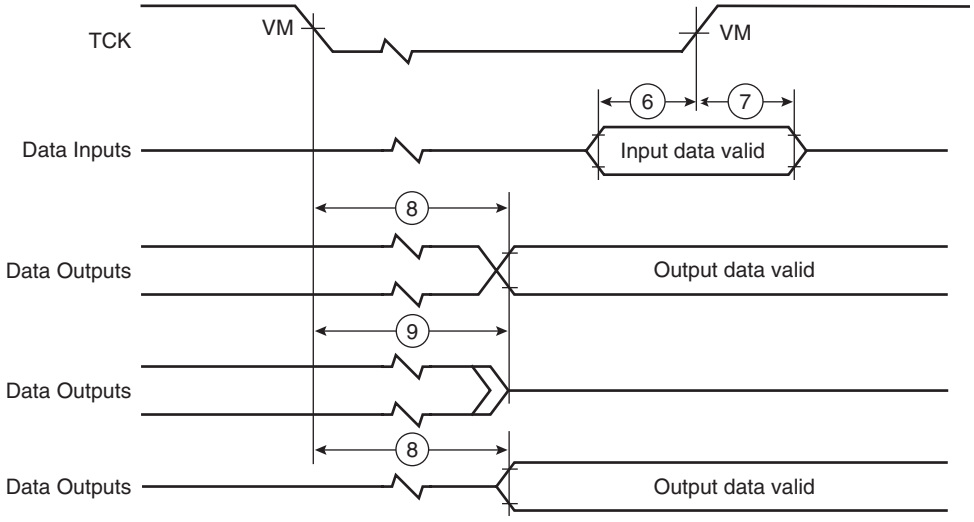
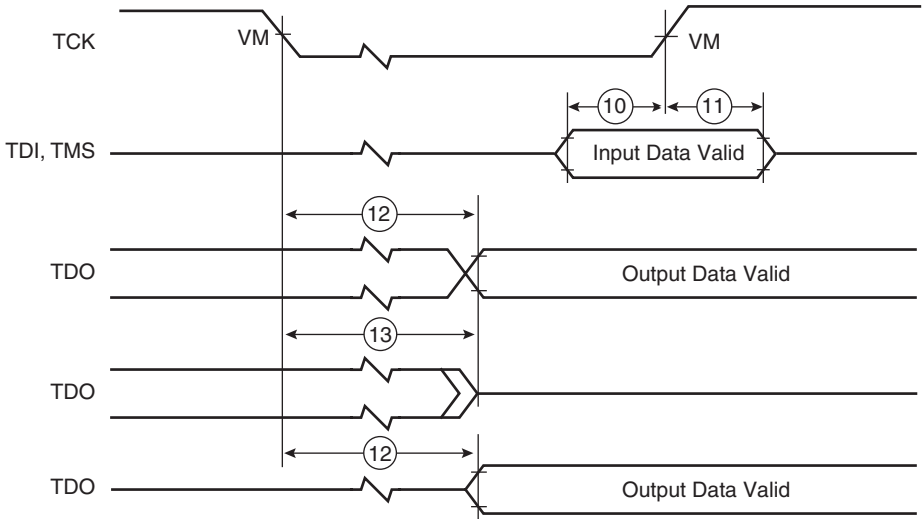


Figure 11-8. Test Access Port Timing Diagram



12. Functional Description

12.1 PowerPC Registers and Programming Model

The PowerPC architecture defines register-to-register operations for most computational instructions. Source operands for these instructions are accessed from the registers or are provided as immediate values embedded in the instruction opcode. The three-register instruction format allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory.

PowerPC processors have two levels of privilege—supervisor mode of operation (typically used by the operating system) and user mode of operation (used by the application software). The programming models incorporate 32 GPRs, 32 FPRs, Special-purpose Registers (SPRs) and several miscellaneous registers. Each PowerPC microprocessor also has its own unique set of Hardware Implementation (HID) registers.

12.1.7 Special-purpose Registers (SPRs)

The powerPC operating environment architecture defines numerous special-purpose registers that serve a variety of functions, such as providing controls, indicating status, configuring the processor, and performing special operations. During normal execution, a program can access the registers, shown in Figure 12-1 on page 32, depending on the program's access privilege (supervisor or user, determined by the privilege-level (PR) bit in the MSR. Note that registers such as the GPRs and FPRs are accessed through operands that are part of the instructions. Access to registers can be explicit (that is, through the use of specific instructions for that purpose such as Move to special-purpose register (**mtspr**) and move from special-purpose register (**mfspr**) instructions or implicit, as the part of the execution of an instruction. Some registers are accessed both explicitly and implicitly.

In the 603R, all SPRs are 32 bits wide.

- User-level SPRs:

  The following 603R SPRs are accessible by user-level software:

  – Link Register (LR) - The link register can be used to provide the branch target address and to hold the return address after branch and link instructions. The LR is 32 bits wide in 32-bit implementations.

  – Count Register (CTR) - The CRT is decremented and tested automatically as a result of branch-and-count instructions. The CTR is 32 bits wide in 32-bit implementations.

  – Integer Exception Register (XER) - The 32-bit XER contains the summary overflow bit, integer carry bit, overflow bit, and a field specifying the number of bytes to be transferred by a Load String Word Indexed (LSWX) or Store String Word Indexed (STSWX) instruction.

- Supervisor-level SPRs:

The 603R also contains SPRs that can be accessed only by supervisor-level software. These registers consist of the following:

  – The 32-bit DSISR defines the cause of data access and alignment exceptions.

  – The Data Address Register (DAR) is a 32-bit register that holds the address of an access after an alignment or DSI exception.

  – Decrementer register (DEC) is a 32-bit decrementing counter that provides a mechanism for causing a decrementer exception after a programmable delay.

  – The 32-bit SDR1 specifies the page table format used in virtual-to-physical address translation for pages. (Note that physical address is referred to as real address in the architecture specification).

  – The machine status Save/Restore Register 0 (SRR0) is a 32-bit register that is used by the 603R for saving the address of the instruction that caused the exception, and the address to return to when a Return from Interrupt (**RFI**) instruction is executed.

  – The machine status Save/Restore Register 1 (SRR1) is a 32-bit register used to save machine status on exceptions and to restore machine status when an **RFI** instruction is executed.

  – The 32-bit SPRG0-SPRG3 registers are provided for operating system use.

  – The External Access Register (EAR) is a 32-bit register that controls access to the external control facility through the External Control In Word Indexed (**ECIWX**) and External Control Out Word Indexed (**ECOWX**) instructions.

12.2 Instruction Set and Addressing Modes

The following subsections describe the PowerPC instruction set and addressing modes in general.

12.2.1 PowerPC Instruction Set and Addressing Modes

All PowerPC instructions are encoded as single-word (32-bit) opcodes. Instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses. This fixed instruction length and consistent format greatly simplifies instruction pipelining.

PowerPC Instruction Set

The PowerPC instructions are divided into the following categories:

- **Integer Instructions** – these include computational and logical instructions
  - Integer arithmetic instructions
  - Integer compare instructions
  - Integer logical instructions
  - Integer rotate and shift instructions
- **Floating-point Instructions** – these include floating-point computational instructions, as well as instructions that affect the FPSCR
  - Floating-point arithmetic instructions
  - Floating-point multiply/add instructions
  - Floating-point rounding and conversion instructions
  - Floating-point compare instructions
  - Floating-point status and control instructions
- **Load/Store Instructions** – these include integer and floating-point load and store instructions
  - Integer load and store instruction
  - Integer load and store multiple instructions
  - Floating-point load and store
  - Primitives used to construct atomic memory operations (**lwarx** and **stwcx** instructions)
- **Flow Control Instructions** – these include branching instructions, condition register logical instructions, trap instructions, and other instructions that affect the instruction flow
  - Branch and trap instructions
  - Condition register logical instructions
- **Processor Control Instructions** – these instructions are used for synchronizing memory accesses and management of caches, TLBs, and the segment registers
  - Move to/from SPR instructions
  - Move to/from MSR
  - Synchronize
  - Instruction synchronize

12.2.2 PowerPC 603R Microprocessor Instruction Set

The 603R instruction set is defined as follows:

- The 603R provides hardware support for all 32-bit PowerPC instructions.
- The 603R provides two implementation-specific instructions used for software table search operations following TLB misses:
  - Load Data TLB Entry (**tlbld**)
  - Load Instruction TLB Entry (**tlbli**)
- The 603R implements the following instructions which are defined as optional by the PowerPC architecture :
  - External Control in Word Indexed (**eciwx**)
  - External Control Out Word Indexed (**ecowx**)
  - Floating Select (**fsed**)
  - Floating Reciprocal Estimate Single-Precision (**fres**)
  - Floating Reciprocal Square Root Estimate (**frsqrte**)
  - Store Floating-Point as Integer Word (**stfiwx**)

12.3 Cache Implementation

The following subsections describe the way the PowerPC architecture deals with cache in general, and the 603R's specific implementation.

12.3.1 PowerPC Cache Characteristics

The PowerPC architecture does not define hardware aspects of cache implementations. For example, some PowerPC processors, including the 603R, have separate instruction and data caches (harvard architecture).

The PowerPC microprocessor controls the following memory access modes on a page or block basis:

- Write-back/write-through mode
- Cache-inhibited mode
- Memory coherency

Note that in the 603R, a cache line is defined as eight words. The VEA defines cache management instructions that provide a means by which the application programmer can affect the cache contents.

12.3.2 PowerPC 603R Microprocessor Cache Implementation

The 603R has two 16-Kbyte, four-way set-associative (instruction and data) caches. The caches are physically addressed, and the data cache can operate in either write-back or write-through modes as specified by the PowerPC architecture.

The data cache is configured as 128 sets of four lines each. Each line consists of 32 bytes, two state bits, and an address tag. The two state bits implement the three-state MEI (Modified/Exclusive/Invalid) protocol. Each line contains eight 32-bit words. Note that the PowerPC architecture defines the term block as the cacheable unit. For the 603R, the block size is equivalent to a cache line. A block diagram of the data cache organization is shown in Figure 12-2 on page 36.

The 603R's TLBs are 64-entry, 2-way set-associative caches that contain instruction and data address translations. The 603R provides hardware assistance for software table search operations through the ashed page table on the TLB misses. The supervisor software can invalidate TLB entries selectively.

The 603R also provides independent four-entry BAT arrays for instructions and data that maintain address translations for blocks of memory. These entries define blocks that can vary from 128 Kbytes to 256 Mbytes. The BAT arrays are maintained by system software.

As specified by the PowerPC architecture, the hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

Also as specified by the PowerPC architecture, the page table contains a number of Page Table Entry Groups (PTEGs). A PTEG contains eight Page Table Entries (PTEs) of eight bytes each; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

12.4.3 Instruction Timing

The 603R is a pipelined superscalar processor. A pipelined processor is one in which the processing of an instruction is reduced into discrete stages. Because the processing of an instruction is broken into a series of stages, an instruction does not require the entire resources of an execution unit. For example, after an instruction completes the decode stage, it can pass on to the next stage, while the subsequent instruction can advance into the decode stage. This improves the throughput of the instruction flow. For example, it may take three cycles for a floating-point instruction to complete, but if there are no stalls in the floating-point pipeline, a series of floating-point instructions can have a throughput of one instruction per cycle.

The instruction pipeline in the 603R has four major pipeline stages, described as follows:

- The fetch pipeline stage primarily involves retrieving instructions from the memory system and determining the location of the next instruction retrieval. Additionally, the BPU decodes branches during the fetch stage and folds out branch instructions before the dispatch stage if possible.
- The dispatch pipeline stage is responsible for decoding the instructions supplied by the instruction retrieval stage, and determining which of the instructions are eligible to be dispatched in the current cycle. In addition, the source operands of the instructions are read from the appropriate register file and dispatched with the instruction to the execute pipeline stage. At the end of the dispatch pipeline stage, the dispatched instructions and their operands are latched by the appropriate execution unit.
- During the execute pipeline stage each execution unit that has an executable instruction executes the selected instruction (perhaps over multiple cycles), writes the instruction's result into the appropriate rename register, and notifies the completion stage when the instruction has finished execution. In the case of an internal exception, the execution unit reports the exception to the completion/writeback pipeline stage and discontinues instruction execution until the exception is handled. The exception is not signaled until that instruction is the next to be completed. Execution of most floating-point instructions is pipelined within the FPU allowing up to three instructions to be executing in the FPU concurrently. The pipeline stages for the floating-point unit are multiply, add, and round-convert. Execution of most load/store instructions is also pipelined. The load/store unit has two pipeline stages. The first stage is for effective address calculation and MMU translation and the second stage is for accessing the data in the cache.

In Table 13-1, the horizontal scale represents the bus frequency (SYSCLK) and the vertical scale represents the PLL-CFG[0-3] signals.

For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation.

Table 13-1. CPU Frequencies for Common Bus Frequencies and Multipliers

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CBGA 255, HiTCE CBGA 255 and CI-CGA 255								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz	Bus 75 MHz
0100	2x	2x	-	-	-	-	-	-	150 (300)
0101	2x	4x	-	-	-	-	-	-	-
0110	2.5x	2x	-	-	-	-	150 (300)	166 (333)	187 (375)
1000	3x	2x	-	-	-	150 (300)	180 (360)	200 (400)	225 (450)
1110	3.5x	2x	-	-	-	175 (350)	210 (420)	233 (466)	263 (525)
1010	4x	2x	-	-	160 (320)	200 (400)	240 (480)	267 (533)	300 (600)
0111	4.5x	2x	-	150 (300)	180 (360)	225 (450)	270 (540)	300 (600)	-
1011	5x	2x	-	166 (333)	200 (400)	250 (500)	300 (600)	-	-
1001	5.5x	2x	-	183 (366)	220 (440)	275 (550)	-	-	-
1101	6x	2x	150 (300)	200 (400)	240 (480)	300 (600)	-	-	-
0011	PLL bypass								
1111	Clock off								

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz
0100	2x	2x	–	–	–	–	–	–
0101	2x	4x	–	–	–	–	–	–
0110	2.5x	2x	–	–	–	–	150 (300)	166 (333)
1000	3x	2x	–	–	–	150 (300)	180 (360)	200 (400)
1110	3.5x	2x	–	–	–	175 (350)	–	–

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz
1010	4x	2x	–	–	160 (320)	200 (400)	–	–
0111	4.5x	2x	–	150 (300)	180 (360)	–	–	–
1011	5x	2x	–	166 (333)	200 (400)	–	–	–
1001	5.5x	2x	–	183 (366)	–	–	–	–
1101	6x	2x	150 (300)	200 (400)	–	–	–	–
0011	PLL bypass							
1111	Clock off							

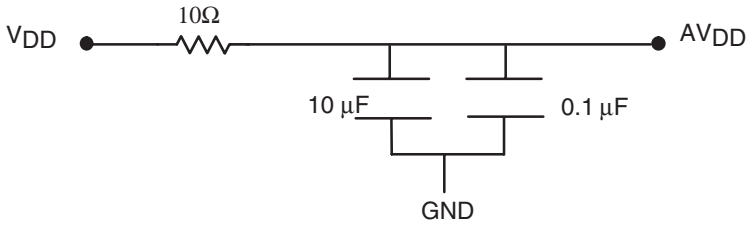
Notes: 1. Some PLL configurations may select bus, CPU or VCO frequencies which are not supported.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
The AC timing specifications given in this document do not apply in PLL-bypass mode.
3. In clock-off mode, no clocking occurs inside the 603e regardless of the SYSCLK input.

14. System Design Information

14.1 PLL Power Supply Filtering

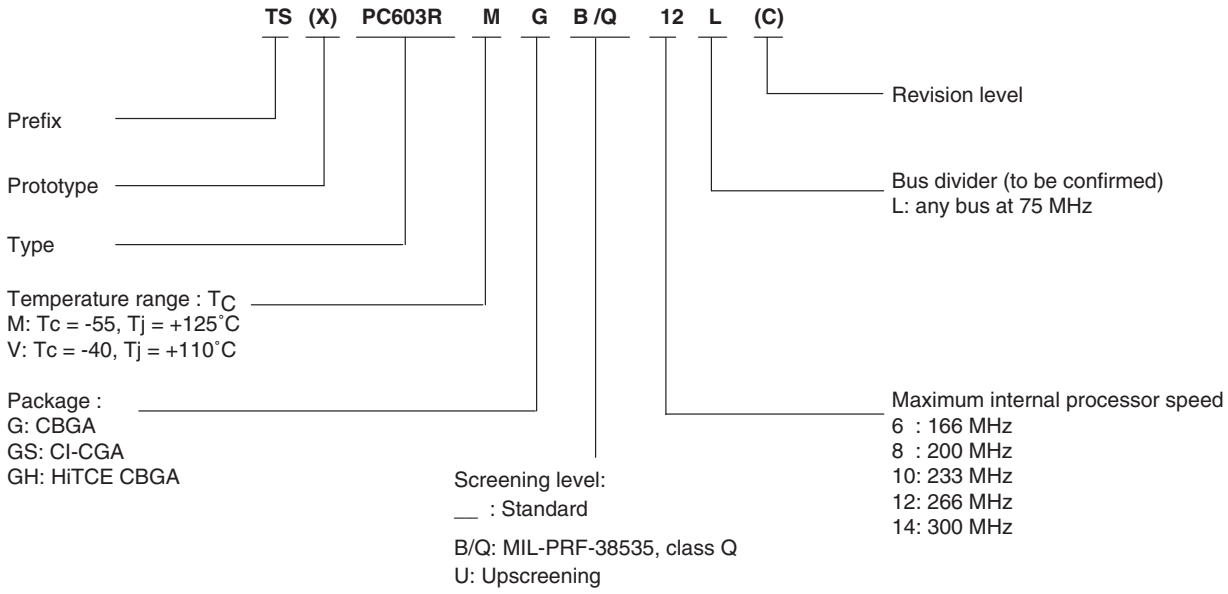
The AV_{DD} power signal is implemented on the 603e to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 14-1. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible. The 0.1 µF capacitor should be closest to the AV_{DD} pin, followed by the 10 µF capacitor, and finally the 10Ω resistor to V_{DD}. These traces should be kept short and direct.

Figure 14-1. PLL Power Supply Filter Circuit

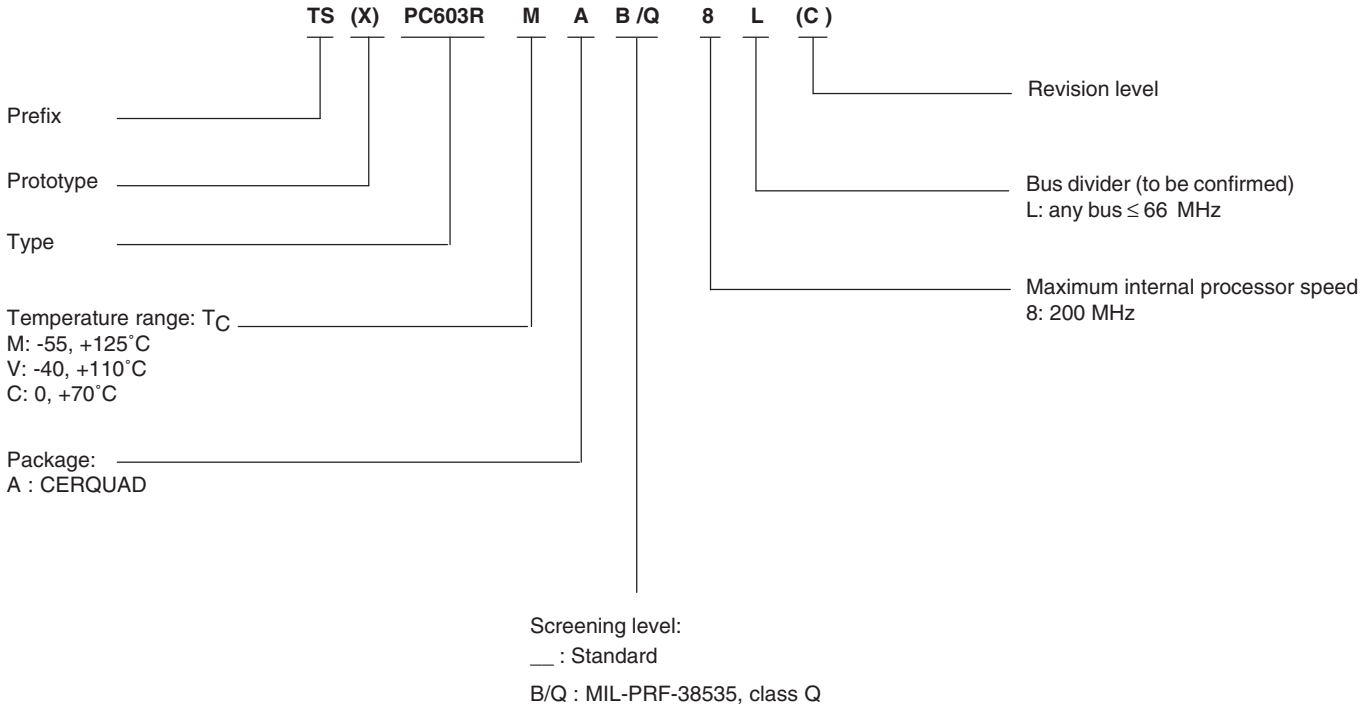


16. Ordering Information

16.1 Ordering Information of the CBGA, CI-CGA and HiTCE Packages



16.2 Ordering Information of the CERQUAD 240 Package



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