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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	255-BCBGA Exposed Pad
Supplier Device Package	255-CBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgu6lc

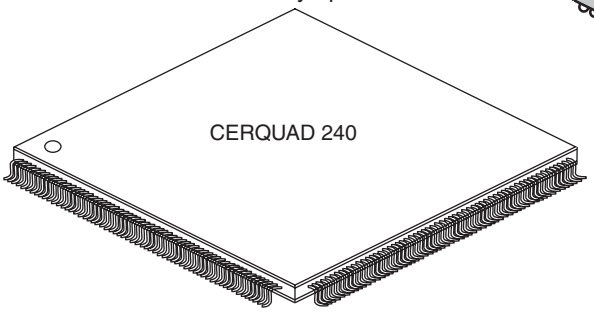
The 603R uses an advanced, 2.5/3.3V CMOS process technology and maintains full interface compatibility with TTL devices. It also integrates in-system testability and debugging features through JTAG boundary-scan capabilities.

2. Screening/Quality/Packaging

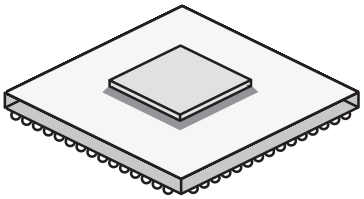
This product is manufactured in full compliance with:

- HiTCE CBGA according to Atmel Standards
- CI-CGA 255 and Cerquad: MIL-PRF-38535 class Q or according to Atmel standards
- CBGA 255: Upscreenings based upon Atmel standards
- CBGA, CI-CGA, HiTCE packages:
  - Full military temperature range (T_C = -55°C, T_j = +125°C)
  - Industrial temperature range (T_C = -40°C, T_j = +110°C)
- Cerquad:
  - Full military temperature range (T_C = -55°C, T_c = +125°C)
  - Industrial temperature range (T_C = -40°C, T_c = +110°C)
  - Commercial temperature ranges (T_C = 0°C, T_C = +70°C)
- Internal I/O Power Supply = 2.5 ±5% // 3.3V ±5%

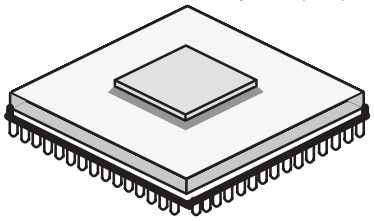
A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier
Cavity up



G suffix
CBGA 255
Ceramic Ball Grid Array



GS suffix
CI-CGA 255
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)



GH suffix
HiTCE 255
Ceramic Ball Grid Array

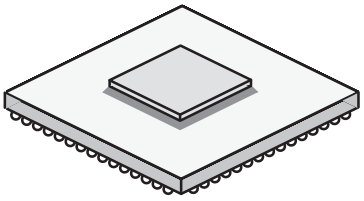
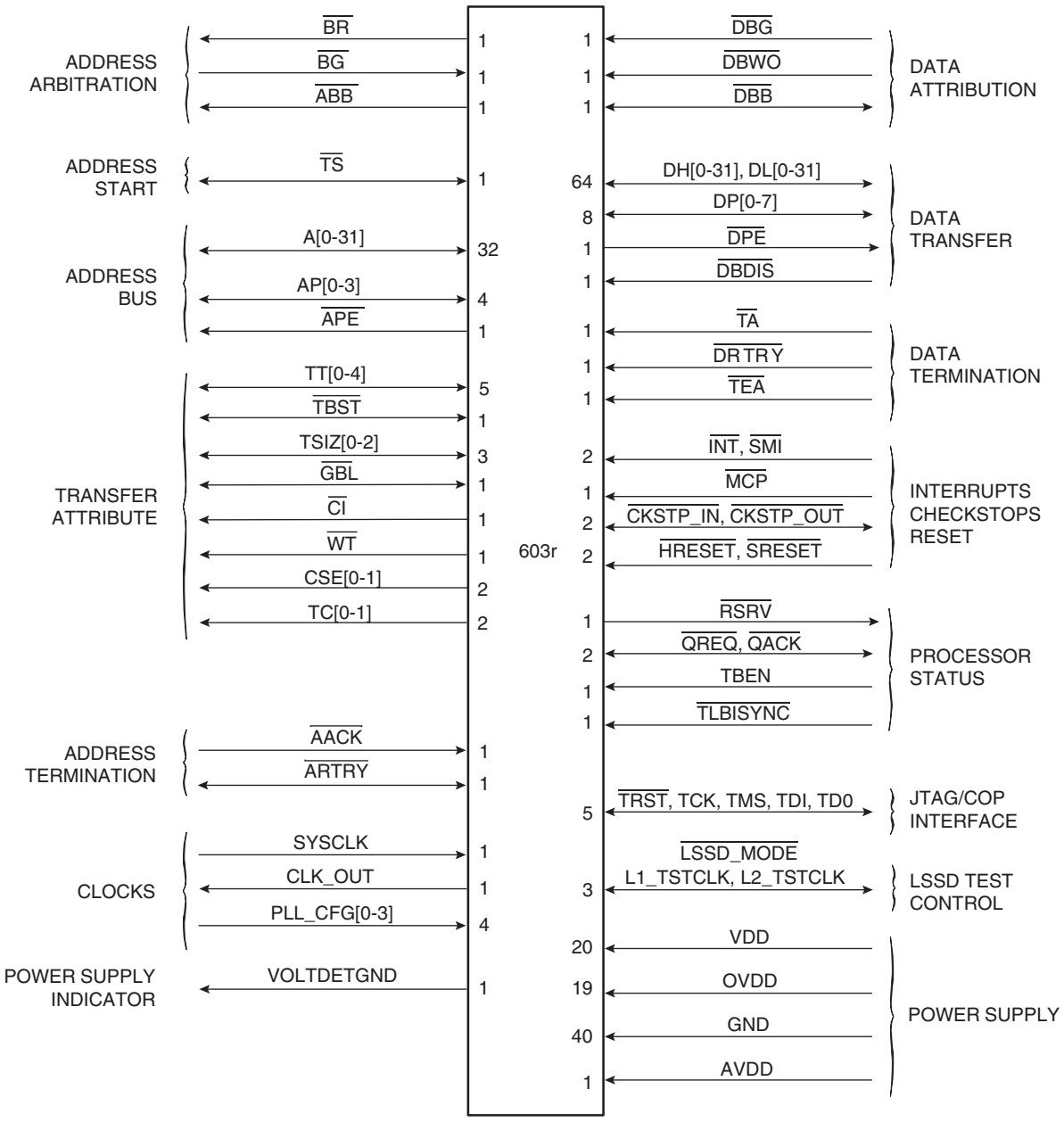


Figure 5-1. Functional Signal Groups



6. Detailed Specifications

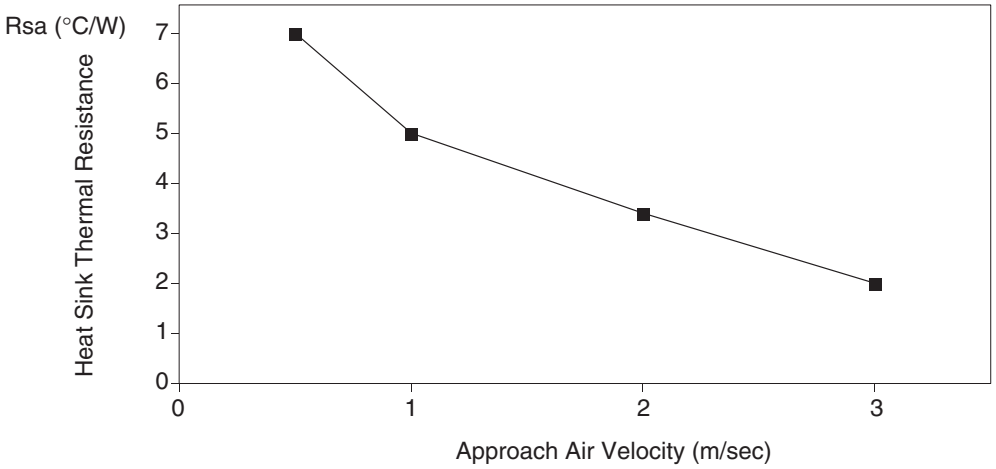
This specification describes the specific requirements for the microprocessor TSPC603R, in compliance with MIL-STD-883 class B or Atmel standard screening.

7. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

Figure 8-1. CBGA Thermal Management Example



Assuming an air velocity of 1 m/sec, the associated overall thermal resistance and junction temperature, found in Table 8-1 will result.

Table 8-1. Thermal Resistance and Junction Temperature

Configuration	R_{ja} (°C/W)	T_j (°C)
With 2328B heat sink	5	106

Vendors such as Aavid, Thermalloy®, and Wakefield Engineering can supply heat sinks with a wide range of thermal performance.

8.2 HiTCE CBGA Package

Table 8-2. HiTCE CBGA Package

Characteristic	Symbol	Value	Unit
Junction-to-bottom of balls(1)	$R\theta_J$	7.5	°C/W
Junction-to-ambient thermal resistance natural convection, four-layer (2s2p) board	$R\theta_{JMA}$	22.4(2)	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.7(3)	°C/W

Notes: 1. Simulation, no convection air flow.
2. Per JEDEC JESD51-2 with the board horizontal.
3. Per JEDEC JESD51-8 with the board horizontal.

8.3 CERQUAD 240 Package

This section provides thermal management data for the 603R. This information is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, wire-bond CERQUAD package with the cavity up (the silicon die is attached to the bottom of the package). This configuration enables dissipation through the PCB.

The thermal characteristics for a wire-bond CERQUAD package are as follows:

- Thermal resistance (junction to bottom of the case) (typical) = $R_{\theta jc}$ or θ_{jc} = 2.5°C/Watt
- Thermal resistance (junction to top of the case) is typically 16°C/W

- Functional units are clocked only when needed
- No software or hardware intervention required after mode is set
- Software/hardware and performance are transparent

Doze Mode

The doze mode disables most functional units but maintains cache coherency by enabling the bus interface unit and snooping. A snoop hit will cause the 603R to enable the data cache, copy the data back to the memory, disable the cache, and fully return to the doze state. In this mode:

- Most functional units are disabled
- Bus snooping and time base/decrementer are still enabled
- Dose mode sequence:
  - Set doze bit (HID0[8] = 1)
  - 603R enters doze mode after several processor clocks
- There are several methods for returning to full-power mode
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- The Transition to full-power state takes no more than a few processor cycles
- Phase Locked Loop (PLL) running and locked to SYSCLK

Nap Mode

The nap mode disables the 603R but still maintains the phase locked loop (PLL) and the time base/decrementer. The time base can be used to restore the 603R to full-on state after a programmed amount of time. Because bus snooping is disabled for nap and sleep modes, a hardware handshake using the quiesce request ($\overline{\text{QREQ}}$) and quiesce acknowledge ($\overline{\text{QACK}}$) signals is required to maintain data coherency. The 603R will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603R will enter the sleep or nap mode. In this mode:

- The time base/decrementer is still enabled
- Most functional units are disabled (including bus snooping)
- All non-essential input receivers are disabled
- Nap mode sequence:
  - Set nap bit (HID0[9] = 1)
  - 603R asserts quiesce request ($\overline{\text{QREQ}}$) signal
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$) signal
  - 603R enters sleep mode after several processor clocks
- There are several methods for returning to full-power mode:
  - Assert $\overline{\text{INT}}$, $\overline{\text{SPI}}$, $\overline{\text{MCP}}$ or decrementer interrupts
  - Assert hard reset or soft reset
- Transition to full-power takes no more than a few processor cycles
- The PLL is running and locked to SYSCLK

9.5 Power Dissipation

Table 9-2. Power Dissipation[1][2][3][4] with V_{DD}/AV_{DD} = 2.5 ±5%V, OV_{DD} = 3.3 ±5%V, GND = 0V, 0°C ≤ T_C ≤ 125°C

	Cerquad 240 Package		CBGA 255, HiTCE CBGA 255 and CI-CGA 255					
CPU Clock Frequency	**166 MHz**	**200 MHz**	**166 MHz**	**200 MHz**	**233 MHz**	**266 MHz**	**300 MHz**	**Units**
Full-on Mode (DPM Enabled)								
Typical	2.1	2.5	2.1	2.5	3	3.5	4	W
Max	3.2	4	3.2	4	4.6	5.3	6	W
Doze Mode								
Typical	1.5	1.7	1.5	1.7	1.8	2	2.1	W
Nap Mode								
Typical	100	120	100	120	140	160	180	mW
Sleep Mode								
Typical	96	110	96	110	123	135	150	mW
Sleep Mode-PLL Disabled								
Typical	60	60	60	60	60	60	60	mW
Sleep Mode-PLL and SYSCLK Disabled								
Typical	25	25	25	25	25	25	25	mW
Maximum	60	60	60	60	60	80	100	mW

Notes:
1. These values apply for all valid PLL_CFG[0-3] settings and do not include output driver power (OV_{DD}) or analog supply power (AV_{DD}). OV_{DD} power is system dependent but is typically ≤ 10% of V_{DD}. Worst case AV_{DD} = 15 mW.
2. Typical power is an average value measured at $V_{DD} = AV_{DD}$ = 2.5V, OV_{DD} = 3.3V, in a system executing typical applications and benchmark sequences.
3. Maximum power is measured at V_{DD} = 2.625V using a worst-case instruction mix.
4. To calculate the power consumption at low temperature (-55°C), **use a factor of 1.25.**

9.6 Marking

Each microcircuit is legible and permanently marked with at least the following information:

- Atmel logo
- Manufacturer's part number
- Class B identification if applicable
- Date code of inspection lot
- ESD identifier if available
- Country of manufacture

10. Pin Assignments

10.1 CBGA 255 and CI-CGA 255 Packages

Figure 10-1 (pin matrix) shows the pinout as viewed from the top of the CBGA and CI-CGA packages. The direction of the top surface view is shown by the side profile of the packages.

10.1.1 Pinout Listing

Table 10-1. Power and Ground Pins

	CBGA, HiTCE CBGA and CI-CGA Pin Number	
	V_{DD}	**GND**
PLL (AV_{DD})	A10	
Internal Logic[1] (V_{DD})	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12
I/O Drivers[1] (OV_{DD})	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	

Notes: 1. OV_{DD} inputs apply power to the I/O drivers and V_{DD} inputs supply power to the processor core.

Table 10-2. Signal Pinout Listing

Signal Name	CBGA, HiTCE CBGA and CI-CGA Pin Number	Active	I/O
A[0-31]	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, G02, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP[0-3]	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
$\overline{\text{ARTRY}}$	J04	Low	I/O
$\overline{\text{BG}}$	L01	Low	Input
$\overline{\text{BR}}$	B06	Low	Output
$\overline{\text{CI}}$	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	A06	Low	Output
CLK_OUT	D07	-	Output
CSE[0-1]	B01, B05	High	Output
$\overline{\text{DBB}}$	J14	Low	I/O
$\overline{\text{DBG}}$	N01	Low	Input
$\overline{\text{DBDIS}}$	H15	Low	Input
$\overline{\text{DBWO}}$	G04	Low	Input
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP[0-7]	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	A05	Low	Output
$\overline{\text{DRTRY}}$	G16	Low	Input

10.2.1 Pinout Listing

Table 10-3. Power and Ground Pins

	CERQUAD Pin Number	
	VCC	**GND**
PLL (AV_{DD})	209	
Internal Logic	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239
Output Drivers	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238

Table 10-4. Signal Pinout Listing

Signal Name	CERQUAD Pin Number
A[0-31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37
$\overline{\text{AACK}}$	28
$\overline{\text{ABB}}$	36
AP[0-3]	231,230,227,226
$\overline{\text{APE}}$	218
$\overline{\text{ARTRY}}$	32
$\overline{\text{BG}}$	27
$\overline{\text{BR}}$	219
$\overline{\text{CI}}$	237
$\overline{\text{CKSTP\_IN}}$	215
$\overline{\text{CKSTP\_OUT}}$	216
CLK_OUT	221
CSE[0-1]	225,150
$\overline{\text{DBB}}$	145
$\overline{\text{DBG}}$	26
$\overline{\text{DBDIS}}$	153
$\overline{\text{DBWO}}$	25
DH[0-31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66
DL[0-31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64
DP[0-7]	38, 40, 41, 42, 46, 47, 48, 50
$\overline{\text{DPE}}$	217
$\overline{\text{DRTRY}}$	156
$\overline{\text{GBL}}$	1
$\overline{\text{HRESET}}$	214

Table 10-4. Signal Pinout Listing (Continued)

Signal Name	CERQUAD Pin Number
$\overline{\text{INT}}$	188
L1_TSTCLK[1]	204
L2_TSTCLK[1]	203
$\overline{\text{LSSD\_MODE}}$[1]	205
$\overline{\text{MCP}}$	186
PLL_CFG[0-3]	213, 211, 210, 208
$\overline{\text{QACK}}$	235
$\overline{\text{QREQ}}$	31
$\overline{\text{RSRV}}$	232
$\overline{\text{SMI}}$	187
$\overline{\text{SRESET}}$	189
SYSCLK	212
$\overline{\text{TA}}$	155
TBEN	234
$\overline{\text{TBST}}$	192
TC[0-1]	224, 223
TCK	201
TDI	199
TDO	198
$\overline{\text{TEA}}$	154
$\overline{\text{TLBISYNC}}$	233
TMS	200
$\overline{\text{TRST}}$	202
$\overline{\text{TS}}$	149
TSIZ[0-2]	197, 196, 195
TT[0-4]	191, 190, 185, 184, 180
$\overline{\text{WT}}$	236
NC	

Notes: 1. These are test signals for factory use only and must be pulled up to V_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core. Future members of the 603 family may use different OV_{DD} and V_{DD} input levels.

Table 10-6. Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

Signal Name	Abbreviation	Signal Function	Signal Type
Global	$\overline{\text{GBL}}$	If output, a transaction is global If input, a transaction must be snooped by the 603R	I/O
Hard Reset	$\overline{\text{HRESET}}$	Initiates a complete hard reset operation	Input
Interrupt	$\overline{\text{INT}}$	Initiates an interrupt if bit EE of MSR register is set	Input
Factory Test	$\overline{\text{LSSD\_MODE}}$	LSSD test control signal for factory use only	Input
	L1_TSTCLK	LSSD test control signal for factory use only	Input
	L2_TSTCLK	LSSD test control signal for factory use only	Input
Machine Check Interrupt	$\overline{\text{MCP}}$	Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set	Input
PLL Configuration	PLL_CFG[0-3]	Configures the operation of the PLL and the internal processor clock frequency	Input
Power supply indicator	VOLTDETGND	Available only on BGA package Indicates to the power supply that a low-voltage processor is present.	Output
Quiescent Acknowledge	$\overline{\text{QACK}}$	All bus activity has terminated and the 603R may enter a quiescent (or low power) state	Input
Quiescent Request	$\overline{\text{QREQ}}$	Is requesting all bus activity normally to enter a quiescent (low power) state	Output
Reservation	$\overline{\text{RSRV}}$	Represents the state of the reservation coherency bit in the reservation address register	Output
System Management Interrupt	$\overline{\text{SMI}}$	Initiates a system management interrupt operation if the bit EE of MSR register is set	Input
Soft Reset	$\overline{\text{SRESET}}$	Initiates processing for a reset exception	Input
System Clock	SYSCLK	Represents the primary clock input for the 603R, and the bus clock frequency for 603R bus operation	Input
Test Clock	CLK_OUT	Provides PLL clock output for PLL testing and monitoring	Output
Transfer Acknowledge	$\overline{\text{TA}}$	A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully	Input
Timebase Enable	TBEN	The timebase should continue clocking	Input
Transfer Burst	$\overline{\text{TBST}}$	If output, a burst transfer is in progress If input, when snooping for single-beat reads	I/O
Transfer Code	TC[0-1]	Special encoding for the transfer in progress	Output
Test Clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)	Input
Test Data Input	TDI	Serial data input for the TAP	Input
Test Data Output	TDO	Serial data output for the TAP	Output
Transfer Error Acknowledge	$\overline{\text{TEA}}$	A bus error occurred	Input
TLBI Sync	$\overline{\text{TLBISYNC}}$	Instruction execution should stop after execution of a **tlbsync** instruction	Input
Test Mode Select	TMS	Selects the principal operations of the test-support circuitry	Input
Test Reset	$\overline{\text{TRST}}$	Provides an asynchronous reset of the TAP controller	Input
Transfer Size	TSIZ[0-2]	For memory accesses, these signals along with $\overline{\text{TBST}}$ indicate the data transfer size for the current bus operation	I/O

3. Leakage currents are measured for nominal OV_{DD} and V_{DD} or both OV_{DD} and V_{DD}. Same variation (for example, both V_{DD} and OV_{DD} vary by either +5% or -5%)

11.3 Dynamic Characteristics

11.3.1 Clock AC Specifications

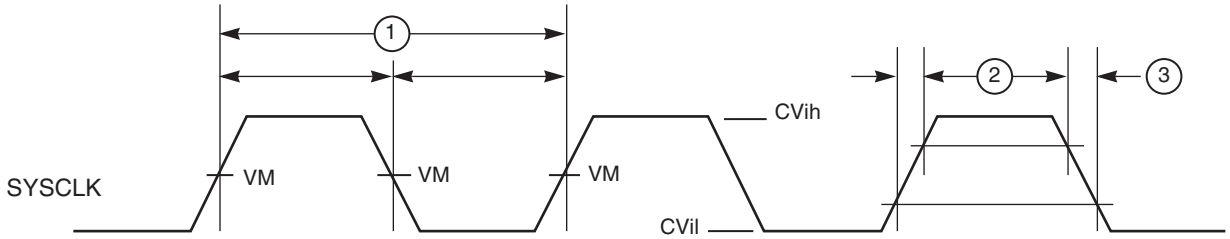
Table 11-2 provides the clock AC timing specifications as defined in Figure 11-1.

Table 11-2. Clock AC Timing Specifications[1][2][3][4] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

Figure Number	Characteristics	CBGA 255, HiTCE CBGA 255, CI-CGA 255 and CERQUAD				CBGA 255, HiTCE CBGA 255 and CI-CGA 255							
		166 MHz		200 MHz		233 MHz		266 MHz		300 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
	Processor Frequency	150	166	150	200	180	233	180	266	180	300	MHz	[5]
	VCO Frequency	300	332	300	400	360	466	360	532	360	600	MHz	[5]
	SYSCLK (bus) Frequency	25	66.7	33.3	66.7	33.3	75	33.3	75	33.3	75	MHz	[5]
1	SYSCLK Cycle Time	15	30	13.3	30	13.3	30	13.3	30	13.3	30	ns	
2,3	SYSCLK Rise and Fall Time	–	2	–	2	–	2	–	2	–	2	ns	[1]
4	SYSCLK Duty Cycle (1.4V measured)	40	60	40	60	40	60	40	60	40	60	%	[3]
	SYSCLK Jitter	–	±150	–	±150	–	±150	–	±150	–	±150	ps	[2]
	603R Internal PLL Relock Time	–	100	–	100	–	100	–	100	–	100	µs	[3][4]

Notes:
1. Rise and fall times for the SYSCLK input are measured from 0.4V to 2.4V.
2. Cycle-to-cycle jitter is guaranteed by design.
3. Timing is guaranteed by design and characterization and is not tested.
4. The PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD}, OV_{DD}, AV_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen so that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description for valid PLL_CFG[0-3] settings.

Figure 11-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage (1.4V)

Having access to privilege instructions, registers, and other resources allows the operating system to control the application environment (providing virtual memory and protecting operating system and critical machine resources). Instructions that control the state of the processor, the address translation mechanism, and supervisor registers can be executed only when the processor is operating in supervisor mode.

The following sections summarize the PowerPC registers that are implemented in the 603R.

12.1.1 General-purpose Registers (GPRs)

The PowerPC architecture defines 32 user-level, General-purpose Registers (GPRs). These registers are either 32 bits wide in 32-bit PowerPC microprocessors or 64 bits wide in 64-bit PowerPC microprocessors. The GPRs serve as the data source or destination for all integer instructions.

12.1.2 Floating-point Registers (FPRs)

The PowerPC architecture also defines 32 user-level, 64-bit Floating-point Registers (FPRs). The FPRs serve as the data source or destination for floating-point instructions. These registers can contain data objects of either single- or double-precision floating-point formats.

12.1.3 Condition Register (CR)

The CR is a 32-bit user-level register that consists of eight four-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

12.1.4 Floating-Point Status and Control Register (FPSCR)

The Floating-point Status and Control Register (FPSCR) is a user-level register that contains all exception signal bits, exception summary bits, exception enable bits, and rounding control bits needed for compliance with the IEEE 754 standard.

12.1.5 Machine State Register (MSR)

The Machine State Register (MSR) is a supervisor-level register that defines the state of the processor. The contents of this register are saved when an exception is taken and restored when the exception handling is completed. The 603R implements the MSR as a 32-bit register, 64-bit PowerPC processors implement a 64-bit MSR.

12.1.6 Segment Registers (SRs)

For memory management, 32-bit PowerPC microprocessors implement sixteen 32-bit Segment Registers (SRs). To speed access, the 603R implements the segment registers as two arrays; a main array (for data memory accesses) and a shadow array (for instruction memory accesses). Loading a segment entry with the Move to Segment Register (STSR) instruction loads both arrays.

12.1.7 Special-purpose Registers (SPRs)

The powerPC operating environment architecture defines numerous special-purpose registers that serve a variety of functions, such as providing controls, indicating status, configuring the processor, and performing special operations. During normal execution, a program can access the registers, shown in Figure 12-1 on page 32, depending on the program's access privilege (supervisor or user, determined by the privilege-level (PR) bit in the MSR. Note that registers such as the GPRs and FPRs are accessed through operands that are part of the instructions. Access to registers can be explicit (that is, through the use of specific instructions for that purpose such as Move to special-purpose register (**mtspr**) and move from special-purpose register (**mfspr**) instructions or implicit, as the part of the execution of an instruction. Some registers are accessed both explicitly and implicitly.

In the 603R, all SPRs are 32 bits wide.

- User-level SPRs:

  The following 603R SPRs are accessible by user-level software:

  – Link Register (LR) - The link register can be used to provide the branch target address and to hold the return address after branch and link instructions. The LR is 32 bits wide in 32-bit implementations.

  – Count Register (CTR) - The CRT is decremented and tested automatically as a result of branch-and-count instructions. The CTR is 32 bits wide in 32-bit implementations.

  – Integer Exception Register (XER) - The 32-bit XER contains the summary overflow bit, integer carry bit, overflow bit, and a field specifying the number of bytes to be transferred by a Load String Word Indexed (LSWX) or Store String Word Indexed (STSWX) instruction.

- Supervisor-level SPRs:

The 603R also contains SPRs that can be accessed only by supervisor-level software. These registers consist of the following:

  – The 32-bit DSISR defines the cause of data access and alignment exceptions.

  – The Data Address Register (DAR) is a 32-bit register that holds the address of an access after an alignment or DSI exception.

  – Decrementer register (DEC) is a 32-bit decrementing counter that provides a mechanism for causing a decrementer exception after a programmable delay.

  – The 32-bit SDR1 specifies the page table format used in virtual-to-physical address translation for pages. (Note that physical address is referred to as real address in the architecture specification).

  – The machine status Save/Restore Register 0 (SRR0) is a 32-bit register that is used by the 603R for saving the address of the instruction that caused the exception, and the address to return to when a Return from Interrupt (**RFI**) instruction is executed.

  – The machine status Save/Restore Register 1 (SRR1) is a 32-bit register used to save machine status on exceptions and to restore machine status when an **RFI** instruction is executed.

  – The 32-bit SPRG0-SPRG3 registers are provided for operating system use.

  – The External Access Register (EAR) is a 32-bit register that controls access to the external control facility through the External Control In Word Indexed (**ECIWX**) and External Control Out Word Indexed (**ECOWX**) instructions.

12.2 Instruction Set and Addressing Modes

The following subsections describe the PowerPC instruction set and addressing modes in general.

12.2.1 PowerPC Instruction Set and Addressing Modes

All PowerPC instructions are encoded as single-word (32-bit) opcodes. Instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses. This fixed instruction length and consistent format greatly simplifies instruction pipelining.

PowerPC Instruction Set

The PowerPC instructions are divided into the following categories:

- **Integer Instructions** – these include computational and logical instructions
  - Integer arithmetic instructions
  - Integer compare instructions
  - Integer logical instructions
  - Integer rotate and shift instructions
- **Floating-point Instructions** – these include floating-point computational instructions, as well as instructions that affect the FPSCR
  - Floating-point arithmetic instructions
  - Floating-point multiply/add instructions
  - Floating-point rounding and conversion instructions
  - Floating-point compare instructions
  - Floating-point status and control instructions
- **Load/Store Instructions** – these include integer and floating-point load and store instructions
  - Integer load and store instruction
  - Integer load and store multiple instructions
  - Floating-point load and store
  - Primitives used to construct atomic memory operations (**lwarx** and **stwcx** instructions)
- **Flow Control Instructions** – these include branching instructions, condition register logical instructions, trap instructions, and other instructions that affect the instruction flow
  - Branch and trap instructions
  - Condition register logical instructions
- **Processor Control Instructions** – these instructions are used for synchronizing memory accesses and management of caches, TLBs, and the segment registers
  - Move to/from SPR instructions
  - Move to/from MSR
  - Synchronize
  - Instruction synchronize

- **Memory Control Instructions** – these instructions provide control of caches, TLBs, and segment registers
  - Supervisor-level cache management instructions
  - User-level cache instructions
  - Segment register manipulation instructions
  - Translation lookaside buffer management instructions

Note that this grouping of the instructions does not indicate which execution unit executes a particular instruction or group of instructions.

Integer instructions operate on byte, half-word, and word operands. Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands. The PowerPC architecture uses instructions that are four bytes long and word-aligned. It provides for byte, half-word, and word operand loads and stores between the memory and a set of 32 GPRs. It also provides for word and double-word operand loads and stores between the memory and a set of 32 Floating-point Registers (FPRs).

Computational instructions do not modify the memory. To use a memory operand in a computation and then modify the same or another memory location, the memory contents must be loaded into a register, modified, and then written back to the target location with distinct instructions.

PowerPC processors follow the program flow when they are in the normal execution state. However, the flow of instructions can be interrupted directly by the execution of an instruction or by an asynchronous event. Either kind of exception may cause one of several components of the system software to be invoked.

- Calculating Effective Address

  The Effective Address (EA) is the 32-bit address computed by the processor when executing a memory access or branch instruction or when fetching the next sequential instruction.

  The PowerPC architecture supports two simple memory addressing modes:

  - EA = (RA|0) + offset (including offset = 0) (register indirect with immediate index)
  - EA = (RA|0) + rB (register indirect with index)

These simple addressing modes allow efficient address generation for memory accesses. Calculation of the effective address for aligned transfers occurs in a single clock cycle.

For a memory access instruction, if the sum of the effective address and the operand length exceeds the maximum effective address, the memory operand is considered to wrap around from the maximum effective address to effective address 0.

Effective address computations for both data and instruction accesses use 32-bit unsigned binary arithmetic. A carry over from bit 0 is ignored in 32-bit implementations.

Table 12-2. Exceptions and Conditions (Continued)

Exception Type	Vector Offset (hex)	Causing Conditions
Program	00700	A program exception is caused by one of the following exception conditions, which correspond to bit settings in SRR1 and arise during execution of an instruction: • Floating-point enabled exception – A floating-point enabled exception condition is generated when the following condition is met: (MSR[FE0] | MSR[FE1]) & FPSCR[FEX] is 1 FPSER[FEX] is set by the execution of a floating-point instruction that causes an enabled exception or by the execution of one of the "move to FPSCR" instructions that results in both an exception condition bit and its corresponding enable bit being set in the FPSCR • Illegal instruction – an illegal instruction program exception is generated when execution of an instruction is attempted with an illegal opcode or illegal combination of opcode and extended opcode fields (including PowerPC instructions not implemented in the 603e), or when execution of an optional instruction not provided in the 603e is attempted (these do not include those optional instructions that are treated as no-ops) • Privileged instruction – a privileged instruction type program exception is generated when the execution of a privileged instruction is attempted and the MSR register user privilege bit, MSR[PR], is set. In the 603e, this exception is generated for **mtspr** or **mfspr** with an invalid SPR field if SPR[0] = 1 and MSR[PR] = 1. This may not be true for all PowerPC processors • Trap – a trap type program exception is generated when any of the conditions specified in a trap instruction is met
Floating-point unavailable	00800	A floating-point unavailable exception is caused by an attempt to execute a floating-point instruction (including floating-point load, store, and more instructions) when the floating-point available bit is disabled, (MSR[FP] = 0)
Decrementer	00900	The decrementer exception occurs when the most significant bit of the decrementer (DEC) register transitions from 0 to 1. Must also be enabled with the MSR[EE] bit
Reserved	00A00–00BFF	–
System call	00C00	A system call exception occurs when a System Call (sc) instruction is executed
Trace	00D00	A trace execution is taken when MSR[SE] = 1 or when the currently completing instruction is a branch and MSR[BE] = 1
Reserved	00E00	The 603e does not generate an exception to this vector. Other PowerPC processors may use this vector for floating-point assist exceptions
Reserved	00E10–00FFF	–
Instruction translation miss	01000	An instruction translation miss exception is caused when an effective address for an instruction fetch cannot be translated by the ITLB
Data load translation miss	01100	A data load translation miss exception is caused when an effective address for a data load operation cannot be translated by the DTLB
Data store translation miss	01200	A data store translation miss exception is caused when an effective address for a data store operation cannot be translated by the DTLB; or where a DTLB hit occurs, and the change bit in the PTE must be set due to a data store operation

In Table 13-1, the horizontal scale represents the bus frequency (SYSCLK) and the vertical scale represents the PLL-CFG[0-3] signals.

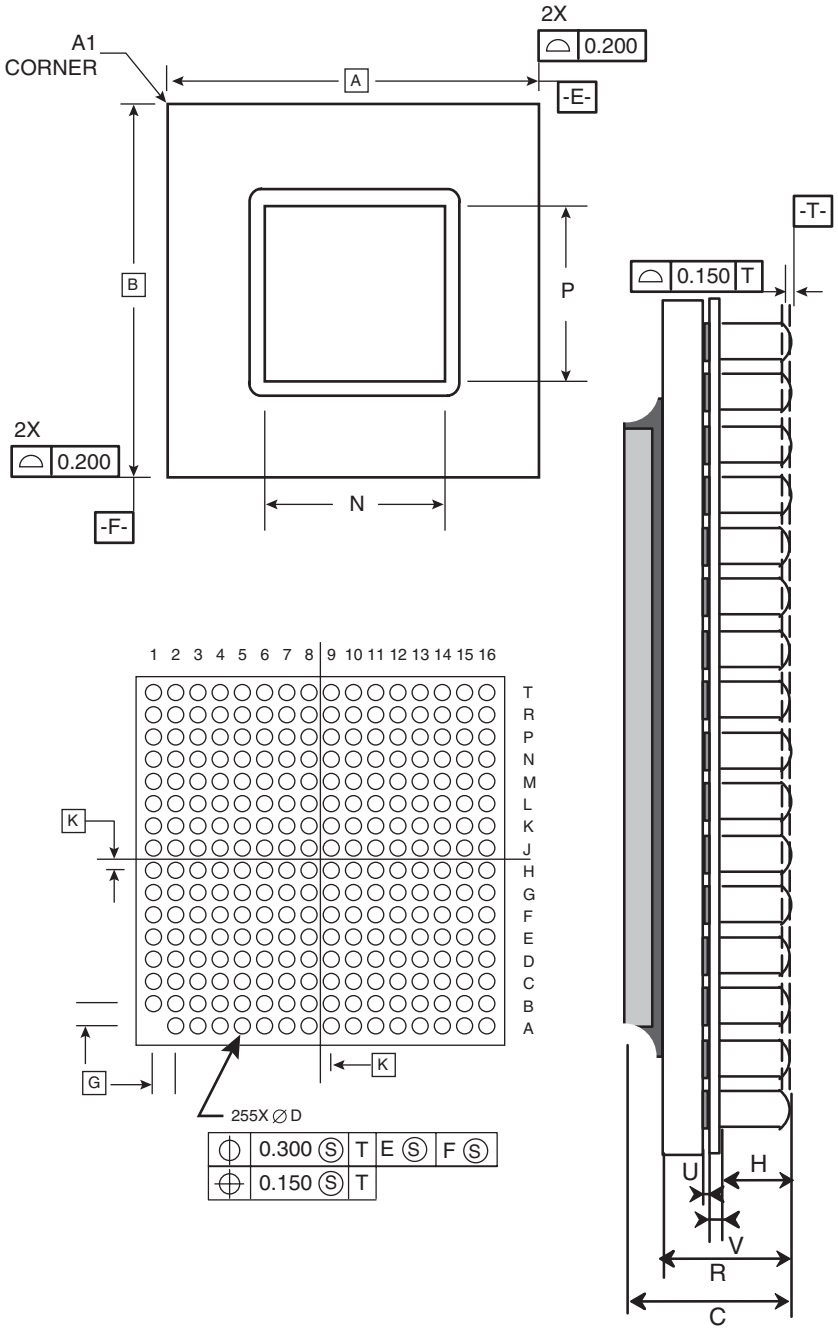
For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation.

Table 13-1. CPU Frequencies for Common Bus Frequencies and Multipliers

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CBGA 255, HiTCE CBGA 255 and CI-CGA 255								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz	Bus 75 MHz
0100	2x	2x	-	-	-	-	-	-	150 (300)
0101	2x	4x	-	-	-	-	-	-	-
0110	2.5x	2x	-	-	-	-	150 (300)	166 (333)	187 (375)
1000	3x	2x	-	-	-	150 (300)	180 (360)	200 (400)	225 (450)
1110	3.5x	2x	-	-	-	175 (350)	210 (420)	233 (466)	263 (525)
1010	4x	2x	-	-	160 (320)	200 (400)	240 (480)	267 (533)	300 (600)
0111	4.5x	2x	-	150 (300)	180 (360)	225 (450)	270 (540)	300 (600)	-
1011	5x	2x	-	166 (333)	200 (400)	250 (500)	300 (600)	-	-
1001	5.5x	2x	-	183 (366)	220 (440)	275 (550)	-	-	-
1101	6x	2x	150 (300)	200 (400)	240 (480)	300 (600)	-	-	-
0011	PLL bypass								
1111	Clock off								

PLL_CFG[0-3]	CPU Frequency in MHZ (VCO Frequency in MHz) specific to CERQUAD							
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz
0100	2x	2x	–	–	–	–	–	–
0101	2x	4x	–	–	–	–	–	–
0110	2.5x	2x	–	–	–	–	150 (300)	166 (333)
1000	3x	2x	–	–	–	150 (300)	180 (360)	200 (400)
1110	3.5x	2x	–	–	–	175 (350)	–	–

Figure 15-3. Mechanical Dimensions and Bottom Surface Nomenclature of the CI-CGA Package

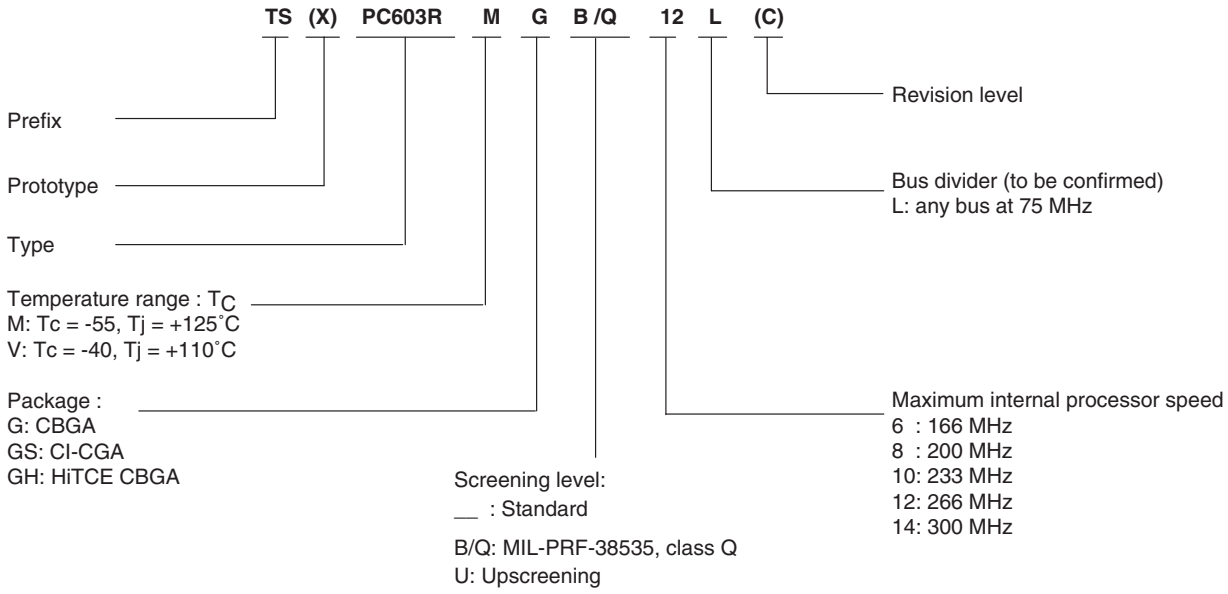


Notes: 1. Dimensioning and tolerancing per ASME Y14.5M—1994
2. Controlling dimension: millimeter

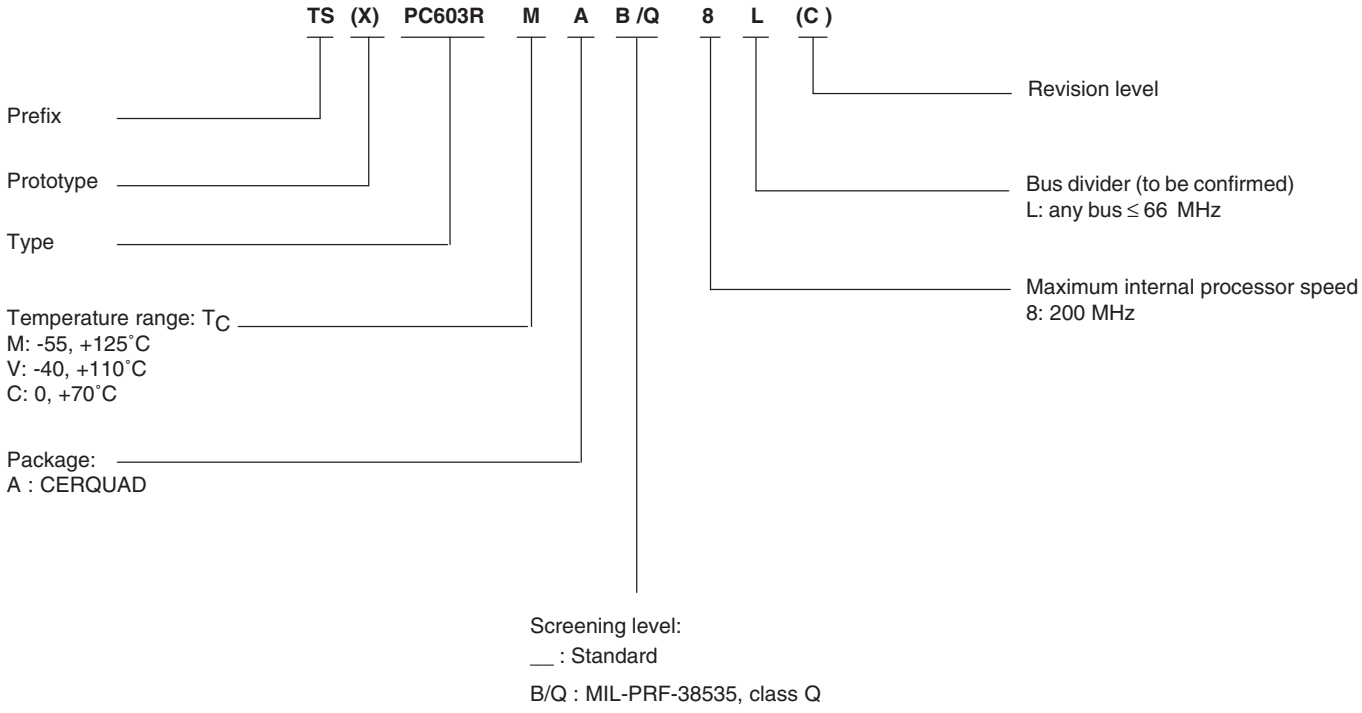
Dim	Millimeters	
	Min	Max
A	21.000 BSC	
B	21.000 BSC	
C	3.84 BSC	
D	0.790	0.990
G	1.270 BSC	
H	1.545	1.695
K	0.635 BSC	
N	5.000	
P	7.000	
R	3.02 BSC	
U	0.10 BSC	
V	0.25	0.35

16. Ordering Information

16.1 Ordering Information of the CBGA, CI-CGA and HiTCE Packages



16.2 Ordering Information of the CERQUAD 240 Package



Note: For availability of the different versions, contact your Atmel sales office.

17. Definitions

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with the customer and application validation	Before design phase
Target specification	This datasheet contains target or goal specifications for product development	Valid during the design phase
Preliminary specification α site	This datasheet contains preliminary data. Additional data may be published at a later date and could include simulation results	Valid before characterization phase
Preliminary specification β site	This datasheet also contains characterization results	Valid before the industrialization phase
Product specification	This datasheet contains final product specifications	Valid for production purpose
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stresses above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification		

17.1 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

18. Document Revision History

Table 18-1 provides a revision history for this hardware specification.

Table 18-1. Document Revision History

Revision Number	Date	Substantive Change(s)
B	07/2005	Added HiTCE package for PowerPC 603R
A	10/2004	This document is a merge of TSPC603R in CBGA255/CI-CGA 255 package (ref 2125B) and TSPC603R in Cerquad package (ref 2127A)