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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

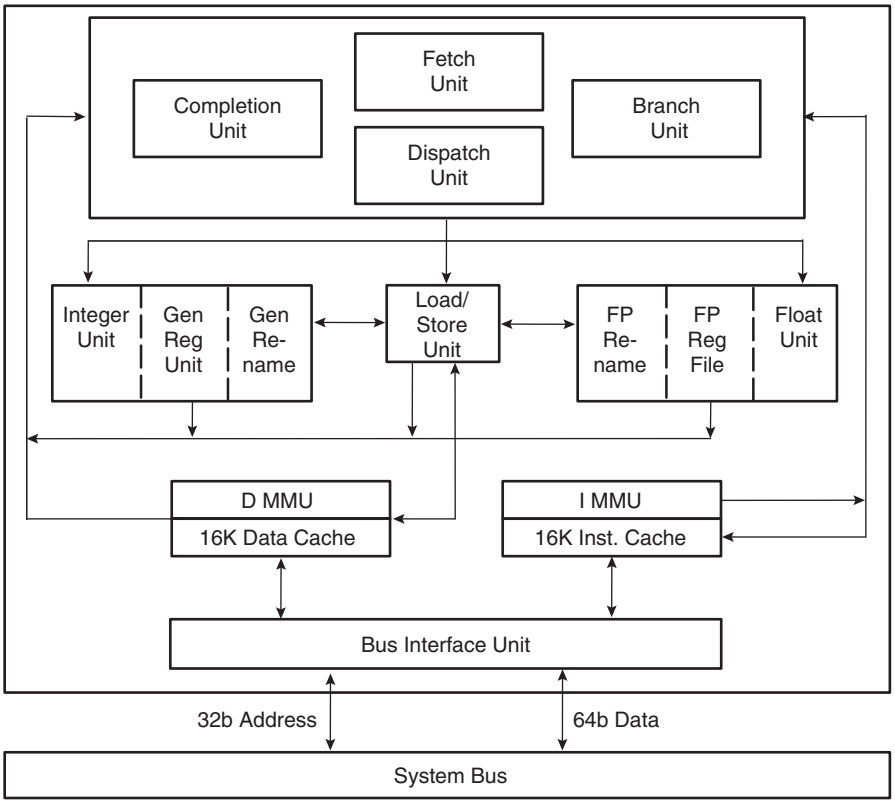
## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC 603e |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 200MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 110°C (TC) |
| Security Features | - |
| Package / Case | 255-BCBGA Exposed Pad |
| Supplier Device Package | 255-CBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/tspc603rvgu8lc |

## 3. Block Diagram

**Figure 3-1.** Block Diagram




## 4. Overview

The 603R is a low-power implementation of the PowerPC microprocessor family of Reduced Instruction Set Computing (RISC) microprocessors. The 603R implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603R provides four software controllable power-saving modes. Three of the modes (nap, doze, and sleep) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603R to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603R is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can be executed in any order for increased performance, but, the 603R makes completion appear sequential.

The 603e integrates five execution units:

- an Integer Unit (IU)
- a Floating-point Unit (FPU)
- a Branch Processing Unit (BPU)

## 7.1 Design and Construction

### 7.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in Table 10-2 on page 15, Table 10-4 on page 18, "Recommended Operating Conditions" on page 6, Figure 15-2 on page 49, Figure 15-4 on page 52 and Figure 5-1 on page 5.

### 7.1.2 *Lead Material and Finish*

Lead material and finish shall be as specified in MIL-STD-1835. (See "Package Mechanical Data" on page 47.)

## 7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only and functional operation at the maximum is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

### 7.2.1 Absolute Maximum Ratings for the 603R(1)(2)(3)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | -0.3 | 2.75 | V |
| PLL supply voltage | $AV_{DD}$ | -0.3 | 2.75 | V |
| I/O supply voltage | $OV_{DD}$ | -0.3 | 3.6 | V |
| Input voltage | $V_{IN}$ | -0.3 | 5.5 | V |
| Storage temperature range | $T_{STG}$ | -55 | +150 | °C |

Notes:
1. **Caution**: The input voltage must not be greater than $OV_{DD}$ by more than 2.5V at any time, including during power-on reset.
2. **Caution**: The $OV_{DD}$ voltage must not be greater than $V_{DD}/AV_{DD}$ by more than 1.2V at any time, including during power-on reset.
3. **Caution**: The $V_{DD}/AV_{DD}$ voltage must not be greater than $OV_{DD}$ by more than 0.4V at any time, including during power-on reset.

Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

### 7.2.2 Recommended Operating Conditions

The following are the recommended and tested operating conditions. Proper device operation outside of these ranges is not guaranteed.

### 7.2.3 Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 2.375 | 2.625 | V |
| PLL supply voltage | $AV_{DD}$ | 2.375 | 2.625 | V |
| I/O supply voltage | $OV_{DD}$ | 3.135 | 3.465 | V |
| Input voltage | $V_{IN}$ | GND | 5.5 | V |
| Operating temperature | $T_c$ | -55 | +125 | °C |
| Junction operating temperature specific to Cerquad | $T_j$ | – | +135 | °C |

### Sleep Mode

Sleep mode consumes the least amount of power of the four modes since all functional units are disabled. To conserve the maximum amount of power, the PLL may be disabled and the SYSCLK may be removed. Due to the fully static design of the 603R, the internal processor state is preserved when no internal clock is present. Because the time base and decrementer are disabled while the 603R is in sleep mode, the 603R's time base contents will have to be updated from an external time base following sleep mode if accurate time-of-day maintenance is required. Before the 603R enters the sleep mode, the 603R will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603R will enter the sleep mode.

In this mode:

- All functional units are disabled (including bus snooping and time base)
- All non-essential input receivers are disabled
  - Internal clock regenerators are disabled
  - The PLL is still running (see below)
- Sleep mode sequence
  - Set sleep bit (HID0[10] = 1)
  - 603R asserts quiesce request ($\overline{\text{QREQ}}$)
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$)
  - 603R enters sleep mode after several processor clocks
- There are several methods for returning to full-power mode
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, or $\overline{\text{MCP}}$ interrupts
  - Assert hard reset or soft reset
- The PLL may be disabled and SYSCLK may be removed while in sleep mode
- Return to full-power mode after PLL and SYSCLK disabled in sleep mode
  - Enable SYSCLK
  - Reconfigure PLL into the desired processor clock mode
  - System logic waits for PLL startup and relock time (100 µs)
  - System logic asserts one of the sleep recovery signals (for example, INT or SMI)

## 9.4 Power Management Software Considerations

Since the 603R is a dual issue processor with out-of-order execution capabilities, care must be taken with the way the power management mode is entered. Furthermore, nap and sleep modes require all outstanding bus operations to be completed before the power management mode is entered. Normally, during the system configuration time, one of the power management modes would be selected by setting the appropriate HID0 mode bit. Later on, the power management mode is invoked by setting the MSR[POW] bit. To provide a clean transition into and out of the power management mode, the **stmsr**[POW] should be preceded by a **sync** instruction and followed by an **isync** instruction.

## 9.5 Power Dissipation

**Table 9-2.** Power Dissipation[1][2][3][4] with $V_{DD}/AV_{DD}$ = 2.5 ±5%V, $OV_{DD}$ = 3.3 ±5%V, GND = 0V, 0°C ≤ $T_C$ ≤ 125°C

| | Cerquad 240 Package | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CPU Clock Frequency** | **166 MHz** | **200 MHz** | **166 MHz** | **200 MHz** | **233 MHz** | **266 MHz** | **300 MHz** | **Units** |
| **Full-on Mode (DPM Enabled)** | | | | | | | | |
| Typical | 2.1 | 2.5 | 2.1 | 2.5 | 3 | 3.5 | 4 | W |
| Max | 3.2 | 4 | 3.2 | 4 | 4.6 | 5.3 | 6 | W |
| **Doze Mode** | | | | | | | | |
| Typical | 1.5 | 1.7 | 1.5 | 1.7 | 1.8 | 2 | 2.1 | W |
| **Nap Mode** | | | | | | | | |
| Typical | 100 | 120 | 100 | 120 | 140 | 160 | 180 | mW |
| **Sleep Mode** | | | | | | | | |
| Typical | 96 | 110 | 96 | 110 | 123 | 135 | 150 | mW |
| **Sleep Mode-PLL Disabled** | | | | | | | | |
| Typical | 60 | 60 | 60 | 60 | 60 | 60 | 60 | mW |
| **Sleep Mode-PLL and SYSCLK Disabled** | | | | | | | | |
| Typical | 25 | 25 | 25 | 25 | 25 | 25 | 25 | mW |
| Maximum | 60 | 60 | 60 | 60 | 60 | 80 | 100 | mW |

Notes:
1. These values apply for all valid PLL_CFG[0-3] settings and do not include output driver power ($OV_{DD}$) or analog supply power ($AV_{DD}$). $OV_{DD}$ power is system dependent but is typically ≤ 10% of $V_{DD}$. Worst case $AV_{DD}$ = 15 mW.
2. Typical power is an average value measured at $V_{DD} = AV_{DD}$ = 2.5V, $OV_{DD}$ = 3.3V, in a system executing typical applications and benchmark sequences.
3. Maximum power is measured at $V_{DD}$ = 2.625V using a worst-case instruction mix.
4. To calculate the power consumption at low temperature (-55°C), **use a factor of 1.25.**

## 9.6 Marking

Each microcircuit is legible and permanently marked with at least the following information:

- Atmel logo
- Manufacturer's part number
- Class B identification if applicable
- Date code of inspection lot
- ESD identifier if available
- Country of manufacture

# 10. Pin Assignments

## 10.1 CBGA 255 and CI-CGA 255 Packages

Figure 10-1 (pin matrix) shows the pinout as viewed from the top of the CBGA and CI-CGA packages. The direction of the top surface view is shown by the side profile of the packages.

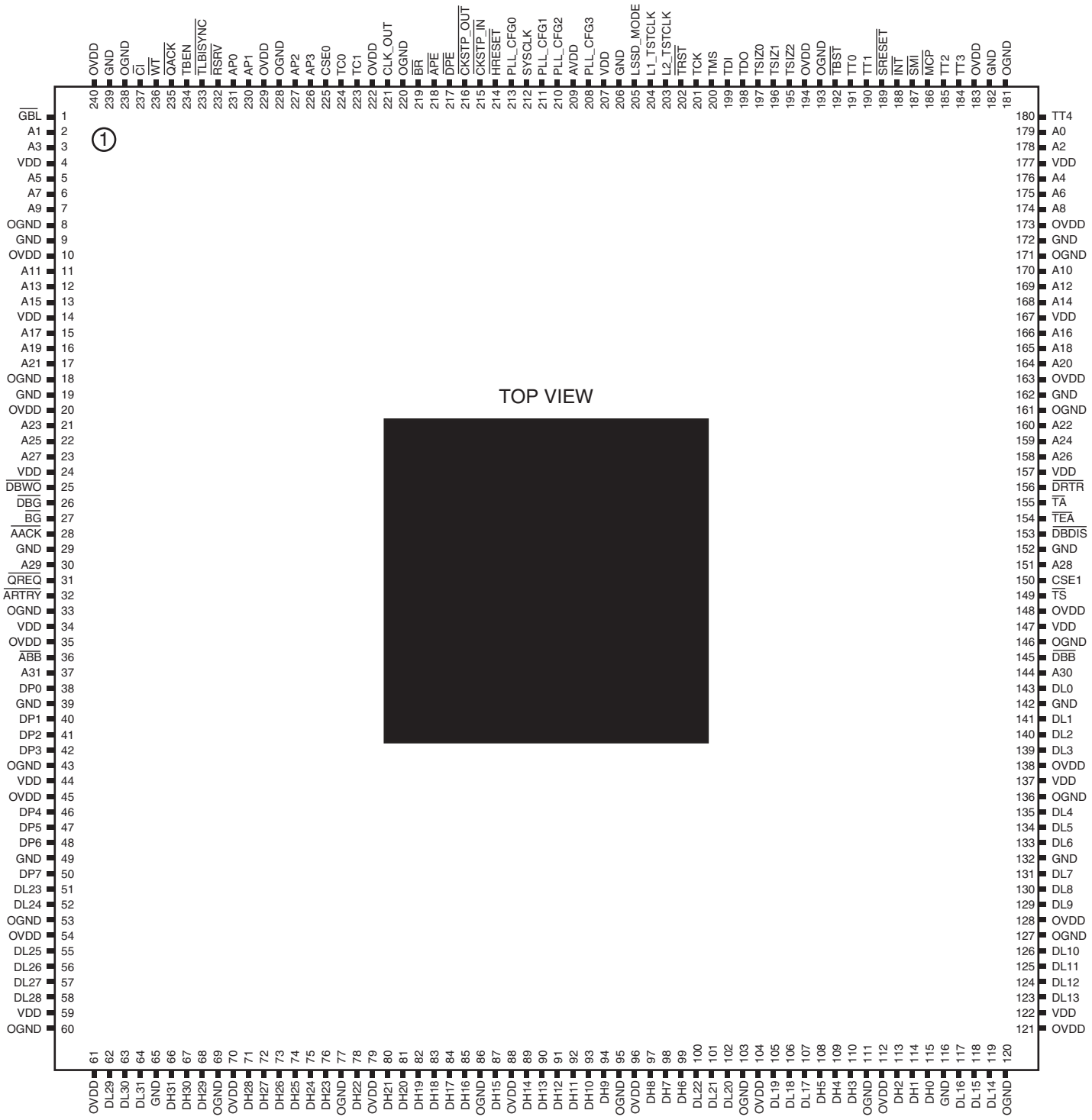
**Table 10-2.** Signal Pinout Listing (Continued)

| Signal Name | CBGA, HiTCE CBGA and CI-CGA Pin Number | Active | I/O |
|---|---|---|---|
| $\overline{\text{GBL}}$ | F01 | Low | I/O |
| $\overline{\text{HRESET}}$ | A07 | Low | Input |
| $\overline{\text{INT}}$ | B15 | Low | Input |
| L1_TSTCLK(1) | D11 | - | Input |
| L2_TSTCLK(1) | D12 | - | Input |
| $\overline{\text{LSSD\_MODE}}$(1) | B10 | Low | Input |
| $\overline{\text{MCP}}$ | C13 | Low | Input |
| PLL_CFG[0-3] | A08, B09, A09, D09 | High | Input |
| $\overline{\text{QACK}}$ | D03 | Low | Input |
| $\overline{\text{QREQ}}$ | J03 | Low | Output |
| $\overline{\text{RSRV}}$ | D01 | Low | Output |
| $\overline{\text{SMI}}$ | A16 | Low | Input |
| $\overline{\text{SRESET}}$ | B14 | Low | Input |
| SYSCLK | C09 | - | Input |
| $\overline{\text{TA}}$ | H14 | Low | Input |
| TBEN | C02 | High | Input |
| $\overline{\text{TBST}}$ | A14 | Low | I/O |
| TC[0-1] | A02, A03 | High | Output |
| TCK | C11 | - | Input |
| TDI | A11 | High | Input |
| TDO | A12 | High | Output |
| $\overline{\text{TEA}}$ | H13 | Low | Input |
| $\overline{\text{TLBISYNC}}$ | C04 | Low | Input |
| TMS | B11 | High | Input |
| $\overline{\text{TRST}}$ | C10 | Low | Input |
| $\overline{\text{TS}}$ | J13 | Low | I/O |
| TSIZ[0-2] | A13, D10, B12 | High | I/O |
| TT[0-4] | B13, A15, B16, C14, C15 | High | I/O |
| $\overline{\text{WT}}$ | D02 | Low | Output |
| NC | B07, B08, C03, C06, C08, D05, D06, F03, H04, J16 | Low | Input |
| VOLTDETGND(2) | F03 | Low | Output |

Notes: 1. These are test signals for factory use only and must be pulled up to $OV_{DD}$ for normal machine operation.
2. NC (not connected) in the 603e BGA package; internally tied to GND in the 603R BGA package to indicate to the power supply that a low-voltage processor is present.

## 10.2 CERQUAD 240 Package

**Figure 10-2.** CERQUAD 240: Top View



### 10.2.1 Pinout Listing

**Table 10-3.** Power and Ground Pins

| | CERQUAD Pin Number | |
|---|---|---|
| | **VCC** | **GND** |
| PLL ($AV_{DD}$) | 209 | |
| Internal Logic | 4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207 | 9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239 |
| Output Drivers | 10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240 | 8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238 |

**Table 10-4.** Signal Pinout Listing

| Signal Name | CERQUAD Pin Number |
|---|---|
| A[0-31] | 179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37 |
| $\overline{\text{AACK}}$ | 28 |
| $\overline{\text{ABB}}$ | 36 |
| AP[0-3] | 231,230,227,226 |
| $\overline{\text{APE}}$ | 218 |
| $\overline{\text{ARTRY}}$ | 32 |
| $\overline{\text{BG}}$ | 27 |
| $\overline{\text{BR}}$ | 219 |
| $\overline{\text{CI}}$ | 237 |
| $\overline{\text{CKSTP\_IN}}$ | 215 |
| $\overline{\text{CKSTP\_OUT}}$ | 216 |
| CLK_OUT | 221 |
| CSE[0-1] | 225,150 |
| $\overline{\text{DBB}}$ | 145 |
| $\overline{\text{DBG}}$ | 26 |
| $\overline{\text{DBDIS}}$ | 153 |
| $\overline{\text{DBWO}}$ | 25 |
| DH[0-31] | 115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66 |
| DL[0-31] | 143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64 |
| DP[0-7] | 38, 40, 41, 42, 46, 47, 48, 50 |
| $\overline{\text{DPE}}$ | 217 |
| $\overline{\text{DRTRY}}$ | 156 |
| $\overline{\text{GBL}}$ | 1 |
| $\overline{\text{HRESET}}$ | 214 |

**Table 10-4.** Signal Pinout Listing (Continued)

| Signal Name | CERQUAD Pin Number |
|---|---|
| $\overline{\text{INT}}$ | 188 |
| L1_TSTCLK[1] | 204 |
| L2_TSTCLK[1] | 203 |
| $\overline{\text{LSSD\_MODE}}$[1] | 205 |
| $\overline{\text{MCP}}$ | 186 |
| PLL_CFG[0-3] | 213, 211, 210, 208 |
| $\overline{\text{QACK}}$ | 235 |
| $\overline{\text{QREQ}}$ | 31 |
| $\overline{\text{RSRV}}$ | 232 |
| $\overline{\text{SMI}}$ | 187 |
| $\overline{\text{SRESET}}$ | 189 |
| SYSCLK | 212 |
| $\overline{\text{TA}}$ | 155 |
| TBEN | 234 |
| $\overline{\text{TBST}}$ | 192 |
| TC[0-1] | 224, 223 |
| TCK | 201 |
| TDI | 199 |
| TDO | 198 |
| $\overline{\text{TEA}}$ | 154 |
| $\overline{\text{TLBISYNC}}$ | 233 |
| TMS | 200 |
| $\overline{\text{TRST}}$ | 202 |
| $\overline{\text{TS}}$ | 149 |
| TSIZ[0-2] | 197, 196, 195 |
| TT[0-4] | 191, 190, 185, 184, 180 |
| $\overline{\text{WT}}$ | 236 |
| NC | |

Notes: 1. These are test signals for factory use only and must be pulled up to $V_{DD}$ for normal machine operation.
2. $OV_{DD}$ inputs supply power to the I/O drivers and $V_{DD}$ inputs supply power to the processor core. Future members of the 603 family may use different $OV_{DD}$ and $V_{DD}$ input levels.

**Table 10-6.** Signal Index for Cerquad, CBGA 255, HiTCE CBGA 255 and CI-CGA 255 Packages (Continued)

| Signal Name | Abbreviation | Signal Function | Signal Type |
|---|---|---|---|
| Transfer Start | $\overline{TS}$ | If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid<br>If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$) | I/O |
| Transfer Type | TT[0-4] | Type of transfer in progress | I/O |
| Write-through | $\overline{WT}$ | A single-beat transaction is write-through | Output |

# 11. Electrical Characteristics

## 11.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 11-1: Static electrical characteristics for the electrical variants
- Table 11-2: Dynamic electrical characteristics for the 603R

The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0 to PLL_CFG3 signals. All timings are respectively specified to the rising edge of SYSCLK.

These specifications are for 166 MHz to 300 MHz processor core frequencies for CBGA 255, HiTCE CBGA 255 and CI-CGA 255 packages and 166 MHz to 200 MHz processor core frequencies for the Cerquad 240 package.

## 11.2 Static Characteristics

**Table 11-1.** Electrical Characteristics with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

| Characteristics | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage (all inputs except SYSCLK) | | $V_{IH}$ | 2 | 5.5 | V |
| Input Low Voltage (all inputs except SYSCLK) | | $V_{IL}$ | GND | 0.8 | V |
| SYSCLK Input High Voltage | | $CV_{IH}$ | 2.4 | 5.5 | V |
| SYSCLK Input Low Voltage | | $CV_{IL}$ | GND | 0.4 | V |
| Input Leakage Current | $V_{IN}$ = 3.465V(1)(3) | $I_{IN}$ | - | 30 | µA |
| | $V_{IN}$ = 5.5V(1)(3) | $I_{IN}$ | - | 300 | µA |
| Hi-Z (off-state) Leakage Current | $V_{IN}$ = 3.465V(1)(3) | $I_{TSI}$ | - | 30 | µA |
| | $V_{IN}$ = 5.5V(1)(3) | $I_{TSI}$ | - | 300 | µA |
| Output High Voltage | $I_{OH}$ = -7 mA | $V_{OH}$ | 2.4 | - | V |
| Output Low Voltage | $I_{OL}$ = +7 mA | $V_{OL}$ | - | 0.4 | V |
| Capacitance, $V_{IN}$ = 0V, f = 1 MHz(2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | | $C_{IN}$ | - | 10 | pF |
| Capacitance, $V_{IN}$ = 0V, f = 1 MHz(2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$) | | $C_{IN}$ | - | 15 | pF |

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100% tested.

3. Leakage currents are measured for nominal $OV_{DD}$ and $V_{DD}$ or both $OV_{DD}$ and $V_{DD}$. Same variation (for example, both $V_{DD}$ and $OV_{DD}$ vary by either +5% or -5%)

## 11.3 Dynamic Characteristics

### 11.3.1 Clock AC Specifications

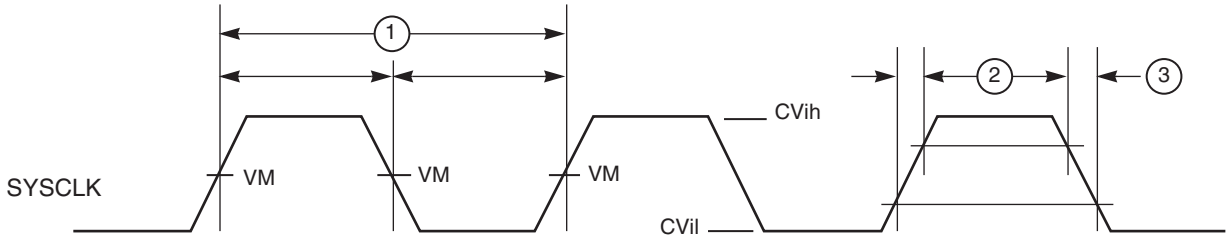
Table 11-2 provides the clock AC timing specifications as defined in Figure 11-1.

**Table 11-2.** Clock AC Timing Specifications[1][2][3][4] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $-55°C \le T_C \le 125°C$

| Figure Number | Characteristics | CBGA 255, HiTCE CBGA 255, CI-CGA 255 and CERQUAD | | | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 166 MHz | | 200 MHz | | 233 MHz | | 266 MHz | | 300 MHz | | Unit | Note |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| | Processor Frequency | 150 | 166 | 150 | 200 | 180 | 233 | 180 | 266 | 180 | 300 | MHz | [5] |
| | VCO Frequency | 300 | 332 | 300 | 400 | 360 | 466 | 360 | 532 | 360 | 600 | MHz | [5] |
| | SYSCLK (bus) Frequency | 25 | 66.7 | 33.3 | 66.7 | 33.3 | 75 | 33.3 | 75 | 33.3 | 75 | MHz | [5] |
| 1 | SYSCLK Cycle Time | 15 | 30 | 13.3 | 30 | 13.3 | 30 | 13.3 | 30 | 13.3 | 30 | ns | |
| 2,3 | SYSCLK Rise and Fall Time | – | 2 | – | 2 | – | 2 | – | 2 | – | 2 | ns | [1] |
| 4 | SYSCLK Duty Cycle (1.4V measured) | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | % | [3] |
| | SYSCLK Jitter | – | ±150 | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps | [2] |
| | 603R Internal PLL Relock Time | – | 100 | – | 100 | – | 100 | – | 100 | – | 100 | µs | [3][4] |

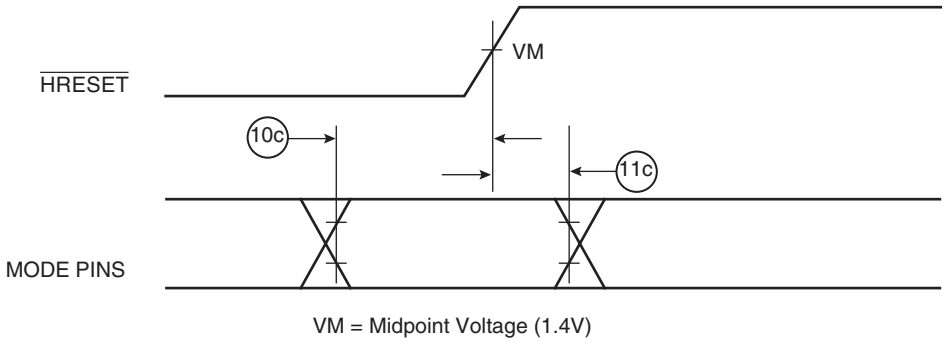
Notes:
1. Rise and fall times for the SYSCLK input are measured from 0.4V to 2.4V.
2. Cycle-to-cycle jitter is guaranteed by design.
3. Timing is guaranteed by design and characterization and is not tested.
4. The PLL relock time is the maximum amount of time required for PLL lock after a stable $V_{DD}$, $OV_{DD}$, $AV_{DD}$ and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen so that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description for valid PLL_CFG[0-3] settings.

**Figure 11-1.** SYSCLK Input Timing Diagram




VM = Midpoint Voltage (1.4V)

**Figure 11-3.** Mode Select Input Timing Diagram




### 11.3.3 Output AC Specifications

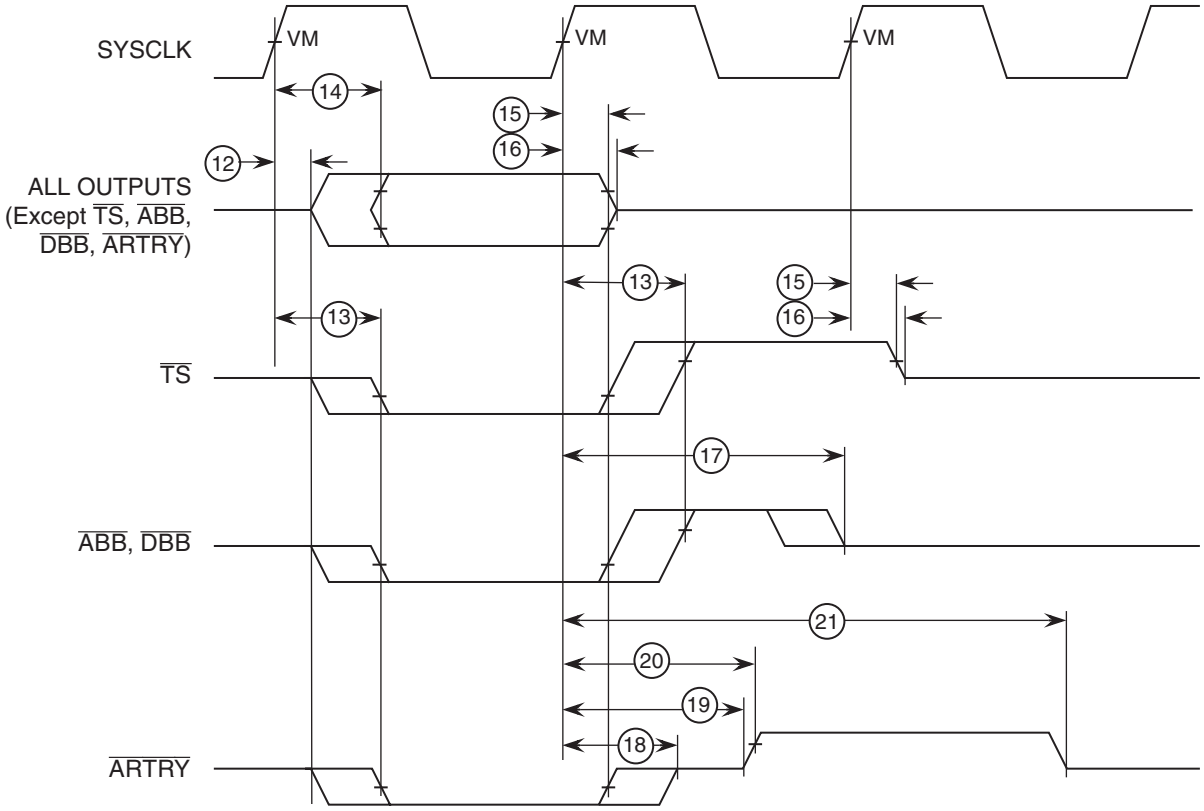
Table 11-4 provides the output AC timing specifications for the 603R (shown in Figure 11-4).

**Table 11-4.** Output AC Timing Specifications[1][2] with $V_{DD} = AV_{DD} = 2.5V \pm 5\%$; $OV_{DD} = 3.3 \pm 5\%V$, GND = 0V, $C_L = 50$ pF, $55°C \le T_C \le 125°C$

| Number | Characteristics | CBGA 255, HiTCE CBGA 255, CI-CGA 255 and Cerquad 240 Packages | | CBGA 255, HiTCE CBGA 255 and CI-CGA 255 | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 166, 200 MHz | | 233, 266 MHz | | 300 MHz | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| 12 | SYSCLK to output driven (output enable time) | 1 | – | 1 | – | 1 | – | ns | |
| 13a | SYSCLK to output valid (5.5V to 0.8V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 9 | – | 9 | – | 9 | ns | (4) |
| 13b | SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 8 | – | 8 | – | 8 | ns | (6) |
| 14a | SYSCLK to output valid (5.5V to 0.8V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 11 | – | 11 | – | 11 | ns | (4) |
| 14b | SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$) | – | 9 | – | 9 | – | 9 | ns | (6) |
| 15 | SYSCLK to output invalid (output hold) | 1 | – | 1 | – | 1 | – | ns | (3) |
| 16 | SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$) | – | 8.5 | – | 8 | – | 8 | ns | |
| 17 | SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge | – | 1 | – | 1 | – | 1 | $t_{SYSCLK}$ | (5)(7) |
| 18 | SYSCLK to $\overline{ARTRY}$ high impedance before precharge | – | 8 | – | 7.5 | – | 7.5 | ns | |
| 19 | SYSCLK to $\overline{ARTRY}$ precharge enable | 0.2 × $t_{SYSCLK}$ + 1 | – | 0.2 × $t_{SYSCLK}$ + 1 | – | 0.2 × $t_{SYSCLK}$ | – | ns | (3)(5) (8) |
| 20 | Maximum delay to $\overline{ARTRY}$ precharge | – | 1 | – | 1 | – | 1 | $t_{SYSCLK}$ | (5)(8) |
| 21 | SYSCLK to $\overline{ARTRY}$ high impedance after precharge | – | 2 | – | 2 | – | 2 | $t_{SYSCLK}$ | (6)(8) |

Notes:
1. All output specifications are measured from the 1.4V of the rising edge of SYSCLK to the TTL level (0.8V or 2V) of the signal in question. Both input and output timings are measured at the pin. See Figure 11-4.
2. All maximum timing specifications assume $C_L$ = 50 pF.
3. This minimum parameter assumes $C_L$ = 0 pF.
4. SYSCLK to output valid (5.5V to 0.8V) includes the extra delay associated with discharging the external voltage from 5.5V to 0.8V instead of from $V_{DD}$ to 0.8V (5V CMOS levels instead of 3.3V CMOS levels).
5. $t_{sysclk}$ is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (ns) of the parameter in question.
6. The output signal transitions from GND to 2V or $V_{DD}$ to 0.8V.
7. The nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 × tsysclk.
8. The nominal precharge width for $\overline{ARTRY}$ is 1 × tsysclk.

**Figure 11-4.** Output Timing Diagram




VM = Midpoint Voltage (1.4V)

**Figure 11-7.** Boundary-scan Timing Diagram

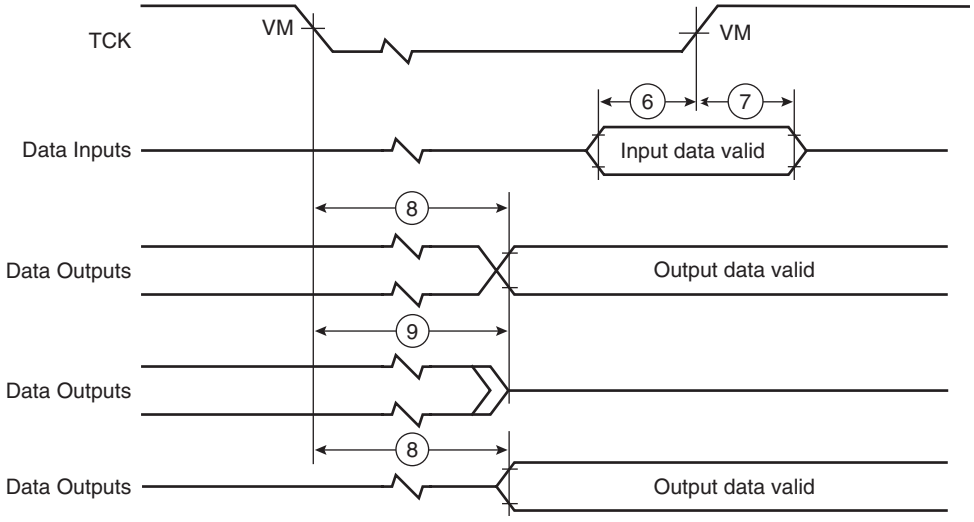
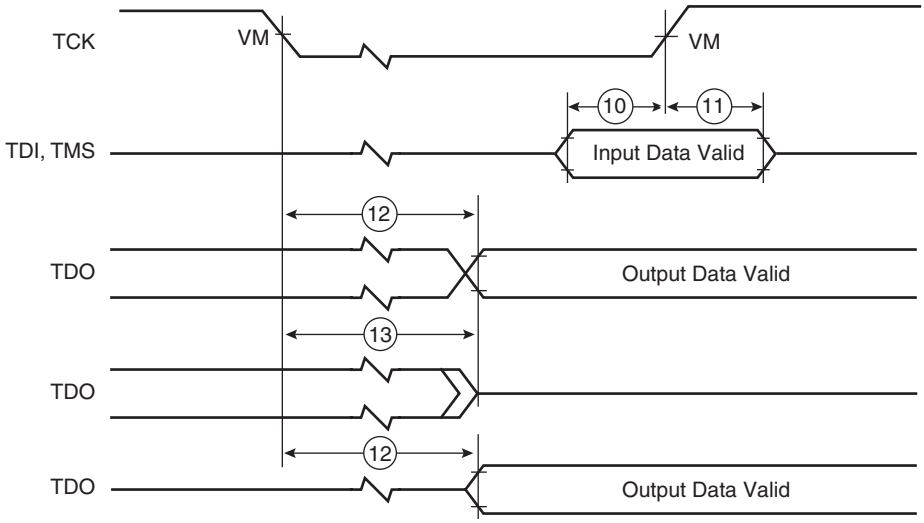



**Figure 11-8.** Test Access Port Timing Diagram




# 12. Functional Description

## 12.1 PowerPC Registers and Programming Model

The PowerPC architecture defines register-to-register operations for most computational instructions. Source operands for these instructions are accessed from the registers or are provided as immediate values embedded in the instruction opcode. The three-register instruction format allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory.

PowerPC processors have two levels of privilege—supervisor mode of operation (typically used by the operating system) and user mode of operation (used by the application software). The programming models incorporate 32 GPRs, 32 FPRs, Special-purpose Registers (SPRs) and several miscellaneous registers. Each PowerPC microprocessor also has its own unique set of Hardware Implementation (HID) registers.

– The Time Base register (TB) is a 64-bit register that maintains the time of day and operates interval timers. The TB consists of two 32-bit fields - Time Base Upper (TBU) and Time Base Lower (TBL).

– The Processor Version Register (PVR) is a 32-bit, read-only register that identifies the version (model) and revision level of the PowerPC processor.

– Block Address Translation (BAT) arrays - The PowerPC architecture defines 16 BAT registers, divided into four pairs of Data BATs (DBATs) and four pairs of instruction BATs (IBATs). See Figure 12-1 for a list of the SPR numbers for the BAT arrays.

The following supervisor-level SPRs are implementation-specific to the 603R:

– The DMISS and IMISS registers are read-only registers that are loaded automatically upon an instruction or data TLB miss.

– The HASH1 and HASH2 registers contain the physical addresses of the primary and secondary Page Table Entry Groups (PTEGs).

– The ICMP and DCMP registers contain a duplicate of the first word in the Page Table Entry (PTE) for which the table search is looking.

– The Required Physical Address (RPA) register is loaded by the processor with the second word of the correct PTE during a page table search.

– The hardware implementation (HID0 and HID1) registers provide the means for enabling the 603R's checkstops and features, and allows software to read the configuration of the PLL configuration signals.

– The Instruction Address Breakpoint Register (IABR) is loaded with an instruction address that is compared to instruction addresses in the dispatch queue. When an address match occurs, an instruction address breakpoint exception is generated.

Figure 12-1 shows all the 603R registers available at the user and supervisor level. The number to the right of the SPRs indicate the number that is used in the syntax of the instruction operands to access the register.

### 12.3.3 Exception Model

The following subsections describe the PowerPC exception model and the 603R implementation.

### 12.3.4 PowerPC Exception Model

The PowerPC exception mechanism allows the processor to change to supervisor state as a result of external singles, errors, or unusual conditions arising in the execution of instructions, and differ from the arithmetic exceptions defined by the IEEE for floating-point operations. When exceptions occur, information about the state of the processor is saved to certain registers and the processor begins execution at an address (exception vector) predetermined for each exception. Processing of exceptions occurs in supervisor mode.

Although multiple exception conditions can map to a single exception vector, a more specific condition may be determined by examining a register associated with the exception - for example, the DSISR and the FPSCR. Additionally, some exception conditions can be explicitly enabled or disabled by software.

The PowerPC architecture requires that exceptions be handled in program order; therefore, although a particular implementation may recognize exception conditions out of order, they are presented strictly in order. When an instruction-caused exception is recognized, any unexecuted instructions that appear earlier in the instruction stream, including any that have not yet entered the execute state, must be completed before the exception is taken. Any exceptions caused by such instructions are handled first. Likewise, exceptions that are asynchronous and precise are recognized when they occur, but are not handled until the instruction currently in the completion state successfully completes execution or generates an exception, and the completed store queue is emptied.

Unless a catastrophe event causes a system reset or machine check exception, only one exception is handled at a time. If, for example, a single instruction encounters multiple exception conditions, those conditions are encountered sequentially.

After the exception handler handles an exception, the instruction execution continues until the next exception condition is encountered. However, in many cases there is no attempt to re-execute the instruction. This method of recognizing and handling exception conditions sequentially guarantees that exceptions are recoverable.

Exception handlers should save the information stored in SRR0 and SRR1 early to prevent the program state from being lost due to a system reset and machine check exception or to an instruction-caused exception in the exception handler, and before enabling external interrupts.

The PowerPC architecture supports four types of exceptions:

- **Synchronous, Precise** – these are caused by instructions. All instruction-caused exceptions are handled precisely; that is, the machine state at the time the exception occurs is known and can be completely restored. This means that (excluding the trap and system call exceptions) the address of the faulting instruction is provided to the exception handler and that neither the faulting instruction nor subsequent instructions in the code stream will complete execution before the exception is taken. Once the exception is processed, execution resumes at the address of the faulting instruction (or at an alternate address provided by the exception handler). When an exception is taken due to a trap or system call instruction, execution resumes at an address provided by the handler.

## 15.2 CBGA Package Parameters

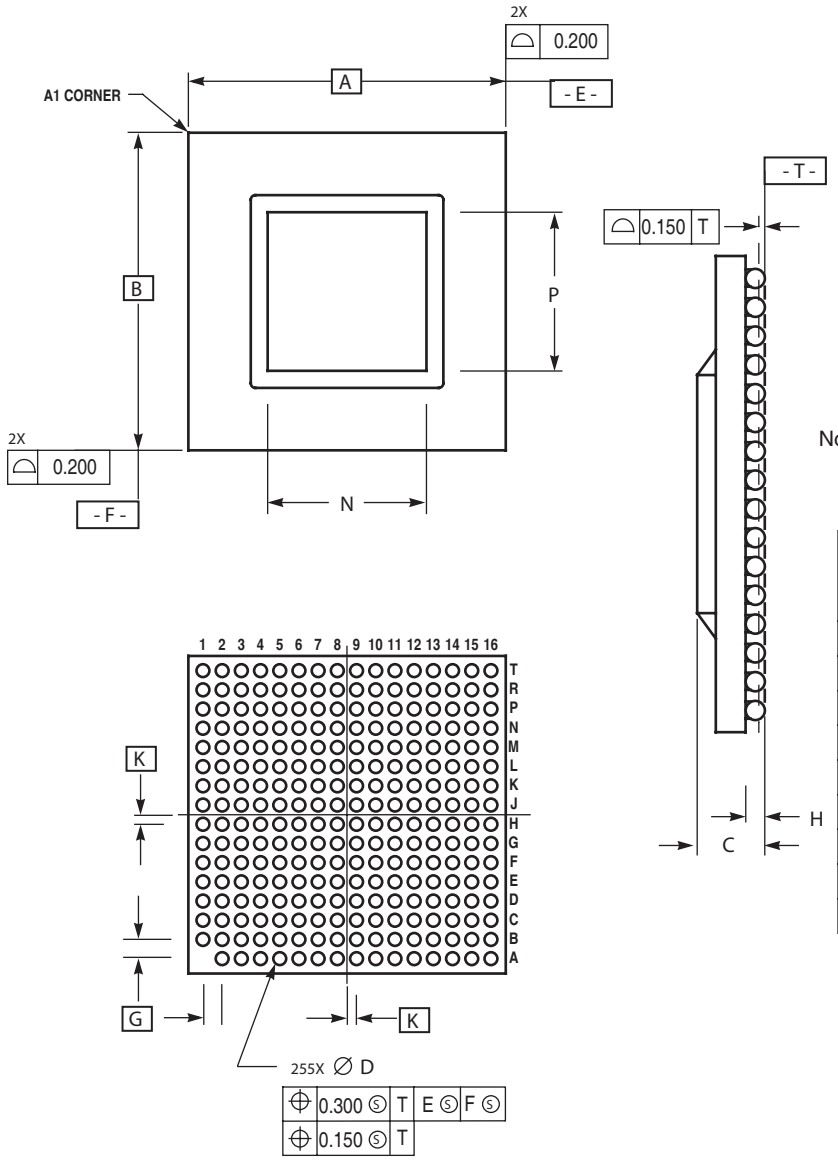
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead Ceramic Ball Grid Array (CBGA).

| | |
|---|---|
| Package outline | 21 mm × 21 mm |
| Interconnects | 255 |
| Pitch | 1.27 mm |
| Maximum module height | 3 mm |

### 15.2.1 Mechanical Dimensions of the CBGA Package

Figure 15-2 provides the mechanical dimensions and bottom surface nomenclature of the CBGA package.

**Figure 15-2.** Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package




Notes: 1. Dimensioning and tolerancing per ASME Y14.5M - 1994
2. controlling dimension: millimeter

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 21.000 BSC | | 0.827 BSC | |
| B | 21.000 BSC | | 0.827 BSC | |
| C | 2.450 | 3.000 | 0.097 | 0.118 |
| D | 0.820 | 0.930 | 0.032 | 0.036 |
| G | 1.270 BSC | | 0.050 BSC | |
| H | 0.790 | 0.990 | 0.031 | 0.039 |
| K | 0.635 BSC | | 0.025 BSC | |
| N | 5.000 | 16.000 | 0.197 | 0.630 |
| P | 5.000 | 16.000 | 0.197 | 0.630 |

## 15.3 CI-CGA Package Parameters

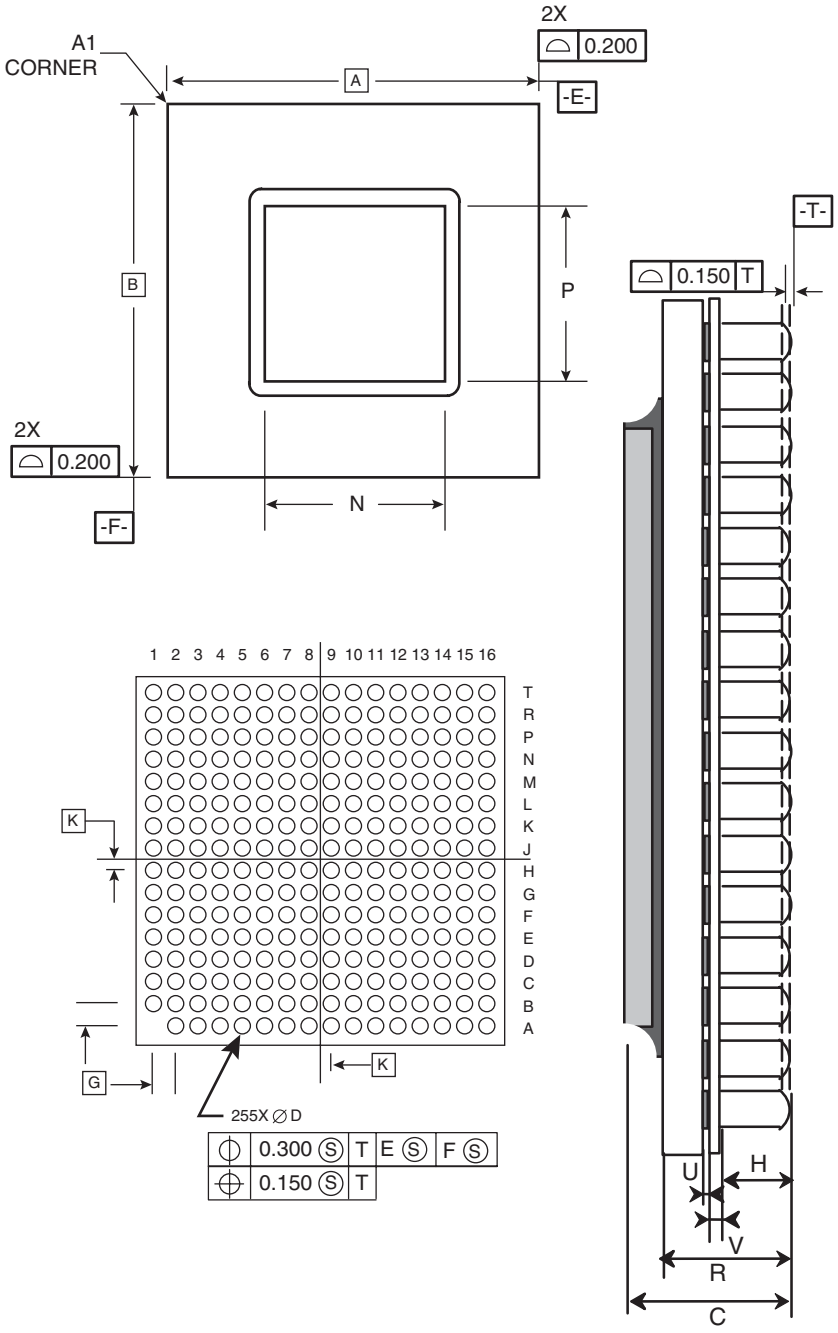
The package parameters are as provided in the following list. The package type is 21 mm, 255-lead ceramic ball grid array (CI-CGA).

| | |
|---|---|
| Package outline | 21 mm × 21 mm |
| Interconnects | 255 |
| Pitch | 1.27 mm |
| Typical module height | 3.84 mm |

### 15.3.1 Mechanical Dimensions of the CI-CGA Package

Figure 15-3 provides the mechanical dimensions and bottom surface nomenclature of the CI-CGA package.

**Figure 15-3.** Mechanical Dimensions and Bottom Surface Nomenclature of the CI-CGA Package

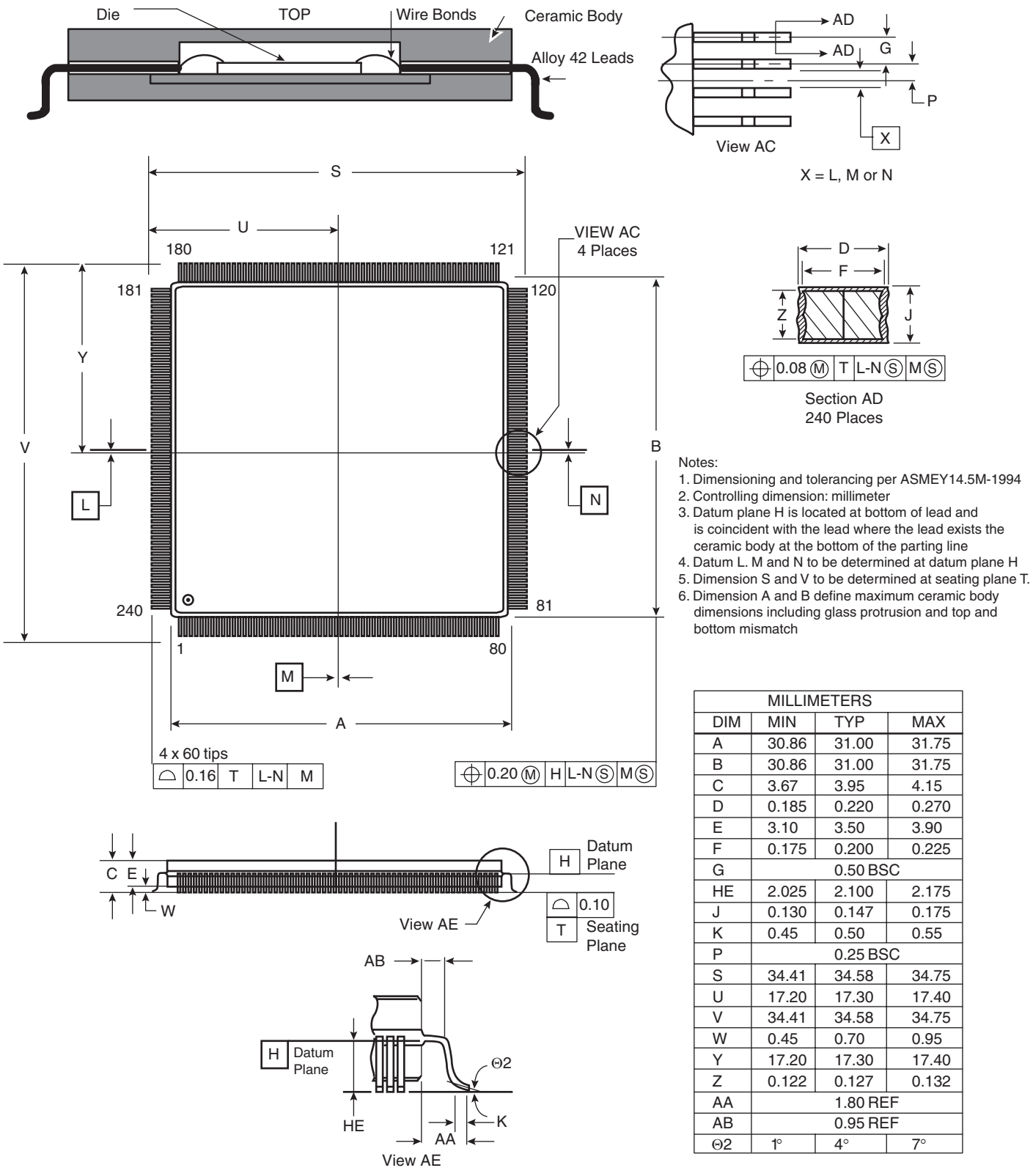



Notes: 1. Dimensioning and tolerancing per ASME Y14.5M—1994
2. Controlling dimension: millimeter

| Dim | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 21.000 BSC | |
| B | 21.000 BSC | |
| C | 3.84 BSC | |
| D | 0.790 | 0.990 |
| G | 1.270 BSC | |
| H | 1.545 | 1.695 |
| K | 0.635 BSC | |
| N | 5.000 | |
| P | 7.000 | |
| R | 3.02 BSC | |
| U | 0.10 BSC | |
| V | 0.25 | 0.35 |

## 15.4 CERQUAD 240 Package

**Figure 15-4.** Mechanical Dimensions of the Wire-bond CERQUAD Package




Notes:
1. Dimensioning and tolerancing per ASMEY14.5M-1994
2. Controlling dimension: millimeter
3. Datum plane H is located at bottom of lead and is coincident with the lead where the lead exists the ceramic body at the bottom of the parting line
4. Datum L. M and N to be determined at datum plane H
5. Dimension S and V to be determined at seating plane T.
6. Dimension A and B define maximum ceramic body dimensions including glass protrusion and top and bottom mismatch

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | TYP | MAX |
| A | 30.86 | 31.00 | 31.75 |
| B | 30.86 | 31.00 | 31.75 |
| C | 3.67 | 3.95 | 4.15 |
| D | 0.185 | 0.220 | 0.270 |
| E | 3.10 | 3.50 | 3.90 |
| F | 0.175 | 0.200 | 0.225 |
| G | | 0.50 BSC | |
| HE | 2.025 | 2.100 | 2.175 |
| J | 0.130 | 0.147 | 0.175 |
| K | 0.45 | 0.50 | 0.55 |
| P | | 0.25 BSC | |
| S | 34.41 | 34.58 | 34.75 |
| U | 17.20 | 17.30 | 17.40 |
| V | 34.41 | 34.58 | 34.75 |
| W | 0.45 | 0.70 | 0.95 |
| Y | 17.20 | 17.30 | 17.40 |
| Z | 0.122 | 0.127 | 0.132 |
| AA | | 1.80 REF | |
| AB | | 0.95 REF | |
| Θ2 | 1° | 4° | 7° |

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