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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79l632a25dl

6. MEMORY ORGANIZATION

The W79E(L)632 separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

The Program Memory on the standard 8052 can only be addressed to 64 Kbytes long. By invoking the banking methodology, W79E(L)632 can extend to two 64KB flash EPROM banks, APFlash0 and APFlash1. There are on-chip ROM banks which can be used similarly to that of the 8052. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region. There is an auxiliary 4KB Flash EPROM bank (LDFlash) resided user loader program for In-System Programming (ISP). Both APFlashs allow serial or parallel download according to user loader program in LDFlash.

Data Memory

The W79E(L)632 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, the W79E(L)632 contains on-chip 1K bytes MOVX SRAM of Data Memory, which can only be accessed by MOVX instructions. These 1K bytes of SRAM are between address 0000H and 03FFH. Access to the on-chip MOVX SRAM is optional under software control. When enabled by software, any MOVX instruction that uses this area will go to the on-chip RAM. MOVX addresses greater than 03FFH automatically go to external memory through Port 0 and 2. When disabled, the 1KB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000H and FFFFH goes to the expanded bus on Port 0 and 2. This is the default condition. In addition, the W79E(L)632 has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small. In the event that larger data contents are present, two selections can be used. One is on-chip MOVX SRAM, the other is the external Data Memory. The on-chip MOVX SRAM can only be accessed by a MOVX instruction, the same as that for external Data Memory. However, the on-chip RAM has the fastest access times.

Table 1. Special Function Register Location Table

F8	EIP							
F0	B							
E8	EIE							
E0	ACC							
D8	WDCON	PWMP	PWM0	PWM1	PWMCON1	PWM2	PWM3	
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4
C0				PWM5	PMR	STATUS		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR		ROMCON	SFRAL	SFRAH	SFDFD	SFRCN
A0	P2	XRAMAH	P4CSIN			P4		
98	SCON0	SBUF	P42AL	P42AH	P43AL	P43AH		CHPCON
90	P1		P4CONA	P4CONB	P40AL	P40AH	P41AL	P41AH
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

Note: The SFRs in the column with dark borders are bit-addressable.

A brief description of the SFRs is shown follows.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory. Besides, it has internal pull-up resisters enabled by setting P0UP of P4CSIN (A2H) to high.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the Scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7–0: Timer 1 LSB

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7–0: Timer 0 MSB

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7–0: Timer 1 MSB

Clock Control

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

WD1–0: Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.

WD1	WD0	Interrupt time-out	Reset time-out
0	0	2^{17}	$2^{17} + 512$
0	1	2^{20}	$2^{20} + 512$
1	0	2^{23}	$2^{23} + 512$
1	1	2^{26}	$2^{26} + 512$

T2M: Timer 2 clock select: When T2M is set to 1, timer 2 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.

T1M: Timer 1 clock select: When T1M is set to 1, timer 1 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.

T0M: Timer 0 clock select: When T0M is set to 1, timer 0 uses a divide by 4 clock, and when set to 0 it uses a divide by 12 clock.

MD2–0: Stretch MOVX select bits: These three bits are used to select the stretch value for the MOVX instruction. Using a variable MOVX length enables the user to access slower external memory devices or peripherals without the need for external circuits. The $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the selected interval. When accessing the on-chip SRAM, the MOVX instruction is always in 2 machine cycles regardless of the stretch setting. By default, the stretch has value of 1. If the user needs faster accessing, then a stretch value of 0 should be selected.

MD2	MD1	MD0	Stretch value	MOVX duration
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles *(Default)*
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7–0: General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. Some pins also have alternate input or output functions. This alternate functions are described below:

P1.0 : T2 External I/O for Timer/Counter 2
P1.1 : T2EX Timer/Counter 2 Capture/Reload Trigger

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

BIT NAME	FUNCTION
P4xM1, P4xM0	Port 4 alternate modes. =00: Mode 0. P4.x is a general purpose I/O port which is the same as Port 1. =01: Mode 1. P4.x is a Read Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =10: Mode 2. P4.x is a Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =11: Mode 3. P4.x is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0
P4xC1, P4xC0	Port 4 Chip-select Mode address comparison: =00: Compare the full address (16 bits length) with the base address registers P4xAH and P4xAL. =01: Compare the 15 high bits (A15-A1) of address bus with the base address registers P4xAH and P4xAL. =10: Compare the 14 high bits (A15-A2) of address bus with the base address registers P4xAH and P4xAL. =11: Compare the 8 high bits (A15-A8) of address bus with the base address registers P4xAH and P4xAL.

P4.0 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P40AL Address: 94h

P4.0 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P40AH Address: 95h

P4.1 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P41AL Address: 96h

P4.1 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P41AH Address: 97h

Slave Address

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADDR Address: A9h

SADDR: The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

ROM Banking Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	EN128K	DCP12	DCP11	DCP10

Mnemonic: ROMCON Address: ABh

EN128K: On-chip ROM banking enable. Set this bit to enable APFlash0 and APFlash1 by banking mechanism. The P1.x is selected to be the auxiliary highest address line A16.

DCP1x: A16 selection. By default, P1.7 is defined as A16.

A16	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
DCP12	0	0	0	0	1	1	1	1
DCP11	0	0	1	1	0	0	1	1
DCP10	0	1	0	1	0	1	0	1

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: SFRAL Address: ACh

Low byte destination address for In System Programming operation. SFRAH and SFRAL address a specific ROM byte for erasure, programming or read.

ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: SFRAH Address: ADh

High byte destination address for In System Programming operation. SFRAH and SFRAL address a specific ROM byte for erasure, programming or read.

Status Register

Bit:	7	6	5	4	3	2	1	0
	-	HIP	LIP	-	-	-	-	-

Mnemonic: STATUS Address: C5h

HIP: High Priority Interrupt Status. When set, it indicates that software is servicing a high priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.

LIP: Low Priority Interrupt Status. When set, it indicates that software is servicing a low priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.

Timed Access

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TfA.0

Mnemonic: TA Address: C7h

TA: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / $\overline{T2}$	CP / $\overline{RL2}$

Mnemonic: T2CON Address: C8h

TF2: Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down count mode. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.

EXF2: Timer 2 External Flag: A negative transition on the T2EX pin (P1.1) or timer 2 overflow will cause this flag to set based on the CP / $\overline{RL2}$, EXEN2 and DCEN bits. If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on T2EX pin will force a timer interrupt if enabled.

RCLK: Receive Clock Flag: This bit determines the serial port 0 time-base when receiving data in serial modes 1 or 3. If it is 0, then timer 1 overflow is used for baud rate generation, otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.

TCLK: Transmit Clock Flag: This bit determines the serial port 0 time-base when transmitting data in modes 1 and 3. If it is set to 0, the timer 1 overflow is used to generate the baud rate clock otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.

EXEN2: Timer 2 External Enable. This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud clocks for the serial port. If this bit is 0, then the T2EX pin will be ignored, otherwise a negative transition detected on the T2EX pin will result in capture or reload.

Timer 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2: Timer 2 LSB

Timer 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TH2: Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

CY: Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.

AC: Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.

F0: User flag 0: General purpose flag that can be set or cleared by the user.

RS.1-0: Register bank select bits:

RS1	RS0	Register bank	Address
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

OV: Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.

F1: User Flag 1: General purpose flag that can be set or cleared by the user by software.

P: Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

Watchdog Control

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	-	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON Address: D8h

POR: Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.

WDIF: Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.

WTRF: Watchdog Timer Reset Flag. Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the watchdog timer will have no affect on this bit.

EWT: Enable Watchdog timer Reset. Setting this bit will enable the Watchdog timer Reset function.

RWT: Reset Watchdog Timer. This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```
TA          EG      C7H
WDCON       REG     D8H
CKCON       REG     8EH
        MOV  TA, #AAH
        MOV  TA, #55H

        SETB  WDCON.0               ; Reset watchdog timer
        ORL  CKCON, #11000000B      ; Select 26 bits watchdog timer
        MOV  TA, #AAH
        MOV  TA, #55H
        ORL  WDCON, #00000010B      ; Enable watchdog
```

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

7. INSTRUCTION

The W79E(L)632 executes all the instructions of the standard 8032 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W79E(L)632, each machine cycle consists of 4 clock periods, while in the standard 8032 it consists of 12 clock periods. Also, in the W79E(L)632 there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8032 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the W79E(L)632 has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W79E(L)632 reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8032.

7.1 Instruction Timing

The instruction timing for the W79E(L)632 is an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the W79E(L)632 and the standard 8032. In the W79E(L)632 each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2 C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the W79E(L)632 does one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the W79E(L)632 are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8032, the MOVX instruction is always two machine cycles long. However in the W79E(L)632, the user has a facility to stretch the duration of this instruction from 2 machine cycles to 9 machine cycles. The $\overline{RD}$ and $\overline{WR}$ strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. The rest of the instructions are either three, four or five machine cycle instructions. Note that in the W79E(L)632, based on the number of machine cycles, there are five different types, while in the standard 8032 there are only three. However, in the W79E(L)632 each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8032. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8032 in terms of clock periods.

Auto-reload Mode, Counting Up/Down

Timer/Counter 2 will be in auto-reload mode as an up/down counter if CP / $\overline{RL2}$ bit in T2CON is cleared and the DCEN bit in T2MOD is set. In this mode, Timer/Counter 2 is an up/down counter whose direction is controlled by the T2EX pin. A 1 on this pin cause the counter to count up. An overflow while counting up will cause the counter to be reloaded with the contents of the capture registers. The next down count following the case where the contents of Timer/Counter equal the capture registers will load an FFFFh into Timer/Counter 2. In either event a reload will set the TF2 bit. A reload will also toggle the EXF2 bit. However, the EXF2 bit can not generate an interrupt while in this mode.

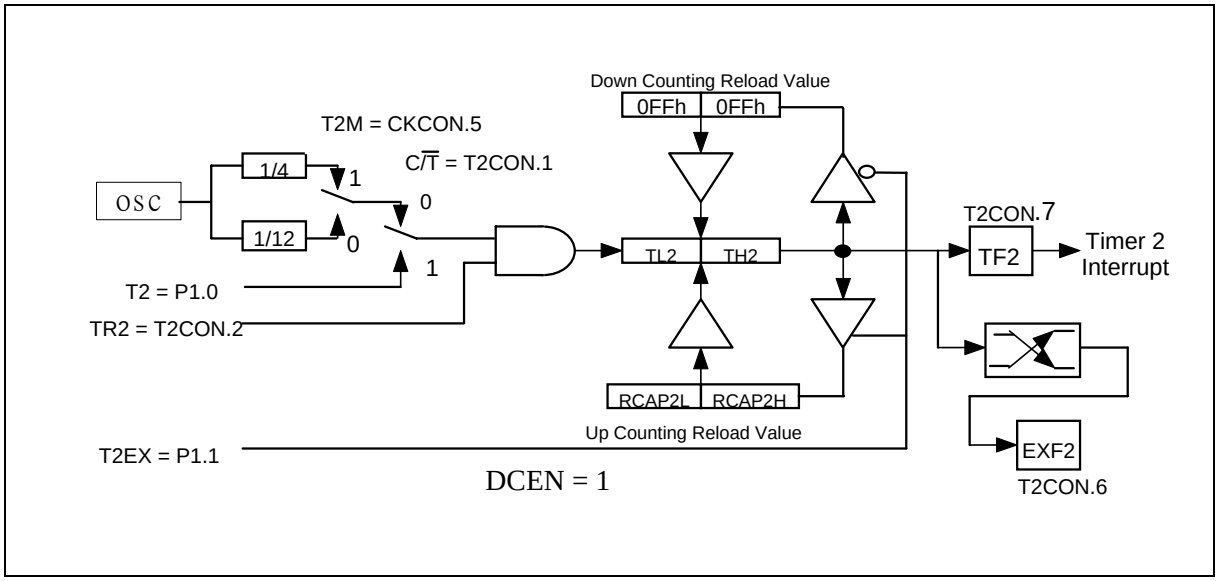


Figure 16. 16-Bit Auto-reload Up/Down Counter

Watchdog Control

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the watchdog timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWT = 0, then this bit will not be affected by the watchdog timer.

EWT: WDCON.1 - Enable Watchdog timer Reset. This bit when set to 1 will enable the Watchdog timer reset function. Setting this bit to 0 will disable the Watchdog timer reset function, but will leave the timer running.

RWT: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog timer reset is enabled, then the RWT has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog timer reset will occur.

Clock Control

WD1, WD0: CKCON.7, CKCON.6 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clock longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The EWT, WDIF and RWT bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the watchdog timer. Please refer as below demo program.

```
        org     63h
        mov     TA,#AAH
        mov     TA,#55H
        clr     WDIF
        jnb     execute_reset_flag,bypass_reset     ; Test if CPU need to reset.
        jmp     $                                   ; Wait to reset
bypass_reset:
        mov     TA,#AAH
        mov     TA,#55H
        setb    RWT
        reti

        org     300h
```

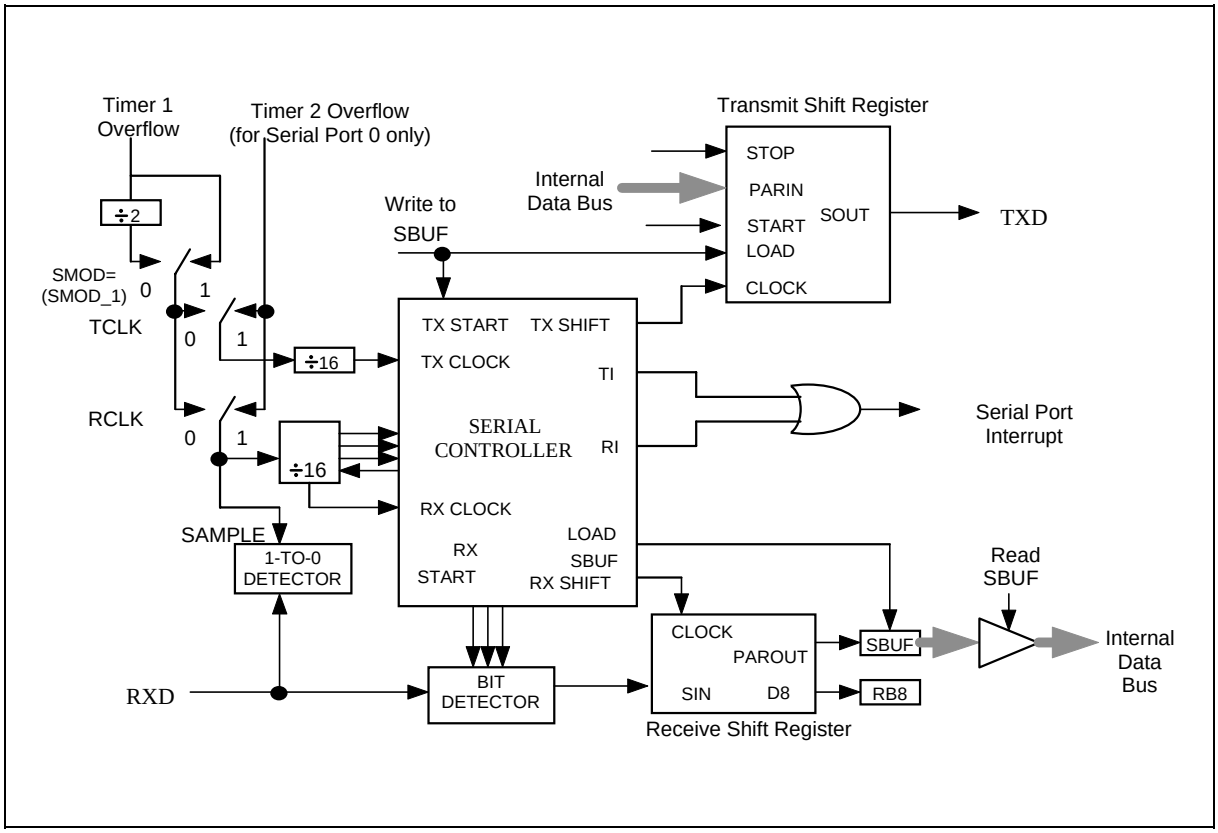


Figure 21. Serial Port Mode 1

Mode 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

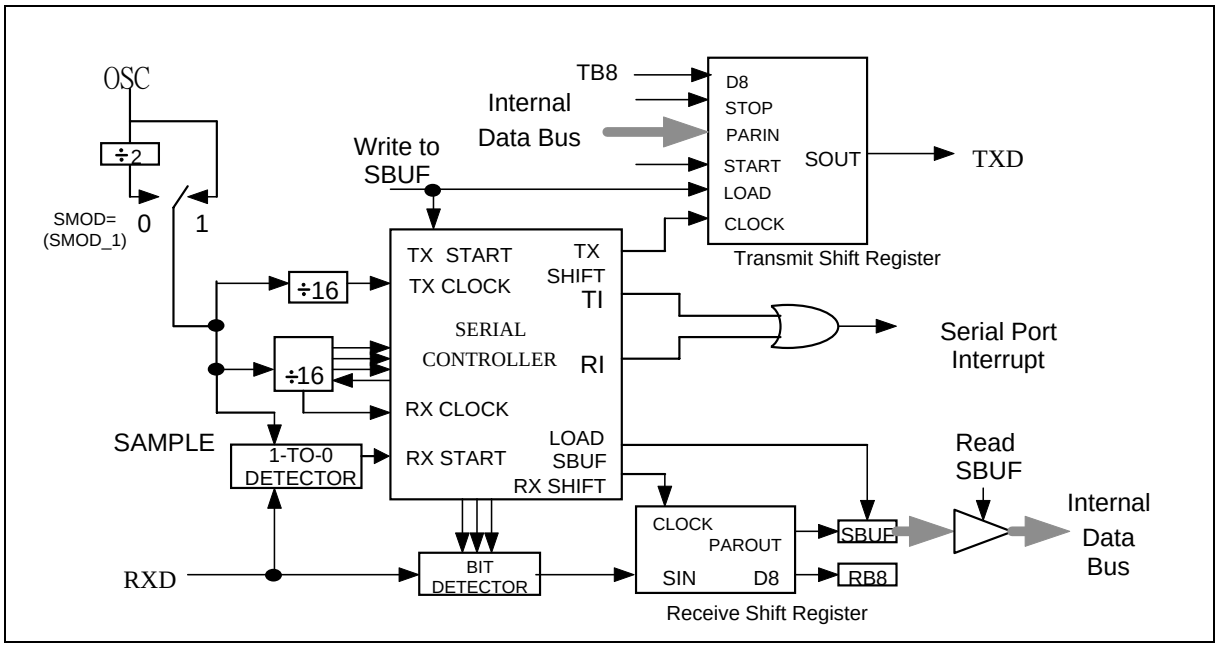


Figure 22. Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

12. TIMED ACCESS PROTECTION

The W79E(L)632 has several new features, like the Watchdog timer, on-chip ROM size adjustment, wait state control signal and Power on/fail reset flag, which are crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E(L)632 has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access(TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG    0C7h          ;define new register TA, located at 0C7h
MOV     TA, #0AAh
MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
MOV     TA, #0AAh       3 M/C
MOV     TA, #055h       3 M/C
MOV     WDCON, #00h     3 M/C
```

Note: M/C = Machine Cycles

Example 2: Valid access

```
MOV     TA, #0AAh       3 M/C
MOV     TA, #055h       3 M/C
NOP                     1 M/C
SETB    EWT             2 M/C
```

Example 3: Valid access

```
MOV     TA, #0Aah       3 M/C
MOV     TA, #055h       3 M/C
ORL     WDCON, #00000010B  3M/C
```

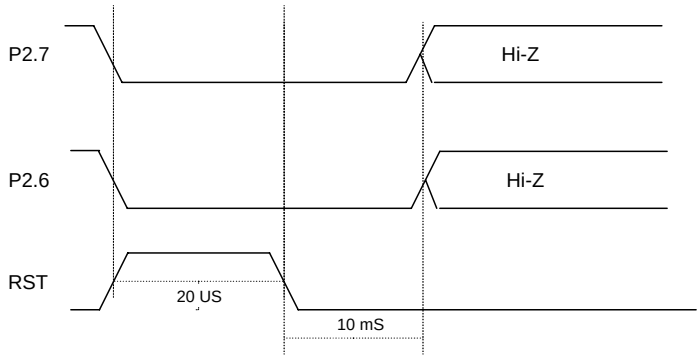
13. H/W REBOOT MODE (BOOT FROM 4K BYTES OF LDFLASH)

The W79E(L)632 boots from APFlash program (64K bytes) by default at the external reset. On some occasions, user can force W79E(L)632 to boot from the LDFlash program (4K bytes) at the external reset. The settings for this special mode is as follow. It is necessary to add 10K resistor on these P2.6, P2.7 and P4.3 pins.

Reboot Mode

OPTION BITS	RST	P4.3	P2.7	P2.6	MODE
Bit4 L	H	X	L	L	REBOOT
Bit5 L	H	L	X	X	REBOOT

The Reset Timing For Entering REBOOT Mode



Notes:

1. The possible situation that you need to enter REBOOT mode is when the APFlash program can not run normally and W79E(L)632 can not jump to LDFlash to execute on chip programming function. Then you can use this REBOOT mode to force the CPU jump to LDFlash and run on chip programming procedure. When you design your system, you can connect the pins P26, P27 to switches or jumpers. For example in a CD ROM system, you can connect the P26 and P27 to PLAY and EJECT buttons on the panel. When the APFlash program is fail to execute the normal application program. User can press both two buttons at the same time and then switch on the power of the personal computer to force the W79E(L)632 to enter the REBOOT mode. After power on of personal computer, you can release both PLAY and EJECT button. And re-run the on chip programming procedure to let the APFlash have the normal program code. Then you can back to normal condition of CD ROM.

2: In application system design, user must take care the P4.3, P2, P3, ALE, /EA and /PSEN pin value at reset to avoid W79E(L)632 entering the programming mode or REBOOT mode in normal operation.

14. IN-SYSTEM PROGRAMMING

14.1 The Loader Program Locates at LDFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #03H value before CPU has entered idle state. CPU will switch to LDFlash memory and execute a reset action. H/W reboot mode will switch to LDFlash memory, too. Set SFRCN register where it locates at user's loader program to update APFlash bank 0 or bank 1 memory. Set a SWRESET (CHPCON.7) to switch back APFlash after CPU has updated APFlash program. CPU will restart to run program from reset state.

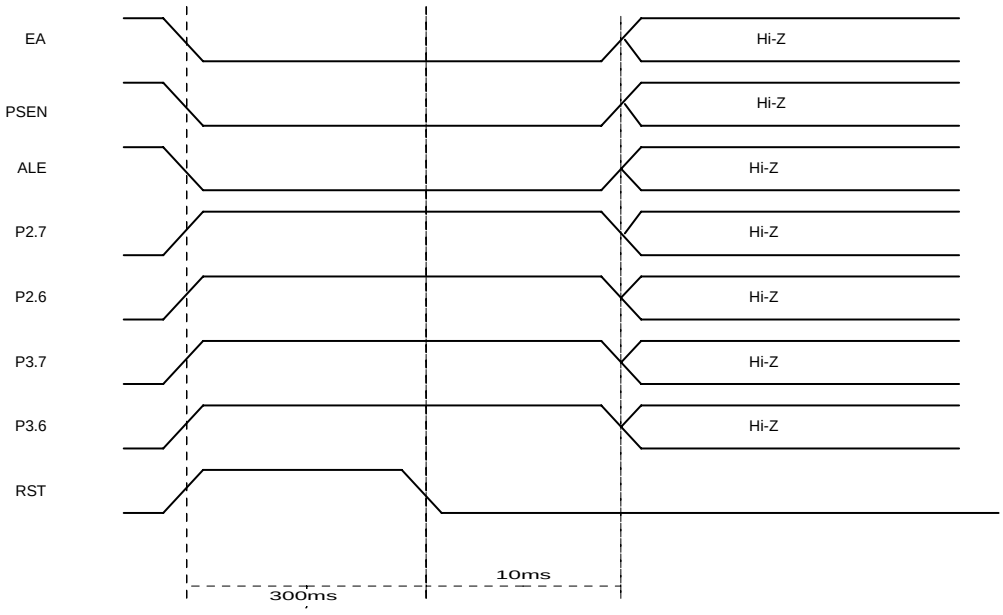
14.2 The Loader Program Locates at APFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #01H value before CPU has entered idle state. Set SFRCN register to update LDFlash or another bank of APFlash program. CPU will continue to run user's APFlash program after CPU has updated program. Please refer demonstrative code to understand other detail description.

15. H/W WRITER MODE

This mode is for the writer to write / read Flash EPROM operation. A general user may not enter this mode.

The Timing For Entering Flash EPROM Mode on the Programmer



17. ELECTRICAL CHARACTERISTICS

17.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	+70	°C
Storage Temperature	Tst	-55	+150	°C

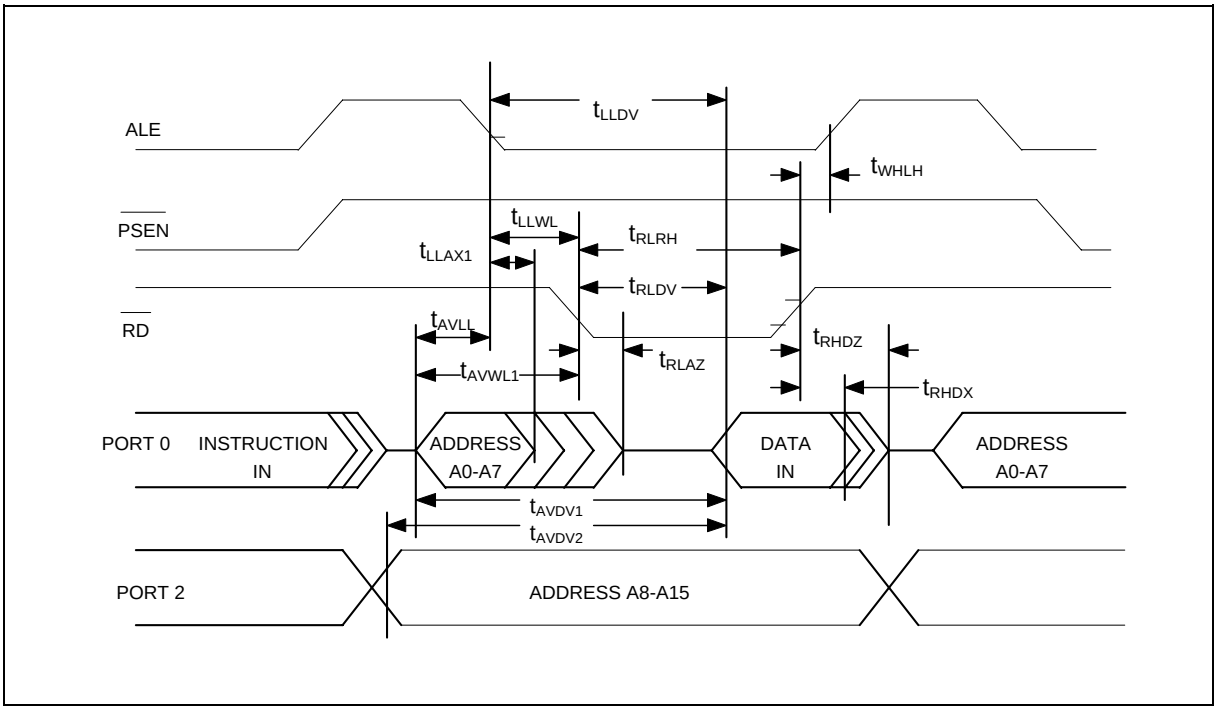
Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

17.2 DC Characteristics

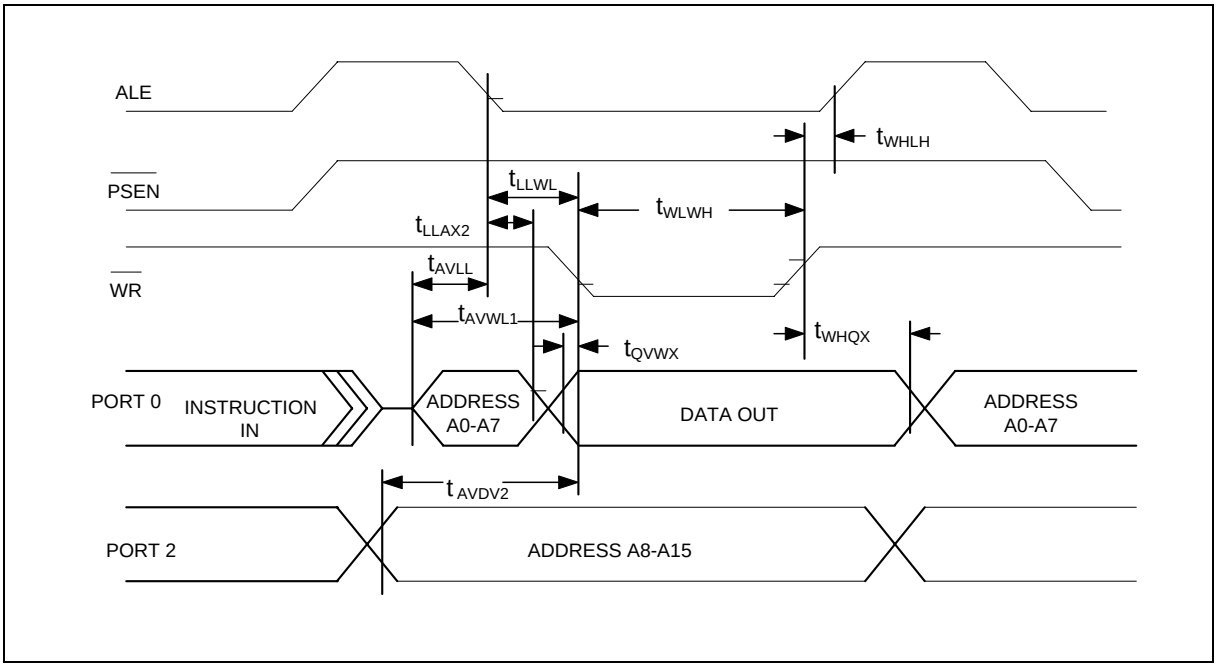
(T_A = 25°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	3.0	5.5	V	V_{DD} >4.5V→Fosc < = 40 MHz V_{DD} >3.0V→Fosc < = 20 MHz
Operating Current	I_{DD}	-	30	mA	V_{DD} = 5.5V, Fosc = 20 MHz
			10	mA	V_{DD} = 3.3V, Fosc = 12 MHz
Idle Current	I_{IDLE}	-	18	mA	V_{DD} = 5.5V, Fosc=20 MHz
			6	mA	V_{DD} = 3.3V, Fosc=12 MHz
Power Down Current	I_{PWDN}	-	10	µA	V_{DD} = 3.3 ~ 5.5V
Input Current P1, P2, P3	I_{IN1}	-50	+10	µA	V_{DD} = 3.3 ~ 5.5V V_{IN} = 0V or V_{DD}
Input Current RST[*1]	I_{IN2}	-	1000	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
		-	500	µA	V_{DD} = 3.3V, 0<V_{IN}<V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 3.3 ~ 5.5V 0V<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3	I_{TL}[*4]	-500	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
		-250	-50	µA	V_{DD} = 3.3V V_{IN} = 1.0V
Input Low Voltage P0, P1, P2, P3, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
		0	0.5	V	V_{DD} =3.3V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
		0	0.5	V	V_{DD} = 3.3V
Input Low Voltage XTAL1[*3]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
		0	0.5	V	V_{DD} = 3.3V

17.3.4 Data Memory Read Cycle



17.3.5 Data Memory Write Cycle



```
READ_VERIFY_64K:
        MOV  SFRAL,R2           ; SFRAL = LOW ADDRESS
        MOV  TCON,#10H          ; TCON = 10H, TR0 = 1,GO
        MOV  PCON,#01H
        INC  R2
        MOVX  A,@DPTR
        INC  DPTR
        CJNE  A,SFRFD,ERROR_64K
        CJNE  R2,#0H,READ_VERIFY_64K
        INC  R1
        MOV  SFRAH,R1
        CJNE  R1,#0H,READ_VERIFY_64K

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
        MOV  TA,#AAH
        MOV  TA,#55H
        MOV  CHPCON,#83H        ; SOFTWARE RESET. CPU will restart from APFlash0

ERROR_64K:
        DJNZ  R4,UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
.                               ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
                .
                .
                .
```