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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c0712pecr51ya

GENERAL DESCRIPTION (Continued)

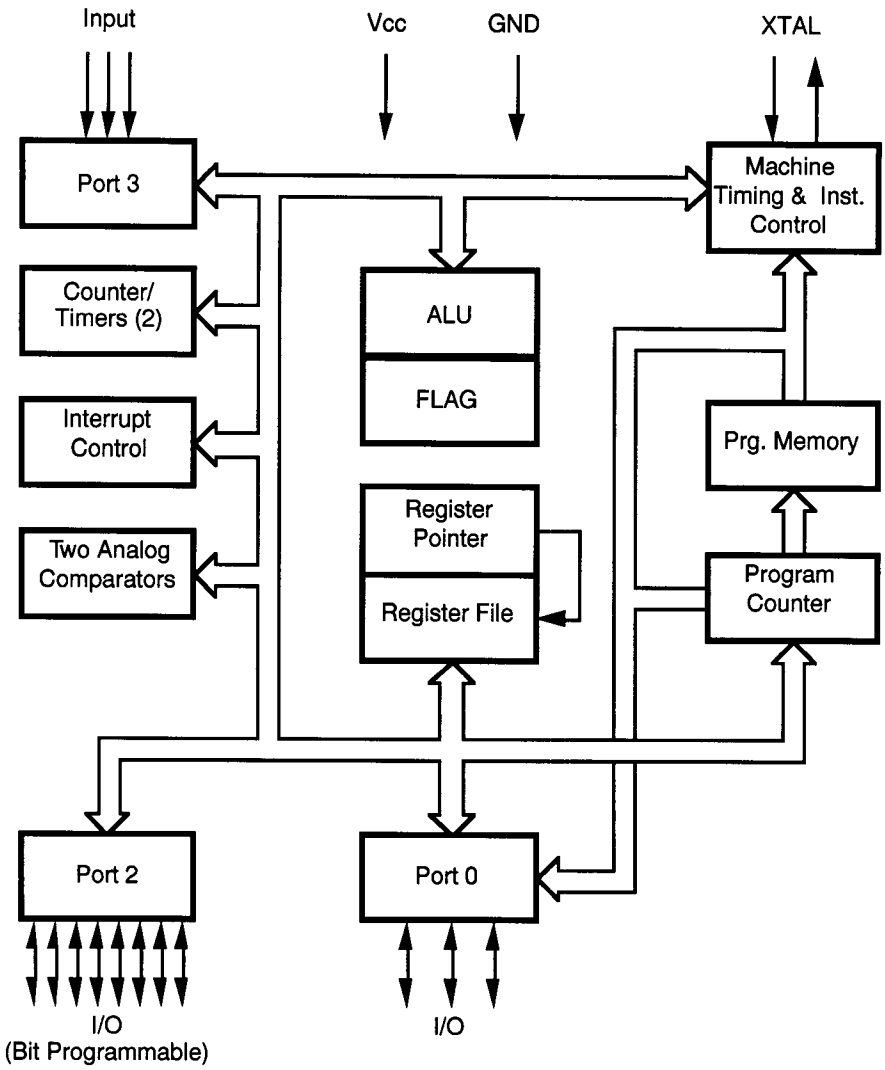


Figure 1. Z86C05/C07 Functional Block Diagram

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70° Min	T_A = 0°C to +70° Max	T_A = −40°C to +105° Min	T_A = −40°C to +105° Max	Typical @ 25°C	Units	Conditions	Note
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	Vss–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		1
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		1
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V		1
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V		1
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	I_{OH} = –2.0 mA	5
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		3.0V	V_{CC}–0.4		V_{CC}–0.4		3.0	V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	5
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	5
		3.0V		0.4		0.4	0.2	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA	5
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA	5
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		
		5.5V		25		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		2.2	2.8			2.6	V	Int. CLK Freq @ 6 MHz Max.	
					2.0	3.0	2.6		Int. CLK Freq @ 4 MHz Max.	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	

DC ELECTRICAL CHARACTERISTICS (CONT.)

			T_A = 0°C to +70°C		T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC} [4]**	**Min**	**Max**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**	**Note**
I_{OL}	Output Leakage	3.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	
		5.5V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = OV, V_{CC}	
V_{VICR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0	0	V_{CC} –1.5		V		
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		2.5		2.5	0.7	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	
		5.5V		4.0		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	
		3.0V		3.0		3.0	0.9	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	
		5.5V		4.5		4.5	2.8	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	
		3.0V		4.0		4.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	
		5.5V		5.0		5.0	3.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP mode V_{IN} = OV, V_{CC} WDT is not Running	
		5.5V		10		20	1.0	µA	STOP mode V_{IN} = OV, V_{CC} WDT is not Running	
I_{ALL}	Auto Latch Low Current	3.0V		12		8.0	3.0	µA	OV < V_{IN} < V_{CC}	
		5.5V		32		30	16	µA	OV < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	3.0V		–8		-5.0	-1.5	µA	OV < V_{IN} < V_{CC}	
		5.5V		–16		-20	-8.0	µA	OV < V_{IN} < V_{CC}	

Notes:

1. Port 0, 2, and 3 only.
2. V_{SS} = 0V = GND.
3. The device operates down to V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
5. Standard Mode (not Low EMI mode).
6. Z86C07/C08 only.
7. CL1 = 100 pF, CL2 = 220 pF, RF = 30 kOhm

AC ELECTRICAL CHARACTERISTICS

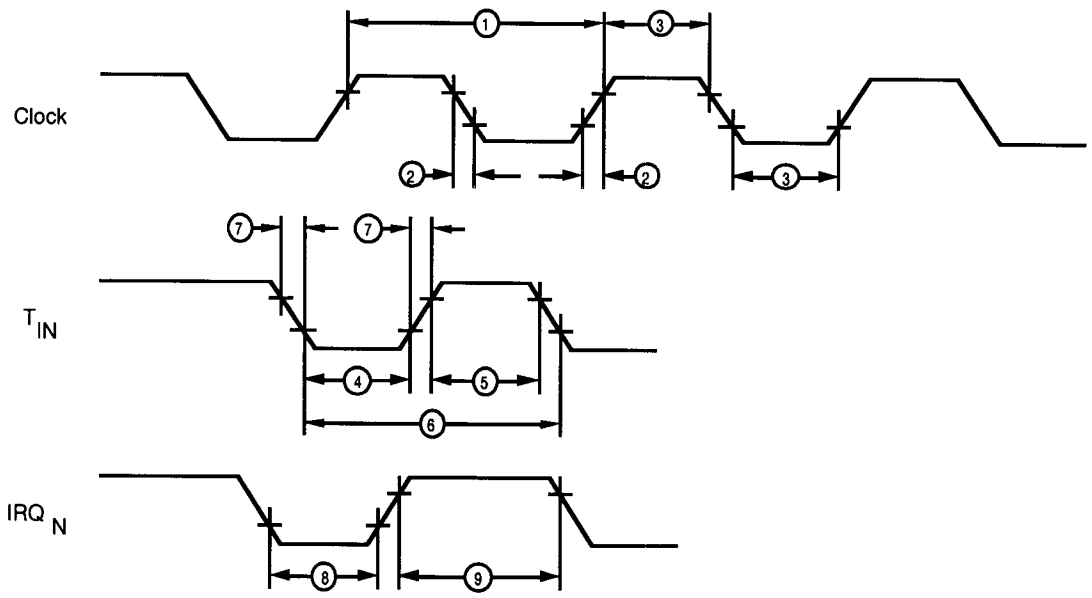


Figure 5. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS (Continued)

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A= 0°C to +70°C				T_A= –40°C to +105°C					
				8 MHz(C05)		12 MHz(C07)		8 MHz(C05)		12 MHz(C07)			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15		25		15	ns	1
			5.5V		25		15		25		15	ns	
3	TwC	Input Clock Width	3.0V	62		41			62		41		1
			5.5V	62		41			62		41	ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time	3.0V		25		25		25		25	ms	1
			5.5V		12		12		10		10	ms	1
11	Tpor		3.0V	24		24		24		24		ms	1
			5.5V	12		12		12		12		ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode

				T_A= 0°C to +70°C				T_A= –40°C to +105°C					
				1 MHz		4 MHz		4 MHz		1 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	3.0V	1000	DC	250	DC	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	3.0V		25		25		25		25	ns	1
			5.5V		25		25		25		25	ns	1
3	TwC	Input Clock Width	3.0V	500		125		500		125		ns	1
			5.5V	500		125		500		125		ns	1
4.	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			1
			5.5V	4TpC		4TpC		4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
9	TwIH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time	3.0V		25		25		25		25	ms	1
			5.5V		12		12		10		10	ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).

LOW NOISE VERSION

Low EMI Emission

The Z8 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

EMI Characteristics

The Z8 operating in the Low EMI mode generates EMI as measured in the following chart:

The measurements, shown in Figure 6, were made while operating the Z8 in three states: (1) idle condition, (2) static output; (3) switched output.

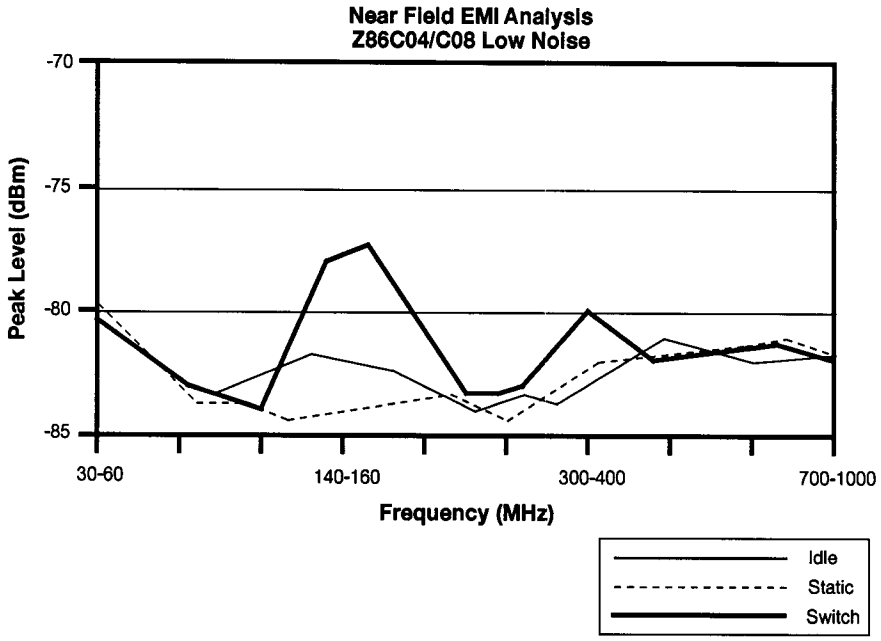


Figure 6. Typical Low Noise Measurements

PIN DESCRIPTION

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a RC, parallel-resonant crystal, LC, or an external single-phase clock to the on-chip clock oscillator and buffer.

Auto Latch. The auto latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. After Power-On Reset, this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. To change the auto latch state, the auto latches must be over driven with current greater than I_{ALH} (high to low) or I_{ALL} (low to high).

Port 0 (P02-P00). Port 0 is a 3-bit I/O, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be configured under software control to be all inputs or all outputs (Figure 7).

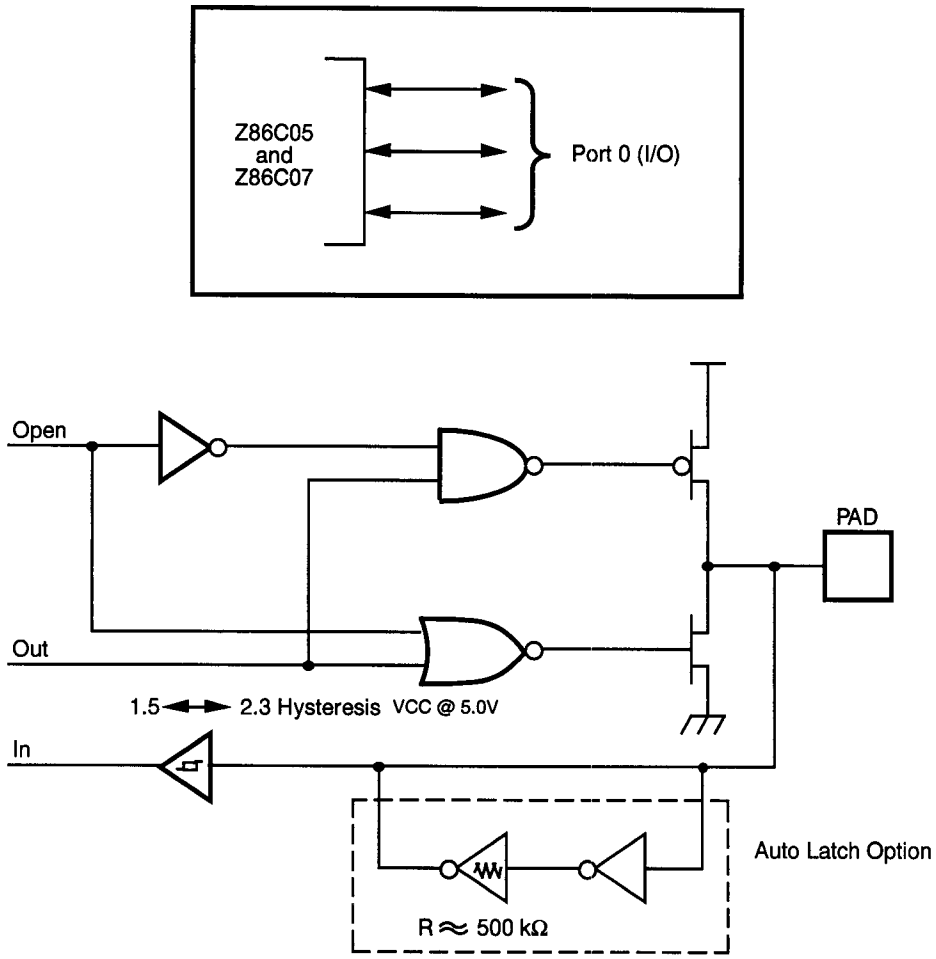


Figure 7. Port 0 Configuration

PIN DESCRIPTION (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit-programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 8).

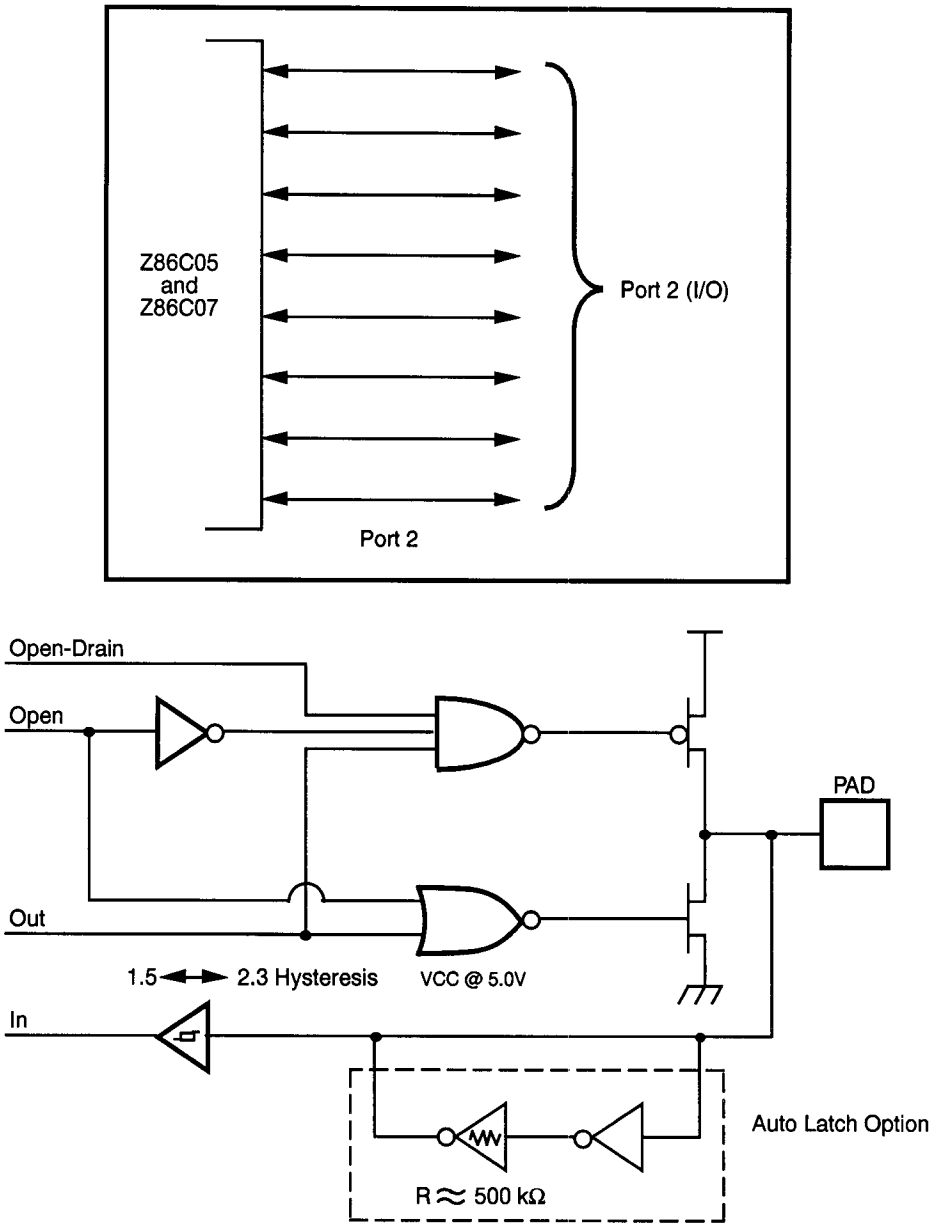


Figure 8. Port 2 Configuration

Port 3 (P33-P31). Port 3 is a 3-bit, Schmitt-triggered CMOS-compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 9).

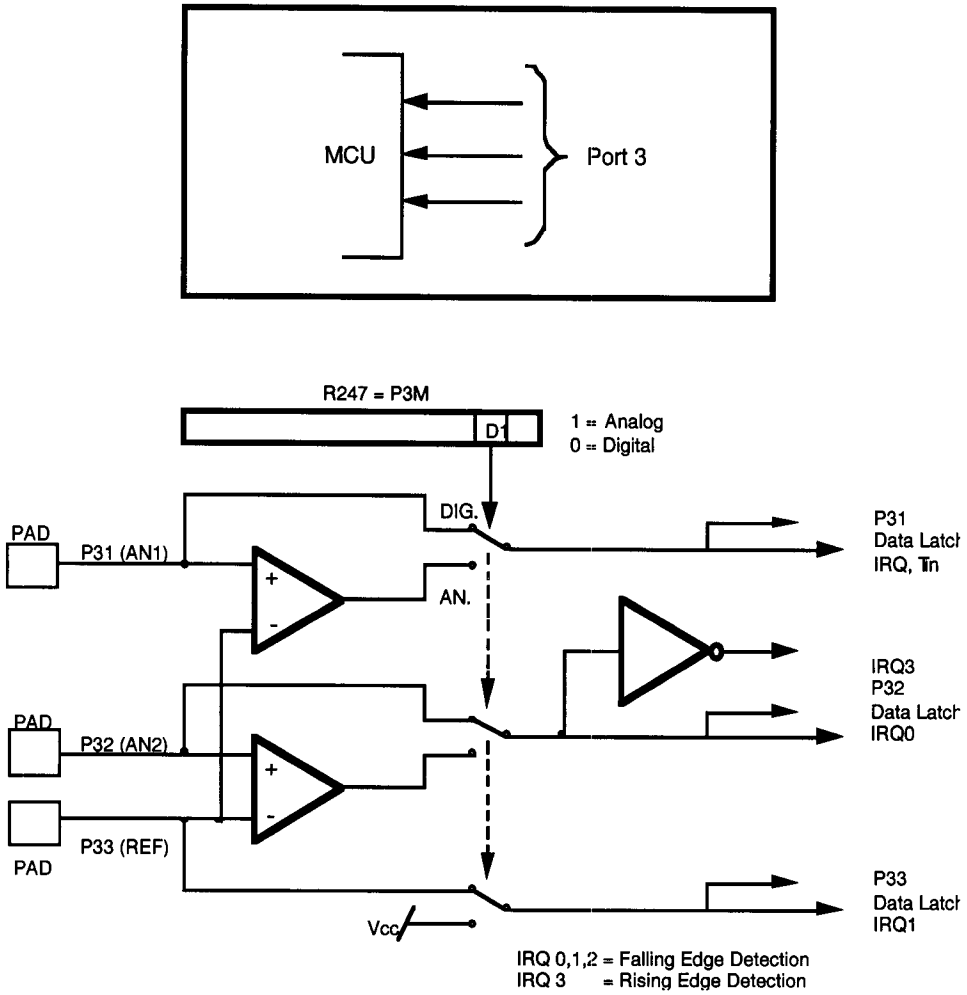


Figure 9. Port 3 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Program Memory. The Z86C05/C07 can address up to 1K/2K bytes of internal program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1023/2047 are on-chip mask-programmed ROM.

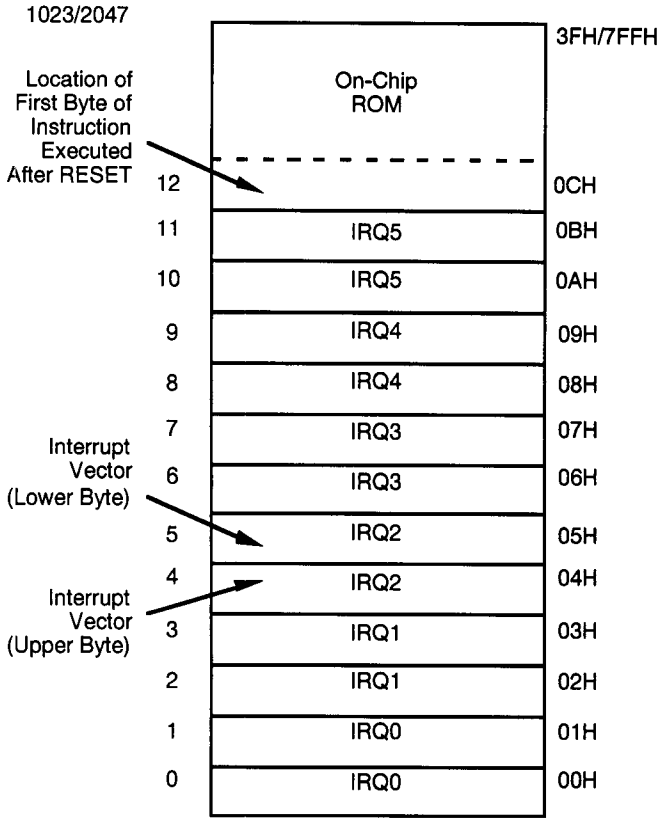


Figure 11. Program Memory Map

Register File. The Register File consists of three I/O port registers, 125 general-purpose registers, and 14 control and status registers (R0, R2-R3, R4-R127, and R241-R255, respectively; see Figure 12). Note that R254 is available for general purpose use. The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group. Upon power-up, the general purpose registers are undefined.

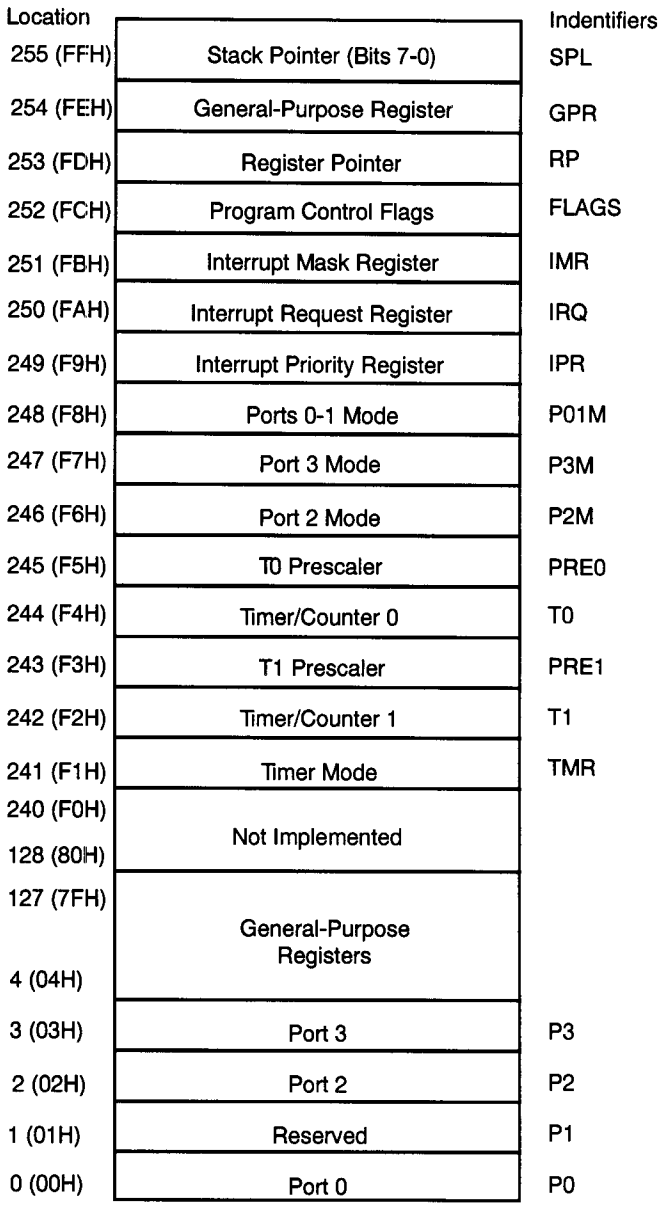


Figure 12. Register File

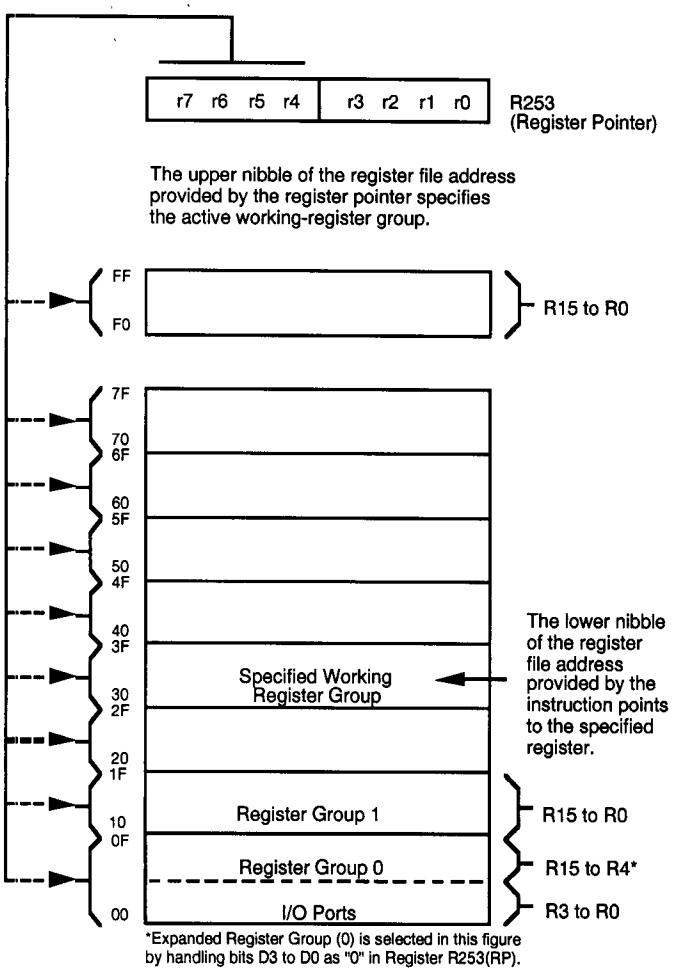


Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Register (GPR). The general-purpose register upon device power-up is undefined. The general-purpose register upon a Stop-Mode Recovery and reset stays in its last state. It may not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V.

Note: Register R254 has been designated as a general-purpose register.

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done within the maximum T_{WDT} period; otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} plus 18 XTAL clock cycles. The WDT does not work (run) in STOP Mode. The WDT is disabled during and after a Reset, until the WDT is enabled again.

Opcode WDH (4FH). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it facilitates running the WDT function during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT Mask Option. Only when the Permanent WDT Mask Option is selected, then the WDT is hardwired to be enabled after reset. The WDT will operate in Run Mode, HALT Mode, and STOP Mode. The Opcode 5FH is used to refresh or clear the WDT counter. The WDH instruction (4FH) has no effect.

Low Voltage Protection (V_{LV}). Maximum (V_{LV}) Conditions:

Case 1: T_A= –40°C, +85°C, Internal Clock Frequency equal or less than 6 MHz

Case 2: T_A= –40°C, +105°C, Internal Clock Frequency equal or less than 4 MHz

Note: The internal clock frequency is one-half the external clock frequency in standard mode.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Cases 1 and 2. The actual low voltage trip point is a function of temperature and process parameters (Figure 17).

2 MHz (Typical

Temp	–40°	0°C	+25°C	+70°C	+105°C
V_{LV}	2.55	2.4		1.7	1.6
	3.0	2.75	2.6	2.3	2.1

ROM Protect. ROM Protect fully protects the Z86C04/C08 ROM code from being read internally. **When ROM Protect is selected. ROM look-up tables can be used in this mode.**

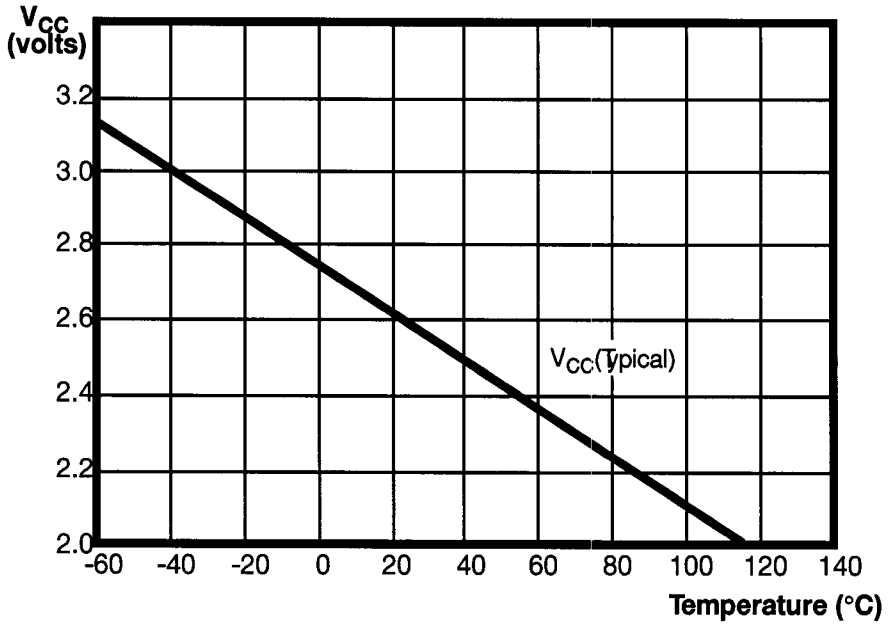


Figure 17. Typical Z86C04/C08 V_{LV} vs. Temperature

Z8® CONTROL REGISTER DIAGRAMS

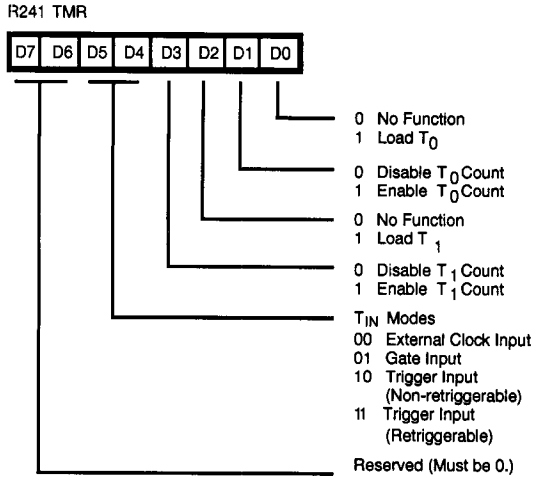


Figure 18. Timer Mode Register ($F1_H$: Read/Write)

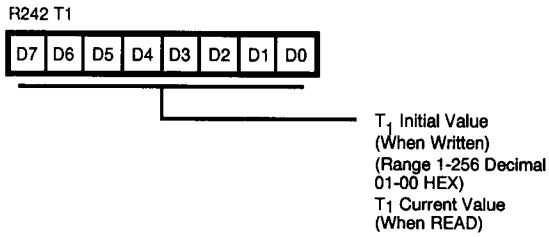


Figure 19. Counter Time 1 Register ($F2_H$: Read/Write)

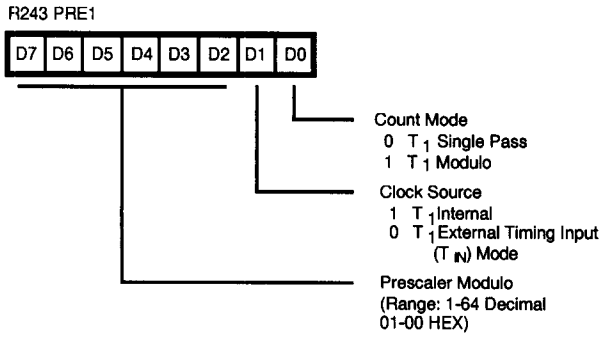


Figure 20. Prescaler 1 Register ($F3_H$: Write Only)

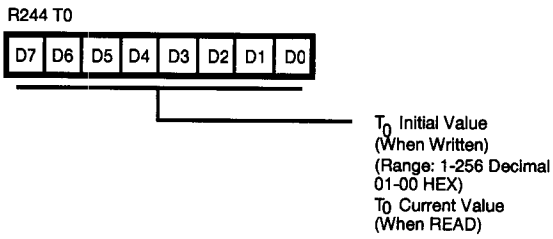


Figure 21. Counter/Timer 0 Register ($F4_H$: Read/Write)

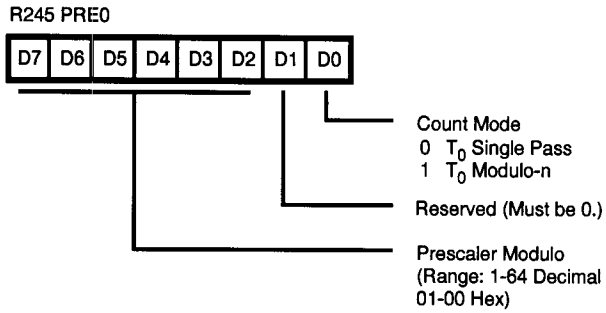


Figure 22. Prescaler 0 Register ($F5_H$: Write Only)

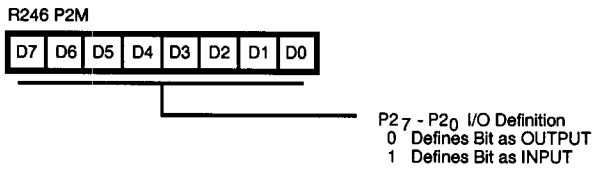


Figure 23. Port 2 Mode Register ($F6_H$: Write Only)

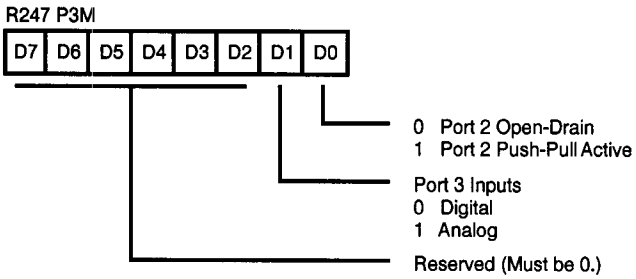


Figure 24. Port 3 Mode Register ($F7_H$: Write Only)

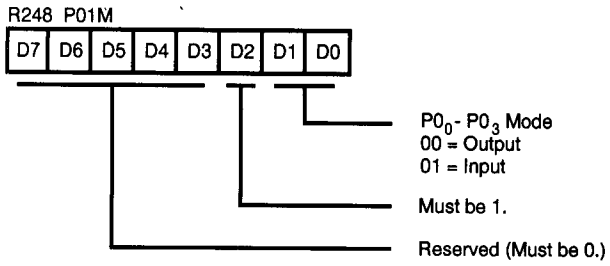


Figure 25. Port 0 and 1 Mode Register
Figure 26. ($F8_H$: Write Only)

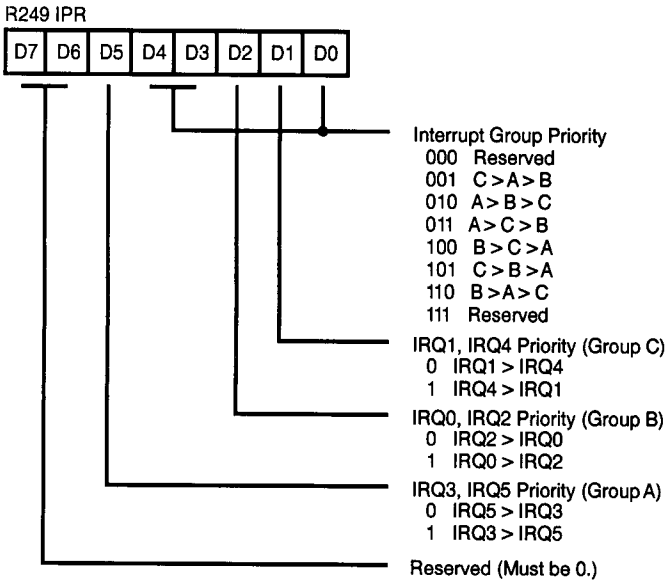


Figure 27. Interrupt Priority Register
Figure 28. ($F9_H$: Write Only)

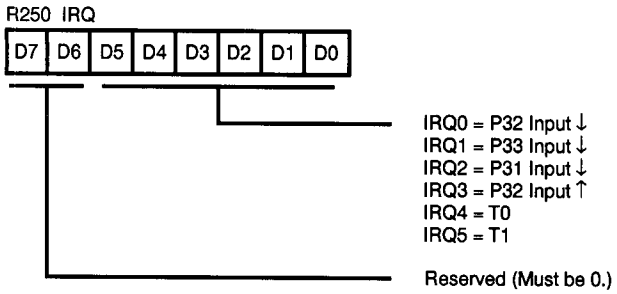


Figure 29. Interrupt Request Register
Figure 30. (FA_H: Read/Write)

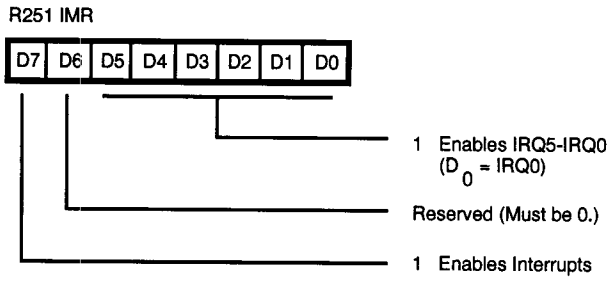


Figure 31. Interrupt Mask Register
Figure 32. (FB_H: Read/Write)

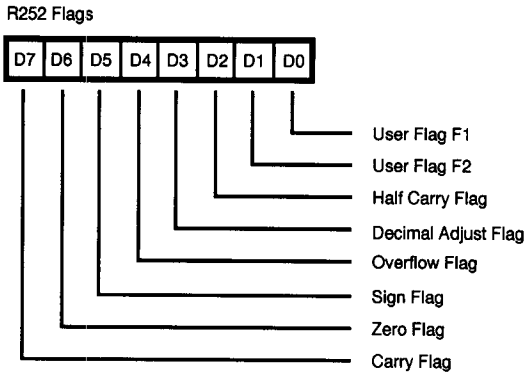


Figure 33. Flag Register
Figure 34. (FC_H: Read/Write)

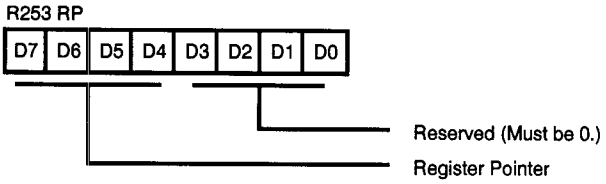


Figure 35. Register Pointer
Figure 36. (FD_H: Read/Write)

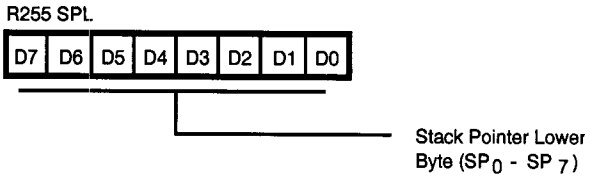


Figure 37. Stack Pointer
Figure 38. (FF_H: Read/Write)

DEVICE CHARACTERISTICS

Standard Mode

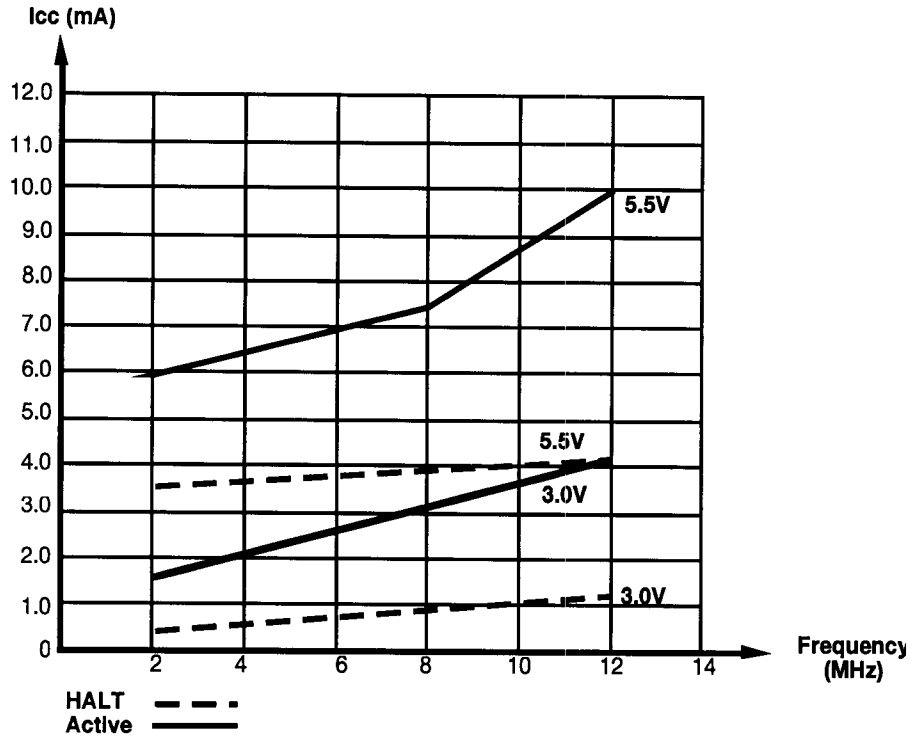


Figure 39. Typical I_{CC} vs. Frequency

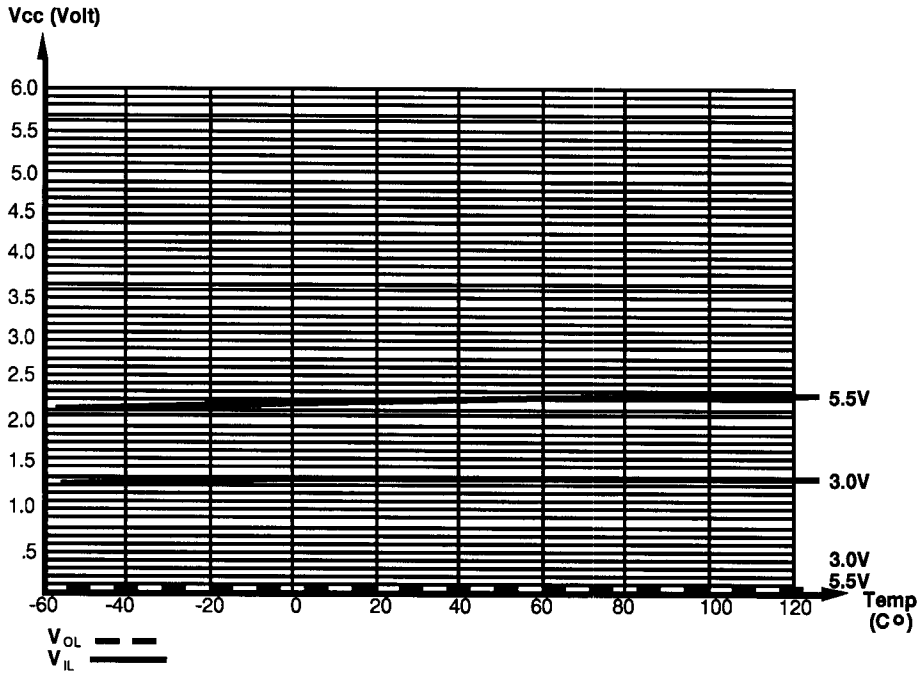


Figure 40. V_{IL}, V_{OL} vs. Temperature

DEVICE CHARACTERISTICS (Continued)

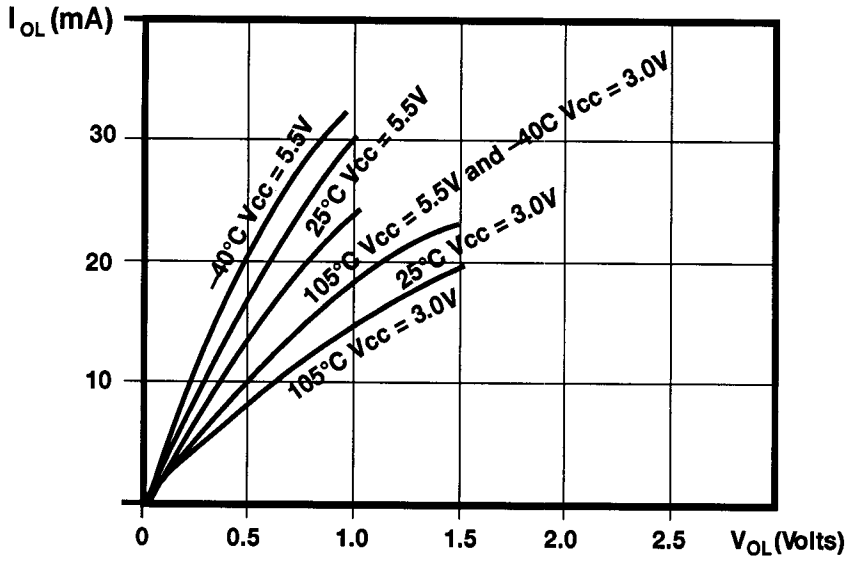


Figure 43. Typical I_{OL} vs. V_{OL}

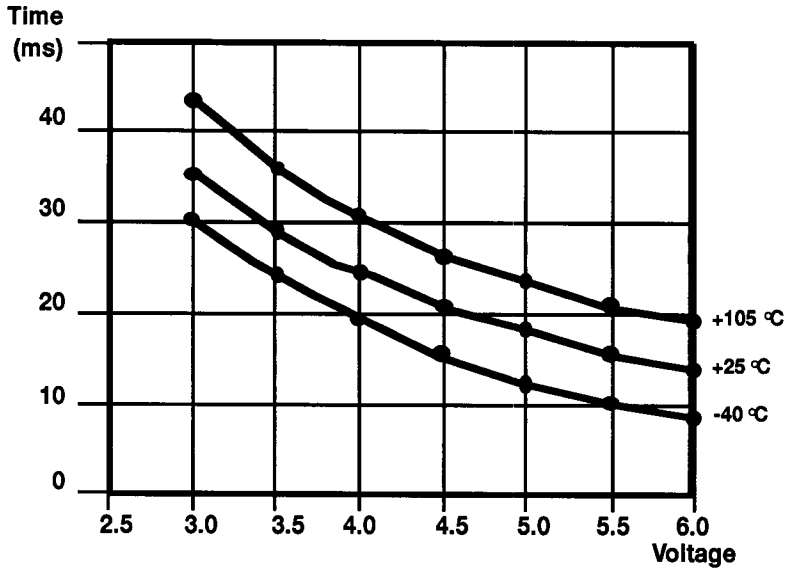
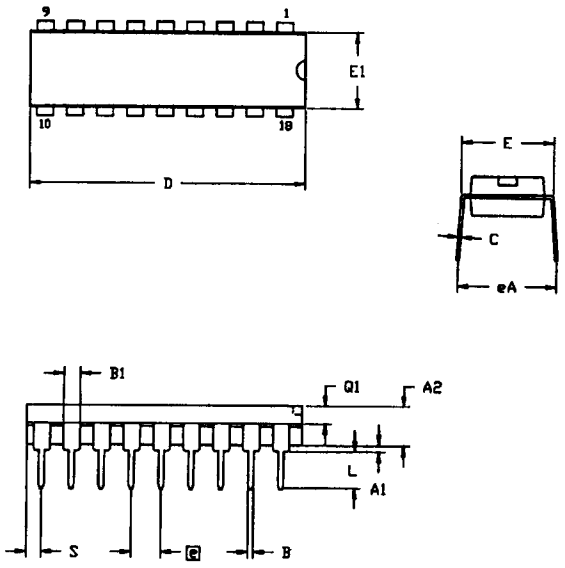


Figure 44. Typical WDT Time Out Period vs. V_{CC} Over Temperature

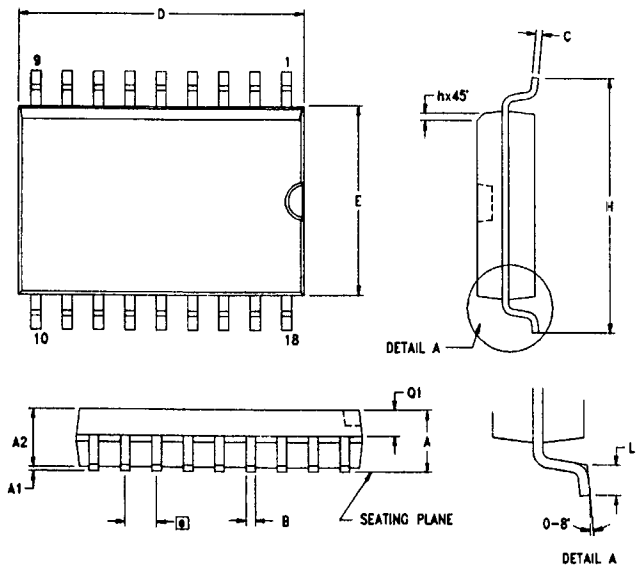
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 45. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 46. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C05 (8 MHz) Standard Temperature		Z86C07 (12 MHz) Standard Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0408PSC	Z86C0408SSC	Z86C0812PSC	Z86C0812SSC
Extended Temperature		**Extended Temperature**	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86C0408PEC	Z86C0408SEC	Z86C0812PEC	Z86C0812SEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = DIP

Longer Lead Time
S = SOIC

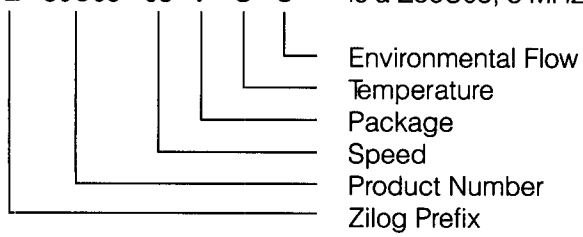
Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:
Z 86C05 08 P S C is a Z86C05, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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