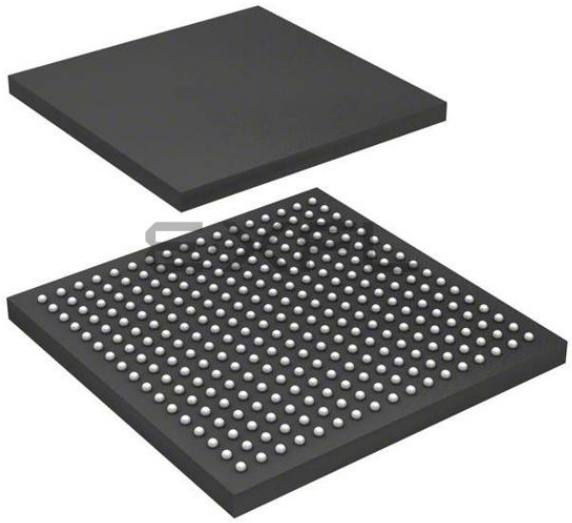

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	454MHz
Co-Processors/DSP	Data; DCP
RAM Controllers	LVDDR, LVDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Hardware ID
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx280dvm4br

such as memories and SD cards, as well as provide battery charging capability for Li-Ion batteries.

The i.MX28 processor includes an additional 128-Kbyte on-chip SRAM to make the device ideal for eliminating external RAM in applications with small footprint RTOS.

The i.MX28 supports connections to various types of external memories, such as mobile DDR, DDR2 and LV-DDR2, SLC and MLC NAND Flash.

The i.MX28 can be connected to a variety of external devices such as high-speed USB2.0 OTG, CAN, 10/100 Ethernet, and SD/SDIO/MMC.

1.1 Device Features

The following lists the features of the i.MX28:

- ARM926EJ-S CPU running at 454 MHz:
  - 16-Kbyte instruction cache and 32-Kbyte data cache
  - ARM embedded trace macrocell (CoreSight™ ETM9™)
  - Parallel JTAG interface
- 128 KBytes of integrated low-power on-chip SRAM
- 128 KBytes of integrated mask-programmable on-chip ROM
- 1280 bits of on-chip one-time-programmable (OCOTP) ROM
- 16-bit mobile DDR (mDDR) (1.8 V), DDR2 (1.8 V) and LV-DDR2 (1.5 V), up to 205 MHz DDR clock frequency with voltage overdrive
- Support for up to eight NAND Flash memory devices with up to 20-bit BCH ECC
- Four synchronous serial ports (SSP) for SDIO/MMC/MS/SPI: SSP0, SSP1, SSP2, and SSP3. SSP0 and SSP1 can support three modes,1-bit, 4-bit, and 8-bit, whereas SSP2 and SSP3 can support only 1-bit and 4-bit modes.
- 10/100-Mbps Ethernet MAC compatible with IEEE Std 802.3™:
  - Single 10/100 Ethernet with GMII/RMII or Dual 10/100 Ethernet with RMII interface
  - Supporting IEEE Std 1588™-compatible hardware timestamp
  - Supporting 50-MHz/25-MHz clock output for external Ethernet PHY
- Two 2.0B protocol-compatible Controller Area Network (CAN) interfaces
- One USB2.0 OTG device/host controller and PHY
- One USB2.0 host controller and PHY
- LCD controller, up to 24-bit RGB (DOTCK) modes and 24-bit system-mode
- Pixel-processing pipeline (PXP) supports full path from color-space conversion, scaling, alpha-blending to rotation without intermediate memory access.
- SPDIF transmitter
- Dual serial audio interface (SAIF) to support full-duplex transmit and receive operations; each SAIF supports three stereo pairs
- Five application Universal Asynchronous Receiver-Transmitters (UARTs), up to 3.25 Mbps with hardware flow control

- One debug UART operating at up to 115 Kb/s using programmed I/O
- Two I^2C master/slave interfaces, up to 400 kbps
- Four 32-bit timers and a rotary decoder
- Eight Pulse Width Modulators (PWMs)
- Real-time clock (RTC)
- GPIO with interrupt capability
- Power Management Unit (PMU) supports a triple output DC-DC switching converter, multiple linear regulators, battery charger, and detector.
- 16-channel Low-Resolution A/D Converter (LRADC). There are 16 physical channels but they can only be mapped to 8 virtual channels at a time.
- Single channel High Speed A/D Converter (HSADC), up to 2 Msps data rate
- 4/5-wire touchscreen controller
- Up to 8X8 keypad matrix with button-detect circuit
- Security features:
  - Read-only unique ID for Digital Rights Management (DRM) algorithms
  - Secure boot using 128-bit AES hardware decryption
  - SHA-1 and SHA256 hashing hardware
  - High assurance boot (HAB4)
- Offered in 289-pin Ball Grid Array (BGA)

1.2 Ordering Information and Functional Part Differences

Table 1 provides the ordering information for the i.MX28.

Table 1. Ordering Information

Part Number	Projected Temperature Range (°C)	Package
MCIMX280DVM4B	–20 to +70	14 x 14 mm, 0.8mm pitch, MAPBGA-289
MCIMX280CVM4B	–40 to +85	14 x 14 mm, 0.8mm pitch, MAPBGA-289
MCIMX283DVM4B	–20 to +70	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX283CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX286DVM4B	–20 to +70	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX286CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289
MCIMX287CVM4B	–40 to +85	14 x 14 mm, 0.8 mm pitch, MAPBGA-289

3 Maximum Ambient Operating Temperature may be limited due to on-chip power dissipation. $T_{A\ (MAX)} \leq T_J - (\Theta_{JA} \times P_D)$ where:
T_J = Maximum Junction Temperature
Θ_{JA} = Package Thermal Resistance. See Section 3.2, “Thermal Characteristics.”
P_D = Total On-chip Power Dissipation =PVDD4P2 + PBatteryCharger + PDCDC + PLinearRegulators + PInternal. Depending on the application, some of these power dissipation terms may not apply.
PVDD4P2 = VDD4P2 On-Chip Power Dissipation = (VDD5V - VDD4P2) x IDD4P2
PBatteryCharger = Battery Charger On-Chip Power Dissipation = (VDD5V - BATT) x ICHARGE
PDCDC = DC-DC Converter On-Chip Power Dissipation = (BATT x DCDC Input Current) x (1 - efficiency)
PLinearRegulators = Linear Regulator On-Chip Power Dissipation = (VDD5V - VDDIO) x (IDDIO + IDDA + IDDD + IDD1P5) + (VDDIO - VDDA) x (IDDA + IDDD) + (VDDA - VDDD) x IDDD + (VDDA - VDD1P5) x IDD1P5
PInternal = Internal Digital On-Chip Power Dissipation = ~VDDD x IDDD

Table 10 provides the recommended analog operating conditions.

Table 10. Recommended Analog Operating Conditions

Parameter	Min	Typ	Max	Unit
Low Resolution ADC Input Impedance (CH0 - CH5)	>1	—	—	MΩ

Table 11 shows the PSWITCH input characteristics. See the reference schematics for the recommended PSWITCH button circuitry.

Table 11. PSWITCH Input Characteristics

Parameter	HW_PWR_STS_PSWITCH	Min	Max	Unit
PSWITCH LOW LEVEL	0x00	0.00	0.30	V
PSWITCH MID LEVEL & STARTUP[1]	0x01	0.65	1.50	V
PSWITCH HIGH LEVEL[2]	0x11	(1.1 * VDDXTAL) + 0.58	2.45	V

1 A MID LEVEL PSWITCH state can be generated by connecting the VDDXTAL output of the SoC to PSWITCH through a switch.

2 PSWITCH acts like a high impedance input (>300 kΩ) when the voltage applied to it is less than 1.5V. However, above 1.5V it becomes lower impedance. To simplify design, it is recommended that a 10 kΩ resistor to VDDIO be applied to PSWITCH to set the HIGH LEVEL state (the PSWITCH input can tolerate voltages greater than 2.45 V as long as there is a 10 kΩ resistor in series to limit the current).

Table 12 shows a test case example for Run IDD.

Table 12. Run IDD Test Case[1,2]

Power Rail	Conditions	Min	Typ	Max	Unit
VDDD	1.57 V	—	150	188	mA
VDDIO33	3.62 V	—	31	34	mA
VDDA	2.12 V	—	1.11	1.17	mA
VDDIO_EMI	1.92 V	—	1.01	1.08	mA
VDDIO18	1.92 V	—	0.61	2.97	µA

1 CPUCLK = 300 MHz, AHBCLK = 150 MHz

2 Continuous read / write to the cache memory

Table 13 illustrates the power supply characteristics.

Table 13. Power Supply Characteristics

Parameter	Min	Typ	Max	Unit
Linear Regulators				
Output Voltage Accuracy (V_{DDIO}, V_{DDA}, V_{DDM}, V_{DDD})[1]	–3	—	+3	%
V_{DDIO} Maximum Output Current (V_{DDIO} = 3.30 V, V_{DD5V} = 4.75 V)[2, 3]	270	—	—	mA
V_{DDM} Maximum Output Current (V_{DDM} = 1.5 V)[2]	160	—	—	mA
V_{DDA} Maximum Output Current (V_{DDA} = 1.8 V)[2, 3]	225	—	—	mA
V_{DDD} Maximum Output Current (V_{DDD} = 1.2 V)[2, 3]	200	—	—	mA
DCDC Converters				
Output Voltage Accuracy (DCDC_VDDIO, DCDC_VDDA, DCDC_VDDD)[1]	–3	—	+3	%
DCDC_VDDD Maximum Output Current (V_{DDD} = 1.55 V)[4, 5]	250	—	—	mA
DCDC_VDDA Maximum Output Current (V_{DDA} = 1.8 V)[4, 5]	200	—	—	mA
DCDC_VDDIO Maximum Output Current (V_{DDIO} = 3.15 V, 3.3 V < BATT < 4.242 V)[4, 5, 6]	250	—	—	mA
VDD4P2 Regulated Output				
VDD4P2 Output Voltage Accuracy (TARGET=4.2V)[1]	–3	—	+3	%
VDD4P2 Output Current Limit Accuracy (VDD5V = 4.75 V, ILIMIT=480 mA)[7]	480	500	520	mA
VDD4P2 Output Current Limit Accuracy (VDD5V=4.75 V, ILIMIT=100 mA)[7]	100	120	140	mA
Battery Charger				
Final Charge Voltage Accuracy (TARGET=4.2 V)	-2	—	+1	%

1 No load.

2 Maximum output current measured when output voltage droops 100 mV from the programmed target voltage with no load present.

3 Because the internal linear regulators are cascaded, it is not possible to simultaneously operate the V_{DDIO}, V_{DDA}, V_{DDM}, and V_{DDD} linear regulators at the maximum specified load current. For example, the V_{DDIO} linear regulator provides current to both the V_{DDIO} 3.3 V supply rail as well as the V_{DDM} and V_{DDA} linear regulator inputs. Likewise, the V_{DDA} linear regulator provides current to both the 1.8 V supply rail as well as the V_{DDD} linear regulator input. The application designer should ensure the following two conditions are met:

(V_{DDIO} Load Current + V_{DDM} Load Current + V_{DDA} Load Current) < V_{DDIO} Maximum Output Current
(V_{DDA} Load Current + V_{DDD} Load Current) < V_{DDA} Maximum Output Current

4 DCDC Double FETs Enabled, Inductor Value = 15 µH.

5 The DCDC Converter is a triple output buck converter. The maximum output current capability of each output of the converter is dependent on the loads on the other two outputs. For a given output, it may be possible to achieve a maximum output current higher than that specified by ensuring the load on the other outputs is well below the maximum.

6 Assumes simultaneous load of IDDD = 250 mA@ 1.55 V and IDDA = 200 mA@1.8 V.

7 Untuned.

Table 20. Power Mode Settings (continued)

Core/Clock/Module	Offstate	Standby	Run
OSC32K	On	On	On
DCDC	Off	On	On
RTC	On	On	On
Other Modules	Off	On/Off	On/Off

3.1.6 Supply Power-Up/Power-Down Requirements

There is no special power-up sequence. After applying 5 V or battery in any order, the rest of the power supplies are internally generated and automatically come up in a safe way.

There is no special power-down sequence. 5 V or the battery can be removed at any time.

3.1.7 Reset Timing

Because the i.MX28 is a PMU and an SoC, power-on reset is generated internally and there is no timing requirement on external pins.

The i.MX28 can be reset by asserting the external pin RESETN for at least 100 mS and later deasserting RESETN.

If the reset occurs while the device is only powered by the battery, then the reset kills all of the power supplies and the system reboots on the assertion of PSWITCH. If auto-restart is set up ahead of time, the system reboots immediately.

If the chip is powered by 5 V, then the reset serves to reset the digital sections of the chip. If the DCDC is operating at the time of the reset, then power switches back to the default linear regulators powered by 5 V.

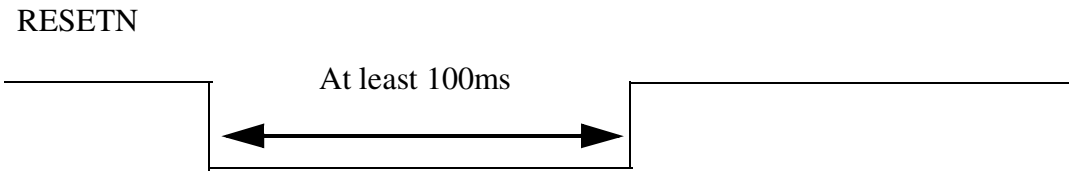

Figure 2. RESETN Timing

3.2 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 21. These values are measured under the following conditions:

- Two layer Substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.160 mm

- Core via I.D: 0.068 mm, Core via plating 0.016 mm
- Flag: trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold Compound: generic mold compound, k = 0.9 W/m K

Table 21. Thermal Resistance Data

Rating			Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	62	°C/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	36	°C/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	53	°C/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	33	°C/W
Junction to boards[2]		$R_{\theta JB}$	24	°C/W
Junction to case (top)[3]		$R_{\theta JCtop}$	15	°C/W
Junction to package top[4]	Natural Convection	Ψ_{JT}	3	°C/W

1 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-2 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (LPDDR1), standard 1.8 V DDR2, and low-voltage 1.5 V DDR2 (LVDDR2)
- General purpose I/O (GPIO)

3.3.1 DDR I/O DC Parameters

Table 22 shows the EMI digital pin DC characteristics.

NOTE

The current values and the I-V curves of the I/O DC characteristics are estimated based on an overly conservative device model. They are updated upon the measurement results of the first silicon.

Table 22. EMI Digital Pin DC Characteristics

Parameter	Symbol	Min.	Max.	Unit
Input voltage high (dc)	VIH	VREF + 0.125	VDDIO_EMI + 0.3	V
Input voltage low (dc)	VIL	0.3	VREF – 0.125	V
Output voltage high (dc)	VOH	0.8 * VDDIO_EMI	—	V
Output voltage low (dc)	VOL	-	0.2 * VDDIO_EMI	V
Output source current (dc) LVDDR2 Mode	IOH[1]—Low	-6.2	—	mA
	IOH—Medium	-7.2	—	mA
	IOH—High	-9.7	—	mA
Output sink current (dc) LVDDR2 Mode	IOL[2]—Low	5.7	—	mA
	IOL—Medium	7.3	—	mA
	IOL—High	10.0	—	mA
Output source current (dc) mDDR, DDR2 Mode	IOH—Low	-5.7	—	mA
	IOH—High	-7.5	—	mA
Output sink current (dc) mDDR, DDR2 Mode	IOL—Low	5.4	—	mA
	IOL—High	8.8	—	mA

1 IOH is the output current at which the VOH specification is met.

2 IOL is the output current at which the VOL specification is met.

Table 23 shows the ON impedance of EMI drivers for different drive strengths.

Table 23. ON Impedance of EMI Drivers for Different Drive Strengths[1]

Mode	Drive	Min. (Ω)	Typ. (Ω)	Max. (Ω)
1.5 LVDDR2	Low	26	38	58
	Medium	17	25	36
	High	15	20	27
1.8 DDR2/mDDR	Low	36	53	78
	Medium	17	27	42
	High	16	19	28

1 ON impedance of the EMI drivers are guaranteed by design and are not tested during production.

Table 27. Base GPIO (continued)

Parameters	Symbol	Test Voltage	Test Capacitance	Min Rise/Fall		MaxRise/Fall		Unit	Notes
Output pad transition times (medium drive)	tpr	1.7~1.9V	10 pF	1.02	1.08	2.34	2.38	ns	—
		1.7~1.9V	20 pF	1.51	1.5	3.34	3.28		—
		1.7~1.9V	50 pF	2.91	2.62	6.24	5.67		—
		3.0~3.6V	10 pF	1.26	1.29	2.9	2.6		—
		3.0~3.6V	20 pF	1.8	1.88	4	3.67		—
		3.0~3.6V	50 pF	3.3	3.46	6.91	6.64		—
Output pad transition times (low drive)	tpr	1.7~1.9V	10 pF	1.62	1.68	3.65	3.68	ns	—
		1.7~1.9V	20 pF	2.55	2.45	5.59	5.37		—
		1.7~1.9V	50 pF	5.42	4.62	11.46	10.01		—
		3.0~3.6V	10 pF	1.95	2.12	4.43	4.25		—
		3.0~3.6V	20 pF	2.96	3.21	6.36	6.25		—
		3.0~3.6V	50 pF	5.89	6.39	12.02	12.18		—
Output pad slew rate (maximum drive)	tps	1.7~1.9V	10 pF	1.39	1.25	0.53	0.52	V/ns	—
		1.7~1.9V	20 pF	0.97	0.93	0.38	0.38		—
		1.7~1.9V	50 pF	0.54	0.56	0.22	0.23		—
		3.0~3.6V	10 pF	2.08	2.00	0.73	0.83		—
		3.0~3.6V	20 pF	1.52	1.44	0.55	0.60		—
		3.0~3.6V	50 pF	0.88	0.83	0.34	0.35		—
Output pad slew rate (medium drive)	tps	1.7~1.9V	10 pF	1.12	1.06	0.44	0.43	V/ns	—
		1.7~1.9V	20 pF	0.75	0.76	0.31	0.31		—
		1.7~1.9V	50 pF	0.39	0.44	0.16	0.18		—
		3.0~3.6V	10 pF	1.71	1.67	0.62	0.69		—
		3.0~3.6V	20 pF	1.20	1.15	0.45	0.49		—
		3.0~3.6V	50 pF	0.65	0.62	0.26	0.27		—
Output pad slew rate (low drive)	tps	1.7~1.9V	10 pF	1.17	1.13	0.47	0.46	V/ns	—
		1.7~1.9V	20 pF	0.75	0.78	0.30	0.32		—
		1.7~1.9V	50 pF	0.35	0.41	0.15	0.17		—
		3.0~3.6V	10 pF	1.11	1.02	0.41	0.42		—
		3.0~3.6V	20 pF	0.73	0.67	0.28	0.29		—
		3.0~3.6V	50 pF	0.37	0.34	0.15	0.15		—
Input pad average hysteresis	tih	1.7 V–1.9 V	—	100		75		mV	—
		3.0 V–3.6 V	—	100		50			—

3.5.4.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

3.5.4.1.1 MII Receive Signal Timing (ENET0_RXD[3:0], ENET0_RX_DV, ENET0_RX_ER, and ENET0_RX_CLK)

The receiver functions correctly up to an ENET0_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET0_RX_CLK frequency.

Figure 9 shows MII receive signal timings. Table 38 describes the timing parameters (M1–M4) shown in the figure.

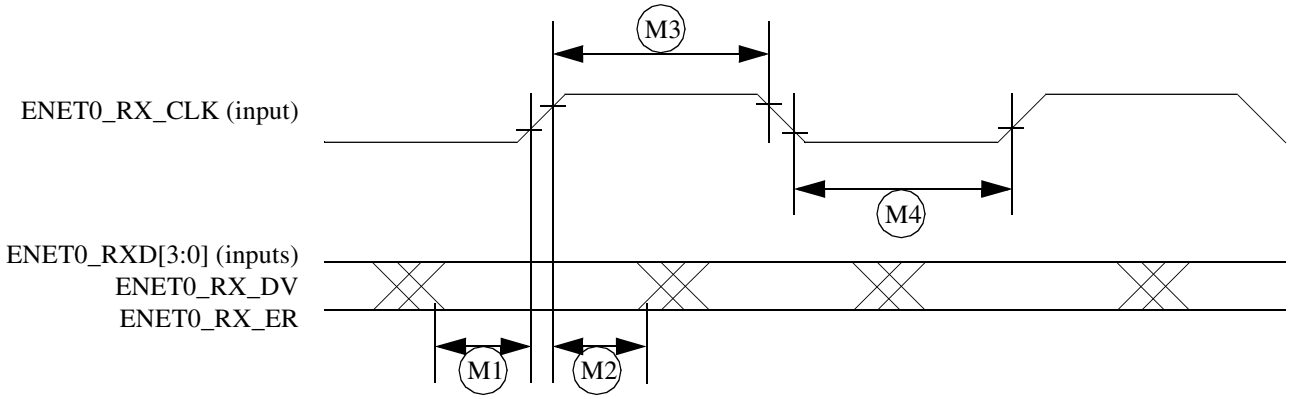

Figure 9. MII Receive Signal Timing Diagram

Table 38. MII Receive Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET0_RXD[3:0], ENET0_RX_DV, ENET0_RX_ER to ENET0_RX_CLK setup	5	—	ns
M2	ENET0_RX_CLK to ENET0_RXD[3:0], ENET0_RX_DV, ENET0_RX_ER hold	5	—	ns
M3	ENET0_RX_CLK pulse width high	35%	65%	ENET0_RX_CLK period
M4	ENET0_RX_CLK pulse width low	35%	65%	ENET0_RX_CLK period

[1] ENET0_RX_DV, ENET0_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

3.5.4.1.2 MII Transmit Signal Timing (ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER, and ENET0_TX_CLK)

The transmitter functions correctly up to an ENET0_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET0_TX_CLK frequency.

3.5.6 FlexCAN AC Timing

Table 45 and Table 46 show voltage requirements for the FlexCAN transceiver Tx and Rx pins.

Table 45. Tx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-level output voltage	V_{OH}	2	—	Vcc[1] + 0.3	V
Low-level output voltage	V_{OL}	—	0.8	—	V

1 Vcc = +3.3 V ± 5%

Table 46. Rx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	0.8 × Vcc[1]	—	Vcc[1]	V
Low-level input voltage	V_{IL}	—	0.4	—	V

1 Vcc = +3.3 V ± 5%

Figure 16 through Figure 19 show the FlexCAN timing, including timing of the standby and shutdown signals.

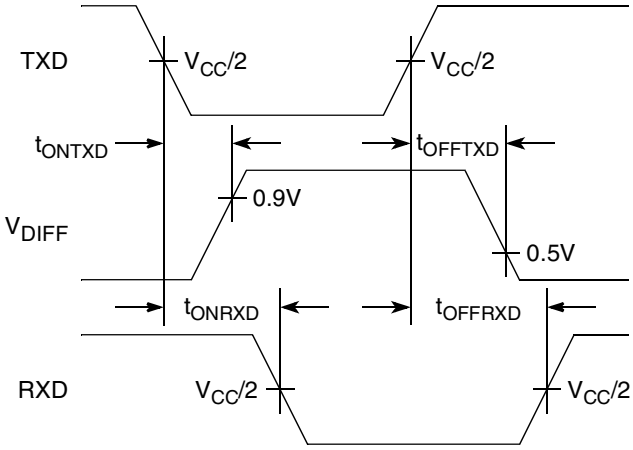

Figure 16. FlexCAN Timing Diagram

Table 47. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100MHz T = 10ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1)*T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1)*T	—	20	—	ns
NF3	$\overline{CE}$n setup time	tCS	(AS+1)*T	—	10	—	ns
NF4	$\overline{CE}$ hold time	tCH	(DH+1)*T	—	20	—	ns
NF5	$\overline{WE}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 The Flash clock maximum frequency is 100 MHz.

2)GPMI's output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP,HW_GPMI_TIMING0_DATA_SETUP,HW_GPMI_TIMING0_DATA_HOLD, this AC timing depends on these registers' setting. In the above table we use AS/DS/DH representing these settings each.

3)AS minimum value could be 0, while DS/DH minimum value is 1.

3.5.10 JTAG Interface Timing

Figure 26 through Figure 29 show respectively the test clock input, boundary scan, test access port, and $\overline{\text{TRST}}$ timings for the SJC. Table 50 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

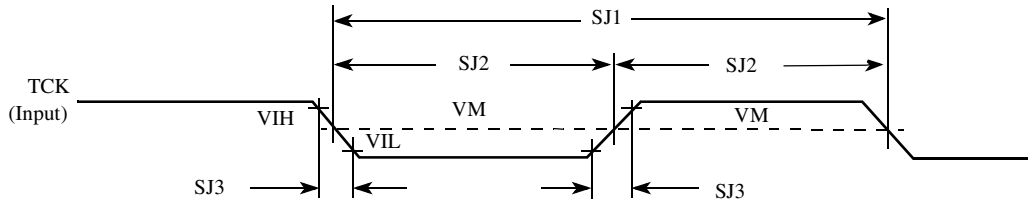

Figure 26. Test Clock Input Timing Diagram

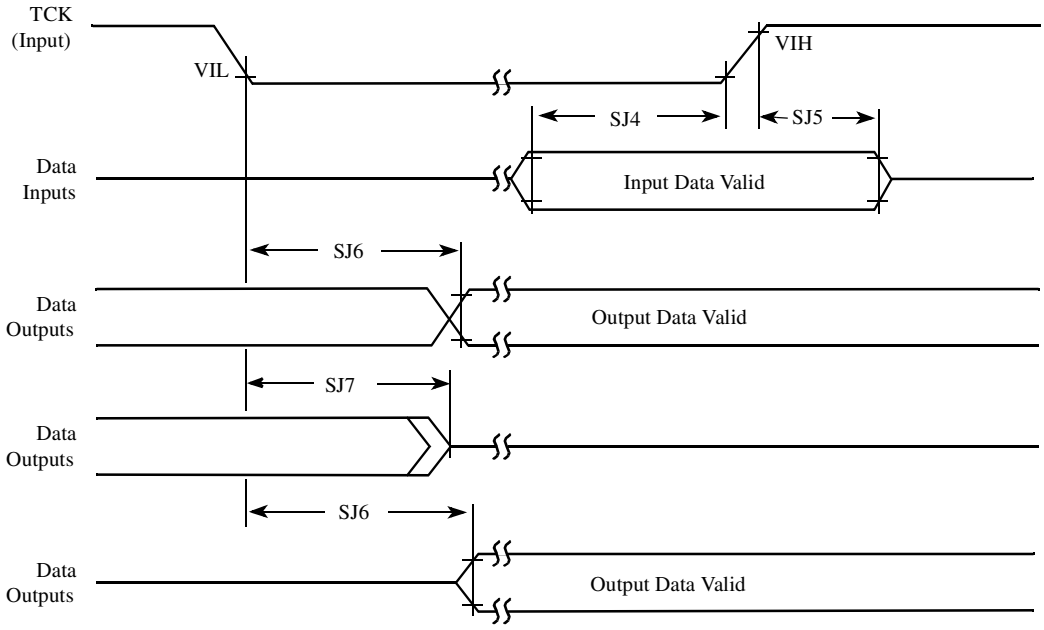

Figure 27. Boundary Scan (JTAG) Timing Diagram

Table 60. MS Parallel Transfer Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
MS5	SCK Fall Time	tCLKf	—	10	ns
MS11	BS Setup Time	tBSsu	8	—	ns
MS12	BS Hold Time	tBSh	1	—	ns
MS13	DATA Setup Time	tDsu	8	—	ns
MS14	DATA Hold Time	tDh	1	—	ns
MS15	DATA Input Delay Time	tDd	—	15	ns

3.5.14.4 SPI AC Timing

Figure 41 depicts the master mode and slave mode timings of the SPI, and Table 61 lists the timing parameters.

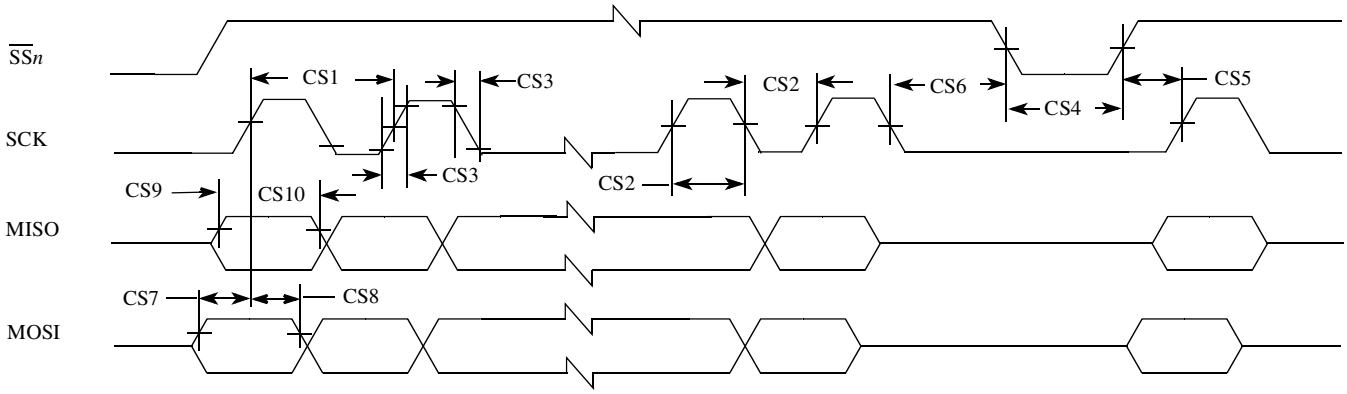

Figure 41. SPI Interface Timing Diagram

Table 61. SPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
CS1	SCK cycle time	t_{clk}	50	—	ns
CS2	SCK high or low time	t_{SW}	25	—	ns
CS3	SCK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{SS}n$ pulse width	t_{CSLH}	25	—	ns
CS5	$\overline{SS}n$ lead time (CS setup time)	t_{SCS}	25	—	ns
CS6	$\overline{SS}n$ lag time (CS hold time)	t_{HCS}	25	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns
CS10	MISO hold time	t_{Hmiso}	5	—	ns

3.5.15 UART (UARTAPP and DebugUART) AC Timing

This section describes the UART module AC timing which is applicable to both UARTAPP and DebugUART.

3.5.15.1 UART Transmit Timing

Figure 39 shows the UART transmit timing, showing only eight data bits and one stop bit. Table 62 describes the timing parameter (UA1) shown in the figure.

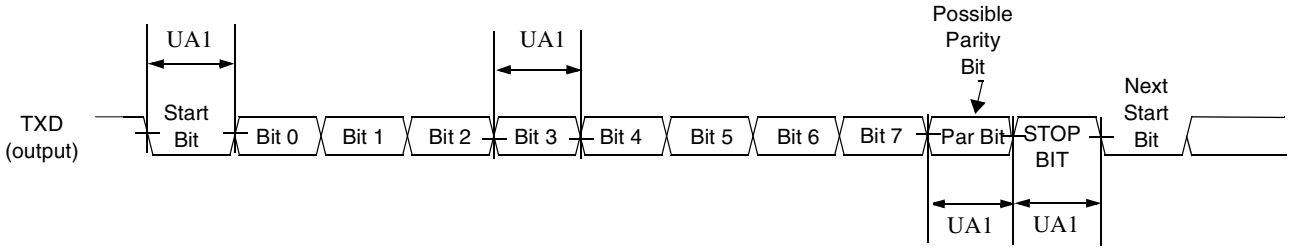

Figure 42. UART Transmit Timing Diagram

Table 62. UART Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UARTAPP can support is 3.25 Mbps. The maximum baud rate of DebugUART is 115.2 kbps.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (which is APBX clock = 24 MHz).

3.5.15.2 UART Receive Timing

Figure 43 shows the UART receive timing, showing only eight data bits and one stop bit. Table 63 describes the timing parameter (UA2) shown in the figure.

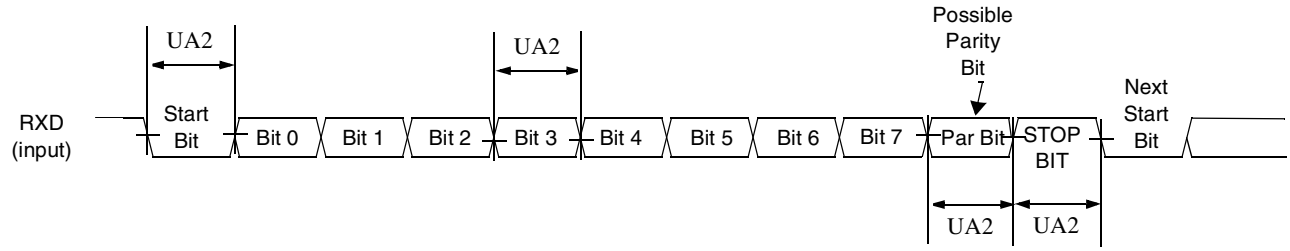

Figure 43. UART Receive Timing Diagram

Table 63. UART Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
UA2	Receive bit time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UARTAPP can support is 3.25 Mbps. The maximum baud rate of DebugUART is 115 kbps.

4 Package Information and Contact Assignments

4.1 Case MAPBGA-289, 14 x 14 mm, 0.8 mm Pitch

The following notes apply to Figure 44:

- All dimensions are in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement excludes any effect of mark on top surface of package.

Figure 44 shows the i.MX28 production package.

Figure 44. i.MX28 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments

Table 64 shows power and ground contact assignments for the MAPBGA package.

Table 64. MAPBGA Power and Ground Contact Assignments

Contact Name	Contact Assignment
VDDA1	C13
VDDD	G12,G11,F10,F11,K12,F12,G10
VDDIO18	G8,F9,F8,G9
VDDIO33	H8,J8,N3,G3,E6,J9,J10,A7,E16
VDDIO33_EMI	N17
VDDIO_EMI	P11,R13,N13,N15,G17,M12,M10,G13,M11,L13,G15

Table 64. MAPBGA Power and Ground Contact Assignments (continued)

Contact Name	Contact Assignment
VDDIO_EMIQ	K15,J13,R15
VDDXTAL	C12
VSS	E15,L11,A1,K10,K11,J11,M14,H11,U1,H9,H12,H3,K9,C16,L10,H16,J12,H10,B7,E5,J15,A9,N4
VSSA1	B13
VSSA2	B11
VSSIO_EMI	F16,R10,H14,M16,F14,L12,P16,U17,T14,P14,R12

4.3 Signal Contact Assignments

Table 65 lists the i.MX287 MAPBGA package signal contact assignments.

Table 65. i.MX287 MAPBGA Contact Assignments

Signal Name	Contact Assignment
AUART0_CTS	J6
AUART0_RTS	J7
AUART0_RX	G5
AUART0_TX	H5
AUART1_CTS	K5
AUART1_RTS	J5
AUART1_RX	L4
AUART1_TX	K4
AUART2_CTS	H6
AUART2_RTS	H7
AUART2_RX	F6
AUART2_TX	F5
AUART3_CTS	L6
AUART3_RTS	K6
AUART3_RX	M5
AUART3_TX	L5
BATTERY	A15
DCDC_BATT	B15
DCDC_GND	A17
DCDC_LN1	B17
DCDC_LP	A16

Signal Name	Contact Assignment
EMI_DQS1N	J16
EMI_ODT0	R17
EMI_ODT1	T17
EMI_RASN	R16
EMI_VREF0	R14
EMI_VREF1	K13
EMI_WEN	T15
ENET0_COL	J4
ENET0_CRS	J3
ENET0_MDC	G4
ENET0_MDIO	H4
ENET0_RXD0	H1
ENET0_RXD1	H2
ENET0_RXD2	J1
ENET0_RXD3	J2
ENET0_RX_CLK	F3
ENET0_RX_EN	E4
ENET0_TXD0	F1
ENET0_TXD1	F2
ENET0_TXD2	G1
ENET0_TXD3	G2

Signal Name	Contact Assignment
LCD_D17	R3
LCD_D18	U4
LCD_D19	T4
LCD_D20	R4
LCD_D21	U5
LCD_D22	T5
LCD_D23	R5
LCD_DOTCLK	N1
LCD_ENABLE	N5
LCD_HSYNC	M1
LCD_RD_E	P4
LCD_RESET	M6
LCD_RS	M4
LCD_VSYNC	L1
LCD_WR_RWN	K1
LRADC0	C15
LRADC1	C9
LRADC2	C8
LRADC3	D9
LRADC4	D13
LRADC5	D15

Table 65. i.MX287 MAPBGA Contact Assignments (continued)

Signal Name	Contact Assignment
EMI_D04	P13
EMI_D05	P17
EMI_D06	L14
EMI_D07	M17
EMI_D08	G16
EMI_D09	H15
EMI_D10	G14
EMI_D11	J14
EMI_D12	H13
EMI_D13	H17
EMI_D14	F13
EMI_D15	F17
EMI_DDR_OPEN	K14
EMI_DDR_OPEN_FB	L15
EMI_DQM0	M15
EMI_DQM1	F15
EMI_DQS0	K17
EMI_DQS0N	K16
EMI_DQS1	J17

Signal Name	Contact Assignment
JTAG_TRST	D14
LCD_CS	P5
LCD_D00	K2
LCD_D01	K3
LCD_D02	L2
LCD_D03	L3
LCD_D04	M2
LCD_D05	M3
LCD_D06	N2
LCD_D07	P1
LCD_D08	P2
LCD_D09	P3
LCD_D10	R1
LCD_D11	R2
LCD_D12	T1
LCD_D13	T2
LCD_D14	U2
LCD_D15	U3
LCD_D16	T3

Signal Name	Contact Assignment
SSP2_MOSI	C3
SSP2_SCK	A3
SSP2_SS0	C4
SSP2_SS1	D3
SSP2_SS2	D4
SSP3_MISO	B2
SSP3_MOSI	C2
SSP3_SCK	A2
SSP3_SS0	D2
TESTMODE	C10
USB0DM	A10
USB0DP	B10
USB1DM	B8
USB1DP	A8
VDD1P5	D16
VDD4P2	A13
VDD5V	E17
XTALI	A12
XTALO	B12

4.4 i.MX280 Ball Map

Table 66 shows the i.MX280 MAPBGA ball map.

Table 66. 289-Pin i.MX280 MAPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS	NC	SSP2_SCK	SSP0_CMD	SSP0_DATA3	SSP0_SCK	VDDIO33	USB1DP	VSS	USB0DM	PSWITCH	XTALI	VDD4P2	RESETN	BATTERY	DCDC_LP	DCDC_GND	A

Table 67. 289-Pin i.MX283 MAPBGA Ball Map (continued)

	U	T	R	P	N	M	L
1	VSS	LCD_D12	LCD_D10	LCD_D07	NC	NC	NC
2	LCD_D14	LCD_D13	LCD_D11	LCD_D08	LCD_D06	LCD_D04	LCD_D02
3	LCD_D15	LCD_D16	LCD_D17	LCD_D09	VDDIO33	LCD_D05	LCD_D03
4	LCD_D18	LCD_D19	LCD_D20	LCD_RD_E	VSS	LCD_RS	AUART1_RX
5	LCD_D21	LCD_D22	LCD_D23	LCD_CS	NC	NC	NC
6	GPMI_D06	GPMI_D07	GPMI_RDN	GPMI_ALE	GPMI_RDY0	LCD_RESET	NC
7	GPMI_D03	GPMI_D04	GPMI_D05	GPMI_CLE	GPMI_CE0N	NC	PWM1
8	GPMI_D00	GPMI_D01	GPMI_D02	GPMI_WRN	GPMI_RDY1	NC	NC
9	EMI_A08	EMI_A13	EMI_A06	EMI_CE1N	GPMI_CE1N	NC	GPMI_RESETN
10	EMI_A04	EMI_A11	VSSIO_EMI	EMI_A09	EMI_A14	VDDIO_EMI	VSS
11	EMI_A12	EMI_A03	EMI_A05	VDDIO_EMI	EMI_A07	VDDIO_EMI	VSS
12	EMI_A01	EMI_BA1	VSSIO_EMI	EMI_CE0N	EMI_BA2	VDDIO_EMI	VSSIO_EMI
13	EMI_A10	EMI_CKE	VDDIO_EMI	EMI_D04	VDDIO_EMI	EMI_D01	VDDIO_EMI
14	EMI_A02	VSSIO_EMI	EMI_VREF0	VSSIO_EMI	EMI_D03	VSS	EMI_D06
15	EMI_A00	EMI_WEN	VDDIO_EMIQ	EMI_D02	VDDIO_EMI	EMI_DQM0	EMI_DDR_OPEN_FB
16	EMI_CASN	EMI_BA0	EMI_RASN	VSSIO_EMI	EMI_D00	VSSIO_EMI	EMI_CLKN
17	VSSIO_EMI	EMI_ODT1	EMI_ODT0	EMI_D05	VDDIO33_EMI	EMI_D07	EMI_CLK
	U	T	R	P	N	M	L

4.6 i.MX286 Ball Map

Table 68 shows the i.MX286 MAPBGA ball map.

Table 68. 289-Pin i.MX286 MAPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS	NC	SSP2_SCK	SSP0_CMD	SSP0_DATA3	SSP0_SCK	VDDIO33	USB1DP	VSS	USB0DM	PSWITCH	XTALI	VDD4P2	RESETN	BATTERY	DCDC_LP	DCDC_GND	A

Table 68. 289-Pin i.MX286 MAPBGA Ball Map (continued)

	U	T	R	P	N	M	L
1	VSS	LCD_D12	LCD_D10	LCD_D07	NC	NC	NC
2	LCD_D14	LCD_D13	LCD_D11	LCD_D08	LCD_D06	LCD_D04	LCD_D02
3	LCD_D15	LCD_D16	LCD_D17	LCD_D09	VDDIO33	LCD_D05	LCD_D03
4	LCD_D18	LCD_D19	LCD_D20	LCD_RD_E	VSS	LCD_RS	AUART1_RX
5	LCD_D21	LCD_D22	LCD_D23	LCD_CS	NC	NC	NC
6	GPMI_D06	GPMI_D07	GPMI_RDN	GPMI_ALE	GPMI_RDY0	LCD_RESET	NC
7	GPMI_D03	GPMI_D04	GPMI_D05	GPMI_CLE	GPMI_CE0N	GPMI_CE2N	PWM1
8	GPMI_D00	GPMI_D01	GPMI_D02	GPMI_WRN	GPMI_RDY1	GPMI_RDY2	GPMI_RDY3
9	EMI_A08	EMI_A13	EMI_A06	EMI_CE1N	GPMI_CE1N	GPMI_CE3N	GPMI_RESETN
10	EMI_A04	EMI_A11	VSSIO_EMI	EMI_A09	EMI_A14	VDDIO_EMI	VSS
11	EMI_A12	EMI_A03	EMI_A05	VDDIO_EMI	EMI_A07	VDDIO_EMI	VSS
12	EMI_A01	EMI_BA1	VSSIO_EMI	EMI_CE0N	EMI_BA2	VDDIO_EMI	VSSIO_EMI
13	EMI_A10	EMI_CKE	VDDIO_EMI	EMI_D04	VDDIO_EMI	EMI_D01	VDDIO_EMI
14	EMI_A02	VSSIO_EMI	EMI_VREF0	VSSIO_EMI	EMI_D03	VSS	EMI_D06
15	EMI_A00	EMI_WEN	VDDIO_EMIQ	EMI_D02	VDDIO_EMI	EMI_DQM0	EMI_DDR_OPEN_FB
16	EMI_CASN	EMI_BA0	EMI_RASN	VSSIO_EMI	EMI_D00	VSSIO_EMI	EMI_CLKN
17	VSSIO_EMI	EMI_ODT1	EMI_ODT0	EMI_D05	VDDIO33_EMI	EMI_D07	EMI_CLK
	U	T	R	P	N	M	L

4.7 i.MX287 Ball Map

Table 69 shows the i.MX287 MAPBGA Ball Map.

Table 69. 289-Pin i.MX287 MAPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS	SSP3_SCK	SSP2_SCK	SSP0_CMD	SSP0_DATA3	SSP0_SCK	VDDIO33	USB1DP	VSS	USB0DM	PSWITCH	XTALI	VDD4P2	RESETN	BATTERY	DCDC_LP	DCDC_GND	A