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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	454MHz
Co-Processors/DSP	Data; DCP
RAM Controllers	LVDDR, LVDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Boot Security, Cryptography, Hardware ID
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx286dvm4br

such as memories and SD cards, as well as provide battery charging capability for Li-Ion batteries.

The i.MX28 processor includes an additional 128-Kbyte on-chip SRAM to make the device ideal for eliminating external RAM in applications with small footprint RTOS.

The i.MX28 supports connections to various types of external memories, such as mobile DDR, DDR2 and LV-DDR2, SLC and MLC NAND Flash.

The i.MX28 can be connected to a variety of external devices such as high-speed USB2.0 OTG, CAN, 10/100 Ethernet, and SD/SDIO/MMC.

1.1 Device Features

The following lists the features of the i.MX28:

- ARM926EJ-S CPU running at 454 MHz:
  - 16-Kbyte instruction cache and 32-Kbyte data cache
  - ARM embedded trace macrocell (CoreSight™ ETM9™)
  - Parallel JTAG interface
- 128 KBytes of integrated low-power on-chip SRAM
- 128 KBytes of integrated mask-programmable on-chip ROM
- 1280 bits of on-chip one-time-programmable (OCOTP) ROM
- 16-bit mobile DDR (mDDR) (1.8 V), DDR2 (1.8 V) and LV-DDR2 (1.5 V), up to 205 MHz DDR clock frequency with voltage overdrive
- Support for up to eight NAND Flash memory devices with up to 20-bit BCH ECC
- Four synchronous serial ports (SSP) for SDIO/MMC/MS/SPI: SSP0, SSP1, SSP2, and SSP3. SSP0 and SSP1 can support three modes,1-bit, 4-bit, and 8-bit, whereas SSP2 and SSP3 can support only 1-bit and 4-bit modes.
- 10/100-Mbps Ethernet MAC compatible with IEEE Std 802.3™:
  - Single 10/100 Ethernet with GMII/RMII or Dual 10/100 Ethernet with RMII interface
  - Supporting IEEE Std 1588™-compatible hardware timestamp
  - Supporting 50-MHz/25-MHz clock output for external Ethernet PHY
- Two 2.0B protocol-compatible Controller Area Network (CAN) interfaces
- One USB2.0 OTG device/host controller and PHY
- One USB2.0 host controller and PHY
- LCD controller, up to 24-bit RGB (DOTCK) modes and 24-bit system-mode
- Pixel-processing pipeline (PXP) supports full path from color-space conversion, scaling, alpha-blending to rotation without intermediate memory access.
- SPDIF transmitter
- Dual serial audio interface (SAIF) to support full-duplex transmit and receive operations; each SAIF supports three stereo pairs
- Five application Universal Asynchronous Receiver-Transmitters (UARTs), up to 3.25 Mbps with hardware flow control

Table 4 describes the digital and analog modules of the device.

Table 4. i.MX28 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
APBHDMA	AHB to APBH Bridge with DMA	System control	The AHB to APBH bridge with DMA includes the AHB-to-APB PIO bridge for memory-mapped I/O to the APB devices, as well a central DMA facility for devices on this bus. The bridge provides a peripheral attachment bus running on the AHB's HCLK. (The 'H' in APBH denotes that the APBH is synchronous to HCLK, as compared to APBX, which runs on the crystal-derived XCLK.) The DMA controller transfers read and write data to and from each peripheral on APBH bridge.
APBXDMA	AHB to APBX Bridge with DMA	System control	The AHB-to-APBX bridge includes the AHB-to-APB PIO bridge for memory-mapped I/O to the APB devices, as well a central DMA facility for devices on this bus. The AHB-to-APBX bridge provides a peripheral attachment bus running on the AHB's XCLK. (The 'X' in APBX denotes that the APBX runs on a crystal-derived clock, as compared to APBH, which is synchronous to HCLK.) The DMA controller transfers read and write data to and from each peripheral on APBX bridge.
ARM9 or ARM926	ARM926EJ-S CPU	ARM®	The ARM926 Platform consists of the ARM926EJ-S™ core and the ETM real-time debug modules. It contains the 16-Kbyte L1 instruction cache, 32-Kbyte L1 data cache, 128-Kbyte ROM and 128-Kbyte RAM.
AUART(5)	Application UART interface	Connectivity peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 3.25 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 16-byte FIFO on Tx and 16-byte FIFO on Rx supporting auto-baud detection
BCH	Bit-correcting ECC accelerator	Connectivity peripherals	The Bose, Ray-Chaudhuri, Hocquenghem (BCH) Encoder and Decoder module is capable of correcting from 2 to 20 single bit errors within a block of data no larger than about 900 bytes (512 bytes is typical) in applications such as protecting data and resources stored on modern NAND Flash devices.
BSI	Boundary Scan Interface	Connectivity peripherals	The boundary scan interface is provided to enable board level testing. There are five pins on the device which is used to implement the IEEE Std 1149.1™ boundary scan protocol.
CLKCTRL	Clock control module	Clocks	The clock control module, or CLKCTRL, generates the clock domains for all components in the i.MX28 system. The crystal clock or PLL clock are the two fundamental sources used to produce most of the clock domains. For lower performance and reduced power consumption, the crystal clock is selected. The PLL is selected for higher performance requirements but requires increased power consumption. In most cases, when the PLL is used as the source, a Phase Fractional Divider (PFD) can be programmed to reduce the PLL clock frequency by up to a factor of 2.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

3.1.2 DC Operating Conditions

Table 8 provides the DC recommended operating conditions.

Table 8. Recommended Power Supply Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog Core Supply Voltage	V_{DDA}	1.62	—	2.10	V
Digital Core Supply Voltage *Specification dependent on frequency.*[1, 2]	V_{DDD}	1.35	—	1.55	V
Digital Supply Voltages: • VDDIO33/VDDIO33_EMI • VDDIO18	V_{DDIO33}/V_{DDIO33_EMI}/V_{DDIO18}	 3.0 1.7	 — —	 3.6 1.9	V
EMI Digital I/O Supply Voltage: • DDR2/mDDR • LVDDR2	$V_{DDIO.EMI}$/V_{DDIO_EMIQ}	 1.7 1.425	 1.8 1.5	 1.9 1.625	V
Battery / DCDC Input Voltage—BATT, DCDC_BATT	BATT DCDC_BATT	3.10[3]	—	4.242	V
VDD5V Supply Voltage	—	4.75	5.00	5.25	V
Offstate Current:[4] • 32-kHz RTC off, BATT = 4.2 V • 32-kHz RTC on, BATT = 4.2 V	 — —	 — —	 21 23	 47 51	 µA µA

1 For optimum USB jitter performance, V_{DDD} = 1.35 V or greater.

2 V_{DDD} supply minimum voltage includes 75 mV guardband.

3 Tested with only the i.MX28 processor loading the MX28 PMU output rails during start up. With external loadings (for example, one DDR2 device and SD Card/NAND Flash), MX28 PMU was tested at BATT/DCDC_BATT > 3.30 V.

4 When the real-time clock is enabled, the chip consumes additional current in the OFF state to keep the crystal oscillator and the real-time clock running.

Table 9 provides the DC operating temperature conditions.

Table 9. Operating Temperature Conditions

Parameter[1, 2, 3]	Symbol	Min	Typ	Max	Unit
Commercial Ambient Operating Temperature Range	T_A	–20	—	70	°C
Commercial Junction Temperature Range	T_J	–20	—	85	°C
Industrial Ambient Operating Temperature Range	T_A	–40	—	85	°C
Industrial Junction Temperature Range	T_J	–40	—	105	°C

1 In most portable systems designs, battery and display specifications limits the operating range to well within these specifications. Most battery manufacturers recommend enabling battery charge only when the ambient temperature is between 0°C and 40°C. To ensure that battery charging does not occur outside the recommended temperature range, the system ambient temperature may be monitored by connecting a thermistor to the LRADC0 or LRADC6 pin on the i.MX28.

2 For applications powered by external 5V only, the Maximum Ambient Operating Temperature specified in Table 9 may not be achieved. Application developers need to do the worst-case power consumption estimation, and then calculate the Total On-chip Power Dissipation based on the equations specified in note 3 below.

3 Maximum Ambient Operating Temperature may be limited due to on-chip power dissipation. $T_{A\ (MAX)} \leq T_J - (\Theta_{JA} \times P_D)$ where:
T_J = Maximum Junction Temperature
Θ_{JA} = Package Thermal Resistance. See Section 3.2, “Thermal Characteristics.”
P_D = Total On-chip Power Dissipation =PVDD4P2 + PBatteryCharger + PDCDC + PLinearRegulators + PInternal. Depending on the application, some of these power dissipation terms may not apply.
PVDD4P2 = VDD4P2 On-Chip Power Dissipation = (VDD5V - VDD4P2) x IDD4P2
PBatteryCharger = Battery Charger On-Chip Power Dissipation = (VDD5V - BATT) x ICHARGE
PDCDC = DC-DC Converter On-Chip Power Dissipation = (BATT x DCDC Input Current) x (1 - efficiency)
PLinearRegulators = Linear Regulator On-Chip Power Dissipation = (VDD5V - VDDIO) x (IDDIO + IDDA + IDDD + IDD1P5) + (VDDIO - VDDA) x (IDDA + IDDD) + (VDDA - VDDD) x IDDD + (VDDA - VDD1P5) x IDD1P5
PInternal = Internal Digital On-Chip Power Dissipation = ~VDDD x IDDD

Table 10 provides the recommended analog operating conditions.

Table 10. Recommended Analog Operating Conditions

Parameter	Min	Typ	Max	Unit
Low Resolution ADC Input Impedance (CH0 - CH5)	>1	—	—	MΩ

Table 11 shows the PSWITCH input characteristics. See the reference schematics for the recommended PSWITCH button circuitry.

Table 11. PSWITCH Input Characteristics

Parameter	HW_PWR_STS_PSWITCH	Min	Max	Unit
PSWITCH LOW LEVEL	0x00	0.00	0.30	V
PSWITCH MID LEVEL & STARTUP[1]	0x01	0.65	1.50	V
PSWITCH HIGH LEVEL[2]	0x11	(1.1 * VDDXTAL) + 0.58	2.45	V

1 A MID LEVEL PSWITCH state can be generated by connecting the VDDXTAL output of the SoC to PSWITCH through a switch.

2 PSWITCH acts like a high impedance input (>300 kΩ) when the voltage applied to it is less than 1.5V. However, above 1.5V it becomes lower impedance. To simplify design, it is recommended that a 10 kΩ resistor to VDDIO be applied to PSWITCH to set the HIGH LEVEL state (the PSWITCH input can tolerate voltages greater than 2.45 V as long as there is a 10 kΩ resistor in series to limit the current).

Table 12 shows a test case example for Run IDD.

Table 12. Run IDD Test Case[1,2]

Power Rail	Conditions	Min	Typ	Max	Unit
VDDD	1.57 V	—	150	188	mA
VDDIO33	3.62 V	—	31	34	mA
VDDA	2.12 V	—	1.11	1.17	mA
VDDIO_EMI	1.92 V	—	1.01	1.08	mA
VDDIO18	1.92 V	—	0.61	2.97	µA

1 CPUCLK = 300 MHz, AHBCLK = 150 MHz

2 Continuous read / write to the cache memory

Table 25. Digital Pin DC Characteristics for GPIO in 3.3-V Mode (continued)

Parameter	Symbol	Min	Max	Unit
10-K pull-up resistance[2]	Rpu10k	8	12	kΩ
47-K pull-up resistance	Rpu47k	39	56	kΩ

1 The conditions of the current measurements for all different drives are as follows:
IOL: at 0.4 V
IOH: at VDDIO * 0.8 V
Maximum corner for 3.3 V mode: 3.6 V, -40°C, fast process.
Minimum corner for 3.3 V mode: 3.0 V, 105°C, slow process.
8 gpio pins (LCD_D0-D7) and 2 gpio_clk pins (LCD_DOTCLK and LCD_WR_RWN) simultaneously loaded.

2 See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

Table 26 shows the digital pin DC characteristics for GPIO in 1.8 V mode.

Table 26. Digital Pin DC Characteristics for GPIO in 1.8 V Mode

	Symbol	Min	Max	Unit
Input voltage high (DC)	VIH	0.7 × VDDIO18	VDDIO18	V
Input voltage low (DC)	VIL	—	0.3 × VDDIO18	V
Output voltage high (DC)	VOH	0.8 * VDDIO18	—	V
Output voltage low (DC)	VOL	—	0.2 × VDDIO18	V
Output source current[1] (DC) *gpio*	IOH – low	-2.2	—	mA
	IOH – medium	-3.5	—	mA
	IOH – high	-4.0	—	mA
Output sink current (DC) *gpio*	IOL – low	3.3	—	mA
	IOL – medium	7.0	—	mA
	IOL – high	7.5	—	mA
Output source current (DC) *gpio_clk*	IOH – low	-4.2	—	mA
	IOH – high	-6.0	—	mA
Output sink current (DC) *gpio_clk*	IOL – low	6.8	—	mA
	IOL – high	11.5	—	mA
10-K pull-up resistance[2]	Rpu10k	8	12	kΩ
47-K pull-up resistance	Rpu47k	39	56	kΩ

1 The condition of the current measurements for all different drives are as follows:
Maximum corner for 1.8 V mode: 1.9 V, -40°C, Fast process.
Minimum corner for 1.8 V mode: 1.7 V, 105°C, Slow process.
1 gpio pin (GPMI_D0) and 1 gpio_clk pin (GPMI_WRN) simultaneously loaded.

2 See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

3.4 I/O AC Timing and Parameters

Figure 3 and Figure 4 show the Driver Used for AC Simulation Testpoint and the Output Pad Transition Waveform.

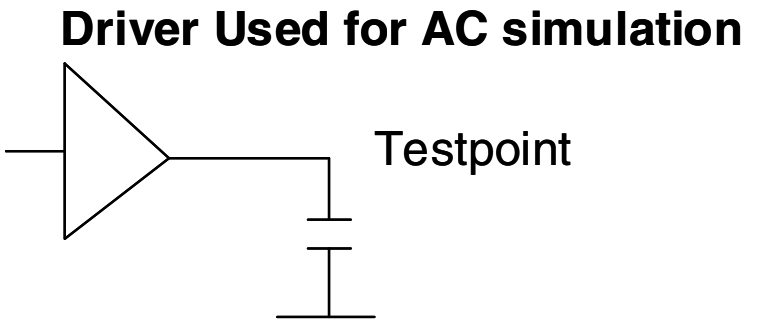

Figure 3. Driver Used for AC Simulation Testpoint

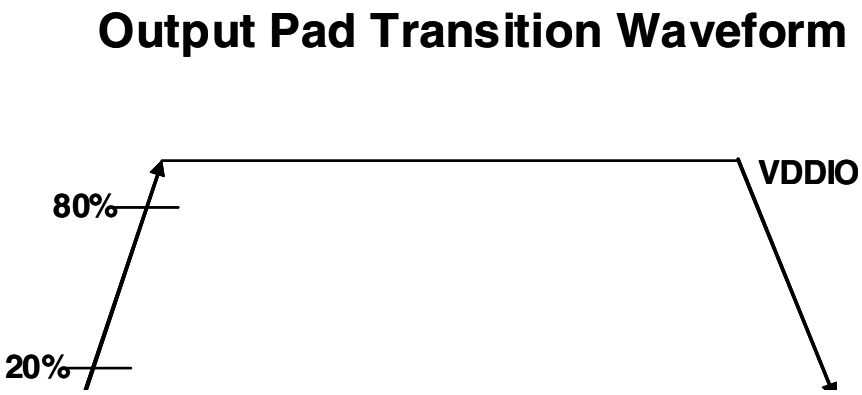

Figure 4. Output Pad Transition Waveform

Table 27 shows the base GPIO AC timing and parameters.

Table 27. Base GPIO

Parameters	Symbol	Test Voltage	Test Capacitance	Min Rise/Fall		MaxRise/Fall		Unit	Notes
Duty cycle	Fduty	—	—	—		—		%	—
Output pad transition times (maximum drive)	tpr	1.7~1.9V	10 pF	0.82	0.91	1.93	1.97	ns	—
		1.7~1.9V	20 pF	1.18	1.22	2.69	2.71		—
		1.7~1.9V	50 pF	2.11	2.03	4.62	4.44		—
		3.0~3.6V	10 pF	1.04	1.08	2.46	2.18		—
		3.0~3.6V	20 pF	1.42	1.5	3.29	3		—
		3.0~3.6V	50 pF	2.46	2.61	5.34	5.12		—

Table 27. Base GPIO (continued)

Parameters	Symbol	Test Voltage	Test Capacitance	Min Rise/Fall		MaxRise/Fall		Unit	Notes
Output pad transition times (medium drive)	tpr	1.7~1.9V	10 pF	1.02	1.08	2.34	2.38	ns	—
		1.7~1.9V	20 pF	1.51	1.5	3.34	3.28		—
		1.7~1.9V	50 pF	2.91	2.62	6.24	5.67		—
		3.0~3.6V	10 pF	1.26	1.29	2.9	2.6		—
		3.0~3.6V	20 pF	1.8	1.88	4	3.67		—
		3.0~3.6V	50 pF	3.3	3.46	6.91	6.64		—
Output pad transition times (low drive)	tpr	1.7~1.9V	10 pF	1.62	1.68	3.65	3.68	ns	—
		1.7~1.9V	20 pF	2.55	2.45	5.59	5.37		—
		1.7~1.9V	50 pF	5.42	4.62	11.46	10.01		—
		3.0~3.6V	10 pF	1.95	2.12	4.43	4.25		—
		3.0~3.6V	20 pF	2.96	3.21	6.36	6.25		—
		3.0~3.6V	50 pF	5.89	6.39	12.02	12.18		—
Output pad slew rate (maximum drive)	tps	1.7~1.9V	10 pF	1.39	1.25	0.53	0.52	V/ns	—
		1.7~1.9V	20 pF	0.97	0.93	0.38	0.38		—
		1.7~1.9V	50 pF	0.54	0.56	0.22	0.23		—
		3.0~3.6V	10 pF	2.08	2.00	0.73	0.83		—
		3.0~3.6V	20 pF	1.52	1.44	0.55	0.60		—
		3.0~3.6V	50 pF	0.88	0.83	0.34	0.35		—
Output pad slew rate (medium drive)	tps	1.7~1.9V	10 pF	1.12	1.06	0.44	0.43	V/ns	—
		1.7~1.9V	20 pF	0.75	0.76	0.31	0.31		—
		1.7~1.9V	50 pF	0.39	0.44	0.16	0.18		—
		3.0~3.6V	10 pF	1.71	1.67	0.62	0.69		—
		3.0~3.6V	20 pF	1.20	1.15	0.45	0.49		—
		3.0~3.6V	50 pF	0.65	0.62	0.26	0.27		—
Output pad slew rate (low drive)	tps	1.7~1.9V	10 pF	1.17	1.13	0.47	0.46	V/ns	—
		1.7~1.9V	20 pF	0.75	0.78	0.30	0.32		—
		1.7~1.9V	50 pF	0.35	0.41	0.15	0.17		—
		3.0~3.6V	10 pF	1.11	1.02	0.41	0.42		—
		3.0~3.6V	20 pF	0.73	0.67	0.28	0.29		—
		3.0~3.6V	50 pF	0.37	0.34	0.15	0.15		—
Input pad average hysteresis	tih	1.7 V–1.9 V	—	100		75		mV	—
		3.0 V–3.6 V	—	100		50			—

Table 29. CLK-Type GPIO (continued)

Parameters	Symbol	Test Voltage	Test Capacitance	Min Rise/Fall		Max Rise/Fall		units	Notes
Output pad slew rate (medium drive)	tps	1.7~1.9V	10 pF	1.50	1.50	0.61	0.63	ns	—
		1.7~1.9V	20 pF	0.93	1.00	0.39	0.42		—
		1.7~1.9V	50 pF	0.43	0.52	0.18	0.22		—
		3.0~3.6V	10 pF	2.40	2.43	0.98	1.05		—
		3.0~3.6V	20 pF	1.58	1.53	0.65	0.67		—
		3.0~3.6V	50 pF	0.76	0.71	0.32	0.31		—
Input pad average hysteresis	tih	1.7 V–1.9 V	—	100		75		mV	—
		3.0 V–3.6 V	—	100		50			—

3.5 Module Timing and Electrical Parameters

3.5.1 ADC Electrical Specifications

This section describes the electrical specifications, including DC and AC information, of Low-Resolution ADC (LRADC) and High-Speed ADC (HSADC).

3.5.1.1 LRADC Electrical Specifications

Table 30 shows the electrical specifications for the LRADC.

Table 30. LRADC Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
AC Electrical Specification					
Input capacitance (C_p)	No pin/pad capacitance included	—	0.5	—	pF
Resolution	—		12		bits
Maximum sampling rate[1] (fs)	—	—	—	428	kHz
Power-up time[2]	—		1		sample cycles
DC Electrical Specification					
DC input voltage		0		1.85	V
Current consumption[3] VDDA	—	—	10	—	µA
Touchscreen Interface					
Expected plate resistance	—	200	—	50000	Ω

1 There is no sample and hold circuit in LRADC, so it is only for DC input voltage or ones with very small slope.

2 This comprises only the required initial dummy conversion cycle, NOT including the Analog part power-up time.

3.5.2 DPLL Electrical Specifications

This section includes descriptions of the USB PLL electrical specifications and Ethernet PLL electrical specifications.

3.5.2.1 USB PLL Electrical Specifications

The i.MX28 integrates a high-frequency USB PLL that provides the 480-MHz clock for the USB and other system blocks.

Table 32 lists the USB PLL output electrical specifications.

Table 32. USB PLL Specifications

Parameter	Test Conditions	Min	Typ	Max	Unit
PLL lock time	—	—	—	10	µs

3.5.2.2 Ethernet PLL Electrical Specifications

i.MX28 provides a 50-MHz/25-MHz output clock, called the Ethernet PLL output.

Table 33 lists the Ethernet PLL output electrical specifications.

Table 33. Ethernet PLL Specifications

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Duty Cycle	—	45	50	55	%
PLL lock time	—	—	—	10	µs
Cycle to cycle jitter	—	—	25	—	ps
Clock output frequency tolerance[1]	—	—	—	+/-20	ppm

[1] This Ethernet output clock tolerance specification is the contribution from the PLL only and assumes a perfect 24 MHz clock/crystal source with 0 ppm deviation. The 24 MHz crystal frequency tolerance/deviation should be added to this number for the total Ethernet clock output frequency tolerance.

Figure 10 shows MII transmit signal timings. Table 39 describes the timing parameters (M5–M8) shown in the figure.

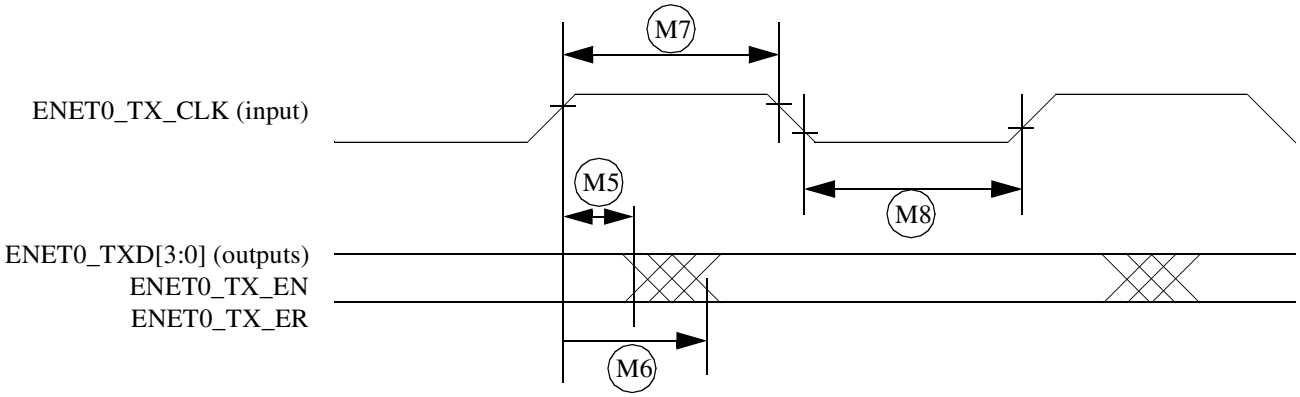

Figure 10. MII Transmit Signal Timing Diagram

Table 39. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER invalid	5	—	ns
M6	ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER valid	—	20	ns
M7	ENET0_TX_CLK pulse width high	35%	65%	ENET0_TX_CLK period
M8	ENET0_TX_CLK pulse width low	35%	65%	ENET0_TX_CLK period

[1] ENET0_TX_EN, ENET0_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.5.4.1.3 MII Asynchronous Inputs Signal Timing (ENET0_CRS and ENET0_COL)

Figure 11 shows MII asynchronous input timings. Table 40 describes the timing parameter (M9) shown in the figure.

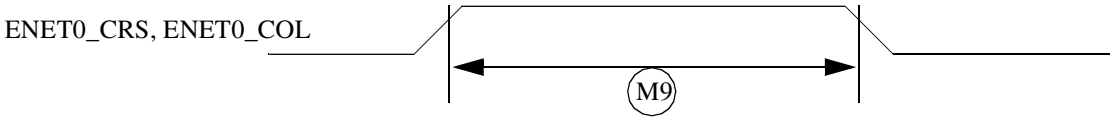

Figure 11. MII Async Inputs Timing Diagram

Table 40. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET0_CRS to ENET0_COL minimum pulse width	1.5	—	ENET0_TX_CLK period

[1] ENET0_COL has the same timing in 10-Mbit 7-wire interface mode.

Figure 14 shows TRACECLK signal timings. Table 43 describes the timing parameters shown in the figure.

Figure 14. TRACECLK Signal Timing Diagram

Table 43. TRACECLK Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
Tr	Clock and data raise time	3	—	ns
Tf	Clock and data fall time	3	—	ns
Twh	High pulse wide	2	—	ns
Twl	Low pulse wide	2	—	ns
Tcyc	Clock period	12.5	—	ns

3.5.5.2 Trace Data Signal Timing

Figure 15 shows the setup and hold requirements of the trace data pins with respect to TRACECLK. Table 44 describes the timing parameters shown in the figure.

Figure 15. Trace Data Signal Timing Diagram

Table 44. Trace Data Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
Ts	Data setup	2	—	ns
Th	Data hold	2	—	ns

3.5.6 FlexCAN AC Timing

Table 45 and Table 46 show voltage requirements for the FlexCAN transceiver Tx and Rx pins.

Table 45. Tx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-level output voltage	V_{OH}	2	—	Vcc[1] + 0.3	V
Low-level output voltage	V_{OL}	—	0.8	—	V

1 Vcc = +3.3 V ± 5%

Table 46. Rx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	0.8 × Vcc[1]	—	Vcc[1]	V
Low-level input voltage	V_{IL}	—	0.4	—	V

1 Vcc = +3.3 V ± 5%

Figure 16 through Figure 19 show the FlexCAN timing, including timing of the standby and shutdown signals.

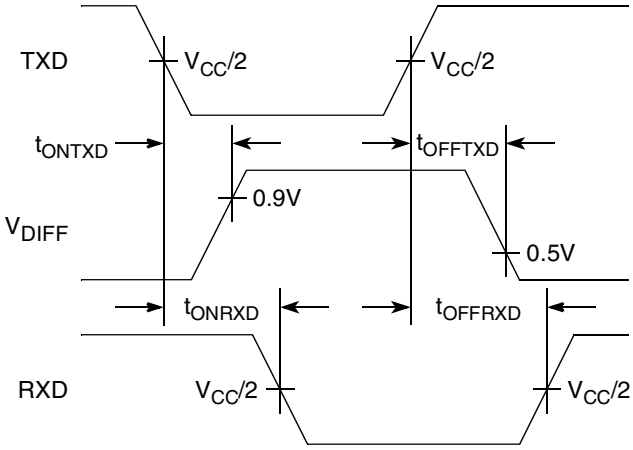

Figure 16. FlexCAN Timing Diagram

3.5.9 Inter IC (I^2C) Timing

The I^2C module is designed to support up to 400-Kbps I^2C connection compliant with I^2C bus protocol. The following section describes I^2C SDA and SCL signal timings.

Figure 25 shows the timing of the I^2C module. Table 49 describes the I^2C module timing parameters (IC1–IC11) shown in the figure.

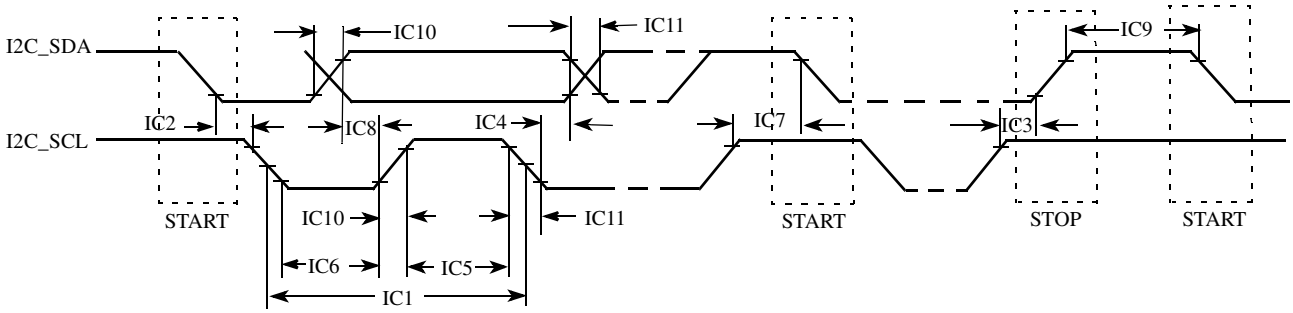

Figure 25. I^2C Module Timing Diagram

Table 49. I^2C Module Timing Parameters: 1.8 V – 3.6 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2C_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2C_SCL clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2C_SCL clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2C_SDA and I2C_SCL signals	—	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both I2C_SDA and I2C_SCL signals	—	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for the I2C_SDA signal in order to bridge the undefined region of the falling edge of I2C_SCL.

2 The maximum IC4 has to be met only if the device does not stretch the LOW period (ID no IC5) of the I2C_SCL signal.

3 A fast-mode I2C bus device can be used in a standard-mode I^2C bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line max_rise_time (ID No IC9) + data_setup_time (ID No IC7) = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the I2C_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

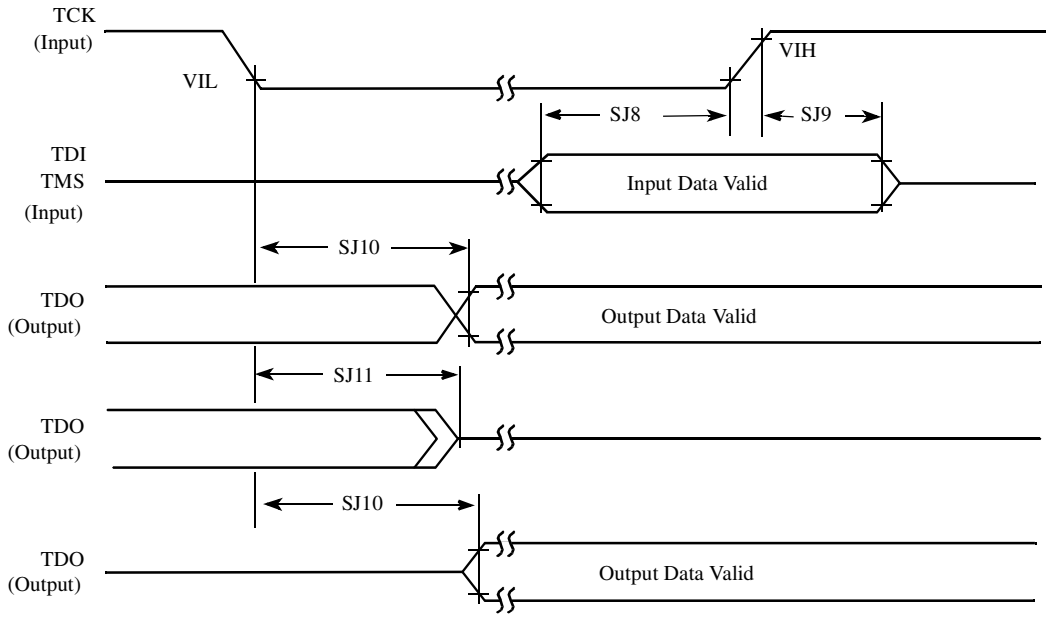

Figure 28. Test Access Port Timing Diagram

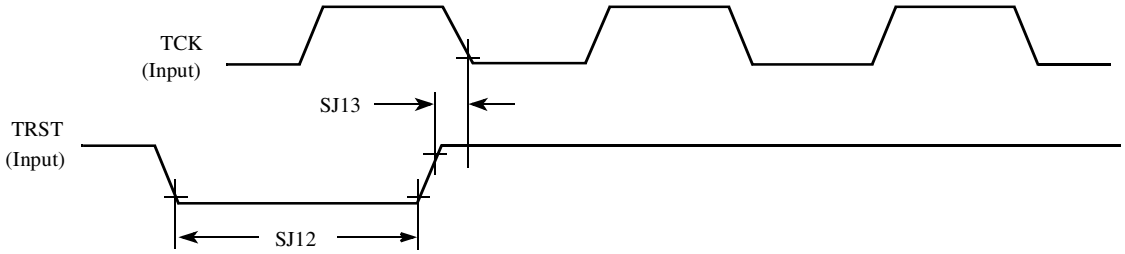

Figure 29. $\overline{\text{TRST}}$ Timing Diagram

Table 50. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100	—	ns
SJ2	TCK clock pulse width measured at V_M[1]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns

Table 54. SAIF Transmitter Timing

ID	Parameter	Min.	Max.	Unit
SS1	BITCLK period	81.4	—	ns
SS2	BITCLK high period	36.0	—	ns
SS3	BITCLK rise time	—	6.0	ns
SS4	BITCLK low period	36.0	—	ns
SS5	BITCLK fall time	—	6.0	ns
SS6	BITCLK high to LRCLK high	—	15.0	ns
SS7	BITCLK high to LRCLK low	—	15.0	ns
SS8	LRCLK rise time	—	6.0	ns
SS9	LRCLK fall time	—	6.0	ns
SS10	BITCLK high to SDATA valid from high impedance	—	15.0	ns
SS11	BITCLK high to SDATA high/low	—	15.0	ns
SS12	BITCLK high to SDATA high impedance	—	15.0	ns
SS13	SDATA rise/fall time	—	6.0	ns

3.5.12.2 SAIF Receiver Timing

Figure 34 shows the timing for the SAIF receiver with internal clock. Table 55 describes the timing parameters (SS1–SS17) shown in the figure.

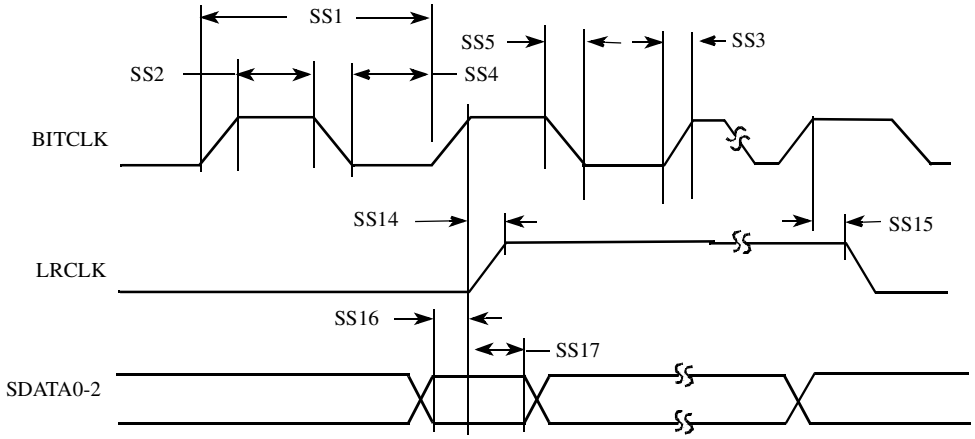

Figure 34. SAIF Receiver Timing Diagram

3.5.14 Synchronous Serial Port (SSP) AC Timing

This section describes the electrical information of the SSP, which includes SD/MMC4.3 (Single Data Rate) timing, MMC4.4 (Dual Date Rate) timing, MS (Memory Stick) timing, and SPI timing.

3.5.14.1 SD/MMC4.3 (Single Data Rate) AC Timing

Figure 36 depicts the timing of SD/MMC4.3, and Table 57 lists the SD/MMC4.3 timing characteristics.

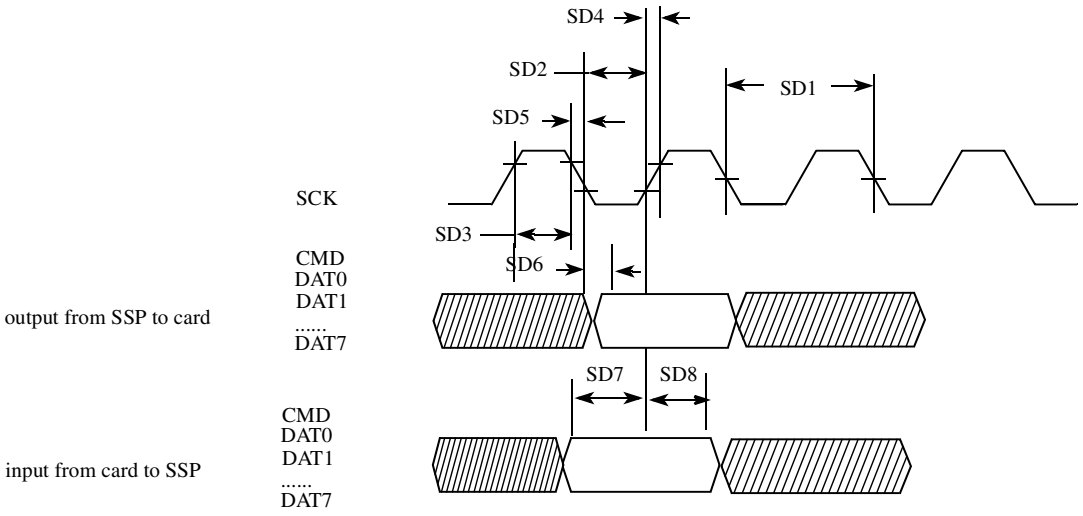

Figure 36. SD/MMC4.3 Timing

Table 57. SD/MMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
SSP Output / Card Inputs CMD, DAT (Reference to CLK)					
SD6	SSP Output Delay	t_{OD}	-5	5	ns
SSP Input / Card Outputs CMD, DAT (Reference to CLK)					

Table 64. MAPBGA Power and Ground Contact Assignments (continued)

Contact Name	Contact Assignment
VDDIO_EMIQ	K15,J13,R15
VDDXTAL	C12
VSS	E15,L11,A1,K10,K11,J11,M14,H11,U1,H9,H12,H3,K9,C16,L10,H16,J12,H10,B7,E5,J15,A9,N4
VSSA1	B13
VSSA2	B11
VSSIO_EMI	F16,R10,H14,M16,F14,L12,P16,U17,T14,P14,R12

4.3 Signal Contact Assignments

Table 65 lists the i.MX287 MAPBGA package signal contact assignments.

Table 65. i.MX287 MAPBGA Contact Assignments

Signal Name	Contact Assignment
AUART0_CTS	J6
AUART0_RTS	J7
AUART0_RX	G5
AUART0_TX	H5
AUART1_CTS	K5
AUART1_RTS	J5
AUART1_RX	L4
AUART1_TX	K4
AUART2_CTS	H6
AUART2_RTS	H7
AUART2_RX	F6
AUART2_TX	F5
AUART3_CTS	L6
AUART3_RTS	K6
AUART3_RX	M5
AUART3_TX	L5
BATTERY	A15
DCDC_BATT	B15
DCDC_GND	A17
DCDC_LN1	B17
DCDC_LP	A16

Signal Name	Contact Assignment
EMI_DQS1N	J16
EMI_ODT0	R17
EMI_ODT1	T17
EMI_RASN	R16
EMI_VREF0	R14
EMI_VREF1	K13
EMI_WEN	T15
ENET0_COL	J4
ENET0_CRS	J3
ENET0_MDC	G4
ENET0_MDIO	H4
ENET0_RXD0	H1
ENET0_RXD1	H2
ENET0_RXD2	J1
ENET0_RXD3	J2
ENET0_RX_CLK	F3
ENET0_RX_EN	E4
ENET0_TXD0	F1
ENET0_TXD1	F2
ENET0_TXD2	G1
ENET0_TXD3	G2

Signal Name	Contact Assignment
LCD_D17	R3
LCD_D18	U4
LCD_D19	T4
LCD_D20	R4
LCD_D21	U5
LCD_D22	T5
LCD_D23	R5
LCD_DOTCLK	N1
LCD_ENABLE	N5
LCD_HSYNC	M1
LCD_RD_E	P4
LCD_RESET	M6
LCD_RS	M4
LCD_VSYNC	L1
LCD_WR_RWN	K1
LRADC0	C15
LRADC1	C9
LRADC2	C8
LRADC3	D9
LRADC4	D13
LRADC5	D15

Table 65. i.MX287 MAPBGA Contact Assignments (continued)

Signal Name	Contact Assignment
EMI_D04	P13
EMI_D05	P17
EMI_D06	L14
EMI_D07	M17
EMI_D08	G16
EMI_D09	H15
EMI_D10	G14
EMI_D11	J14
EMI_D12	H13
EMI_D13	H17
EMI_D14	F13
EMI_D15	F17
EMI_DDR_OPEN	K14
EMI_DDR_OPEN_FB	L15
EMI_DQM0	M15
EMI_DQM1	F15
EMI_DQS0	K17
EMI_DQS0N	K16
EMI_DQS1	J17

Signal Name	Contact Assignment
JTAG_TRST	D14
LCD_CS	P5
LCD_D00	K2
LCD_D01	K3
LCD_D02	L2
LCD_D03	L3
LCD_D04	M2
LCD_D05	M3
LCD_D06	N2
LCD_D07	P1
LCD_D08	P2
LCD_D09	P3
LCD_D10	R1
LCD_D11	R2
LCD_D12	T1
LCD_D13	T2
LCD_D14	U2
LCD_D15	U3
LCD_D16	T3

Signal Name	Contact Assignment
SSP2_MOSI	C3
SSP2_SCK	A3
SSP2_SS0	C4
SSP2_SS1	D3
SSP2_SS2	D4
SSP3_MISO	B2
SSP3_MOSI	C2
SSP3_SCK	A2
SSP3_SS0	D2
TESTMODE	C10
USB0DM	A10
USB0DP	B10
USB1DM	B8
USB1DP	A8
VDD1P5	D16
VDD4P2	A13
VDD5V	E17
XTALI	A12
XTALO	B12

4.4 i.MX280 Ball Map

Table 66 shows the i.MX280 MAPBGA ball map.

Table 66. 289-Pin i.MX280 MAPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS	NC	SSP2_SCK	SSP0_CMD	SSP0_DATA3	SSP0_SCK	VDDIO33	USB1DP	VSS	USB0DM	PSWITCH	XTALI	VDD4P2	RESETN	BATTERY	DCDC_LP	DCDC_GND	A

5 Revision History

Table 70 summarizes revisions to this document.

Table 70. Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 3	07/2012	• Removed the Power Consumption table, and added Table 12, "Run IDD Test Case›," on page 14. • Updated Table 23, "ON Impedance of EMI Drivers for Different Drive Strengths," on page 20.
Rev. 2	03/2012	• In Section 1.1, “Device Features:” —Updated synchronous serial ports (SSP) support for the i.MX28 —Updated Ethernet support for the i.MX28 —Updated Low-Resolution A/D Converter (LRADC) support for the i.MX28 • Updated Table 2, "i.MX28 Functional Differences," on page 4. • In Table 6, "DC Absolute Maximum Ratings," on page 12, removed the PSWITCH parameter as this paramater is explained in detail in Table 11. • In Table 8, "Recommended Power Supply Operating Conditions," on page 13: —Updated two parameters: “VDD5V Supply Voltage” and “Offstate Current” —Updated the third footnote • In Table 9, "Operating Temperature Conditions," on page 13, added a new footnote in the “Parameter” column. • In Table 13, "Power Supply Characteristics," on page 15, updated the “VDD4P2 Output Current Limit Accuracy” parameter. • In Section 3.1.2.1, “Recommended Operating Conditions for Specific Clock Targets:” —Removed the “System Clocks” table —Updated two TBD values in the first row of Table 14 —Removed the first row in Table 15 —Removed the first row in Table 16 • In Table 20, "Power Mode Settings," on page 17, changed the second column name from “Deep Sleep” to “Offstate.” • Updated Table 22, "EMI Digital Pin DC Characteristics," on page 20. • In Table 30, "LRADC Electrical Specifications," on page 27, updated the “DC Electrical Specification” section. • In Table 31, "HSADC Electrical Specification," on page 28, updated the “DC Electrical Specification” section. • In Section 3.5.5, “Coresight ETM9 AC Interface Timing,” updated the first paragraph. • In Section 3.5.5.1, “TRACECLK Timing,” corrected the title of Table 43. • In Section 3.5.5.2, “Trace Data Signal Timing,” corrected the titles of Figure 15 and Table 44.
Rev. 1	04/2011	• Updated Section 1.1, “Device Features.” • Added Section 3.2, “Thermal Characteristics.” • In Table 1, "Ordering Information," on page 3, added two rows. • Updated Table 2, "i.MX28 Functional Differences," on page 4. • Updated Table 4, "i.MX28 Digital and Analog Modules," on page 7. • In Table 8, "Recommended Power Supply Operating Conditions," on page 13, updated BATT row. • Updated Table 9, "Operating Temperature Conditions," on page 13. • Replaced the term “DC Characteristics” with “Power Consumption” in the title and introduction of the Power Consumption table. Also changed Dissipation to Consumption in first row. • Updated Table 25, "Digital Pin DC Characteristics for GPIO in 3.3-V Mode," on page 21. • Updated Table 26, "Digital Pin DC Characteristics for GPIO in 1.8 V Mode," on page 22. • Updated and added a footnote to Table 33, "Ethernet PLL Specifications," on page 29. • Updated DDR1 row of Table 34, "EMI Command/Address AC Timing," on page 30. • Added Section 4.4, “i.MX280 Ball Map.” • In Section 4.5, “i.MX283 Ball Map,” updated Figure 67.

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