Renesas Electronics America Inc - DS72011RW100FPV Datasheet

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Details	
Product Status	Last Time Buy
Core Processor	SH-2A
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, SCI, Serial Sound
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/ds72011rw100fpv

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	BO	0	R/W	BO Bit Indicates that a register bank has overflowed.
13	CS	0	R/W	CS Bit Indicates that, in CLIP instruction execution, the value has exceeded the saturation upper-limit value or fallen below the saturation lower-limit value.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	M	—	R/W	M Bit
8	Q	—	R/W	Q Bit Used by the DIV0S, DIV0U, and DIV1 instructions.
7 to 4	I[3:0]	1111	R/W	Interrupt Mask Level
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	S	—	R/W	S Bit Specifies a saturation operation for a MAC instruction.
0	T	—	R/W	T Bit True/false condition or carry/borrow bit

These possibilities of each exceptional handling on floating-point operation are shown in the individual instruction descriptions. All exception events that originate in the floating-point operation are assigned as the same FPU exceptional handling event. The meaning of an exception generated by floating-point operation is determined by software by reading from FPSCR and interpreting the information it contains. Also, the destination register is not changed when FPU exception handling operation occurs.

Except for the above, the FPU disables exception handling. In every processing, the bit corresponding to source V, Z, O, U, or I is set to 1, and a default value is generated as the operation result.

- Invalid operation (V): qNaN is generated as the result.
- Division by zero (Z): Infinity with the same sign as the unrounded value is generated.
- Overflow (O):
  When rounding mode = RZ, the maximum normalized number, with the same sign as the unrounded value, is generated.
  When rounding mode = RN, infinity with the same sign as the unrounded value is generated.
- Underflow (U):
  Zero with the same sign as the unrounded value is generated.
- Inexact exception (I): An inexact result is generated.

Clock Operating Mode	FRQCR Setting	PLL Frequency Multiplier: PLL Circuit 1	PLL Frequency Multiplier: PLL Circuit 2	Ratio of Internal Clock Frequencies (I:B:P)*1	Selectable Frequency Range (MHz): Input Clock*2	Output Clock (CKIO Pin)*3	CPU Clock (Iϕ)*3	Bus Clock (Bϕ)*3	Peripheral Clock (Pϕ)*3
2	H'1226	ON (×3)	ON (×2)	2:2:1/2	10 to 20	20 to 40	20 to 40	20 to 40	5 to 10
	H'1303	ON (×4)	ON (×2)	8:2:2	10 to 15	20 to 30	80 to 120	20 to 30	20 to 30
	H'1305	ON (×4)	ON (×2)	8:2:1	10 to 15	20 to 30	80 to 120	20 to 30	10 to 15
	H'1306	ON (×4)	ON (×2)	8:2:2/3	10 to 15	20 to 30	80 to 120	20 to 30	6.67 to 10
	H'1313	ON (×4)	ON (×2)	4:2:2	10 to 20	20 to 40	40 to 80	20 to 40	20 to 40
	H'1315	ON (×4)	ON (×2)	4:2:1	10 to 25	20 to 50	40 to 100	20 to 50	10 to 25
	H'1316	ON (×4)	ON (×2)	4:2:2/3	10 to 25	20 to 50	40 to 100	20 to 50	6.67 to 16.67
	H'1333	ON (×4)	ON (×2)	2:2:2	10 to 20	20 to 40	20 to 40	20 to 40	20 to 40
	H'1335	ON (×4)	ON (×2)	2:2:1	10 to 25	20 to 50	20 to 50	20 to 50	10 to 25
	H'1336	ON (×4)	ON (×2)	2:2:2/3	10 to 25	20 to 50	20 to 50	20 to 50	6.67 to 16.67
	H'1404	ON (×6)	ON (×2)	12:2:2	10	20	120	20	20
	H'1406	ON (×6)	ON (×2)	12:2:1	10	20	120	20	10
	H'1414	ON (×6)	ON (×2)	6:2:2	10 to 16.67	20 to 33.33	60 to 100	20 to 33.33	20 to 33.33
	H'1416	ON (×6)	ON (×2)	6:2:1	10 to 16.67	20 to 33.33	60 to 100	20 to 33.33	10 to 16.67
	H'1424	ON (×6)	ON (×2)	4:2:2	10 to 16.67	20 to 33.33	40 to 66.67	20 to 33.33	20 to 33.33
	H'1426	ON (×6)	ON (×2)	4:2:1	10 to 16.67	20 to 33.33	40 to 66.67	20 to 33.33	10 to 16.67
	H'1444	ON (×6)	ON (×2)	2:2:2	10 to 16.67	20 to 33.33	20 to 33.33	20 to 33.33	20 to 33.33
	H'1446	ON (×6)	ON (×2)	2:2:1	10 to 16.67	20 to 33.33	20 to 33.33	20 to 33.33	10 to 16.67
	H'1515	ON (×8)	ON (×2)	8:2:2	10 to 12.5	20 to 25	80 to 100	20 to 25	20 to 25
	H'1535	ON (×8)	ON (×2)	4:2:2	10 to 12.5	20 to 25	40 to 50	20 to 25	20 to 25
	H'1555	ON (×8)	ON (×2)	2:2:2	10 to 12.5	20 to 25	20 to 25	20 to 25	20 to 25
3	H'1000	ON (×1)	OFF	1:1:1	20 to 40	—	20 to 40	20 to 40	20 to 40
	H'1001	ON (×1)	OFF	1:1:1/2	20 to 60	—	20 to 60	20 to 60	10 to 30
	H'1002	ON (×1)	OFF	1:1:1/3	20 to 60	—	20 to 60	20 to 60	6.67 to 20
	H'1003	ON (×1)	OFF	1:1:1/4	20 to 60	—	20 to 60	20 to 60	5 to 15
	H'1004	ON (×1)	OFF	1:1:1/6	20 to 60	—	20 to 60	20 to 60	3.33 to 10
	H'1005	ON (×1)	OFF	1:1:1/8	20 to 60	—	20 to 60	20 to 60	2.5 to 7.5
	H'1006	ON (×1)	OFF	1:1:1/12	20 to 60	—	20 to 60	20 to 60	1.67 to 5

5.2.4 Manual Reset

(1) Manual Reset by Means of $\overline{\text{MRES}}$ Pin

When the $\overline{\text{MRES}}$ pin is driven low, this LSI enters the manual reset state. To reset this LSI without fail, the $\overline{\text{MRES}}$ pin should be kept at the low level for at least 20-tcyc. In the manual reset state, the CPU's internal state is initialized, but all the on-chip peripheral module registers are not initialized. In the manual reset state, manual reset exception handling starts when the $\overline{\text{MRES}}$ pin is first driven low for a fixed period and then returned to high. The CPU operates as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from the exception handling vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception handling vector table.
3. The vector base register (VBR) is cleared to H'00000000, the interrupt mask level bits (I3 to I0) of the status register (SR) are initialized to H'F (B'1111), and the BO and CS bits are initialized. The BN bit in IBNR of the INTC is also initialized to 0.
4. The values fetched from the exception handling vector table are set in the PC and SP, and the program begins executing.

(2) Manual Reset Initiated by WDT

When a setting is made for a manual reset to be generated in the WDT's watchdog timer mode, and WTCNT of the WDT overflows, this LSI enters the manual reset state.

When manual reset exception processing is started by the WDT, the CPU operates in the same way as when a manual reset was caused by the $\overline{\text{MRES}}$ pin.

(3) Notes at a Manual Reset

When a manual reset is generated, the bus cycle is retained. Thus, manual reset exception handling will be deferred until the CPU acquires the bus mastership. The CPU and the BN bit in IBNR of the INTC are initialized by a manual reset. The FPU and other modules are not initialized.

5.10 Usage Notes

5.10.1 Value of Stack Pointer (SP)

The value of the stack pointer must always be a multiple of four. If it is not, an address error will occur when the stack is accessed during exception handling.

5.10.2 Value of Vector Base Register (VBR)

The value of the vector base register must always be a multiple of four. If it is not, an address error will occur when the stack is accessed during exception handling.

5.10.3 Address Errors Caused by Stacking of Address Error Exception Handling

When the stack pointer is not a multiple of four, an address error will occur during stacking of the exception handling (interrupts, etc.) and address error exception handling will start up as soon as the first exception handling is ended. Address errors will then also occur in the stacking for this address error exception handling. To ensure that address error exception handling does not go into an endless loop, no address errors are accepted at that point. This allows program control to be shifted to the address error exception service routine and enables error processing.

When an address error occurs during exception handling stacking, the stacking bus cycle (write) is executed. During the stacking of the status register (SR) and program counter (PC), the SP is decremented by 4 for both, so the value of SP will not be a multiple of four after the stacking either. The address value output during stacking is the SP value, so the address where the error occurred is itself output. This means the write data stacked will be undefined.

Interrupt Source			Interrupt Vector: Vector	Interrupt Vector: Vector Table Address Offset	Interrupt Priority (Initial Value)	Corresponding IPR (Bit)	IPR Setting Unit: Internal Priority	IPR Setting Unit: Default Priority
MTU2	MTU3	TGI3A	132	H'00000210 to H'00000213	0 to 15 (0)	IPR07 (3 to 0)	1	High
		TGI3B	133	H'00000214 to H'00000217			2	
		TGI3C	134	H'00000218 to H'0000021B			3	
		TGI3D	135	H'0000021C to H'0000021F			4	
		TCI3V	136	H'00000220 to H'00000223	0 to 15 (0)	IPR08 (15 to 12)	—	
	MTU4	TGI4A	140	H'00000230 to H'00000233	0 to 15 (0)	IPR08 (11 to 8)	1	
		TGI4B	141	H'00000234 to H'00000237			2	
		TGI4C	142	H'00000238 to H'0000023B			3	
		TGI4D	143	H'0000023C to H'0000023F			4	
		TCI4V	144	H'00000240 to H'00000243	0 to 15 (0)	IPR08 (7 to 4)	—	
	MTU5	TGI5U	148	H'00000250 to H'00000253	0 to 15 (0)	IPR08 (3 to 0)	1	
		TGI5V	149	H'00000254 to H'00000257			2	
		TGI5W	150	H'00000258 to H'0000025B			3	
RTC	ARM		152	H'00000260 to H'00000263	0 to 15 (0)	IPR09 (15 to 12)	1	
	PRD		153	H'00000264 to H'00000267			2	
	CUP		154	H'00000268 to H'0000026B			3	Low

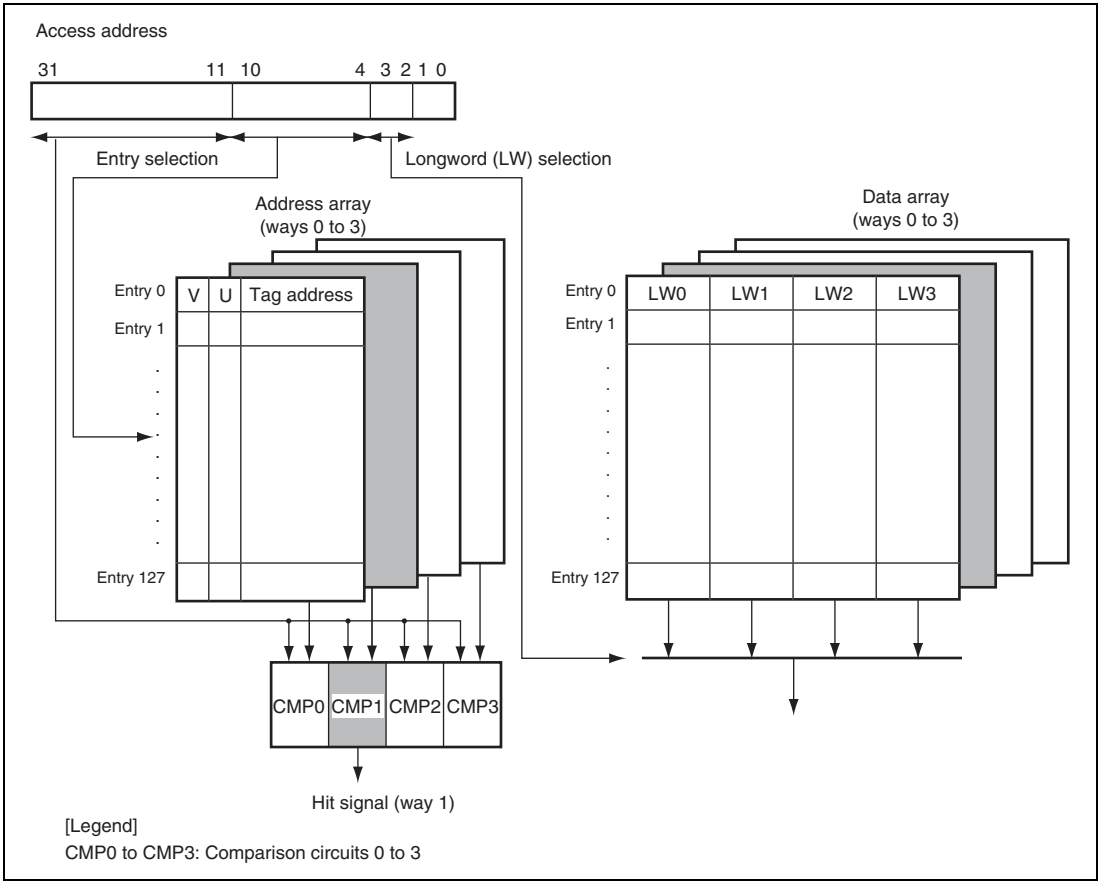

Figure 8.2 Cache Search Scheme

Bit	Bit Name	Initial Value	R/W	Description
18 to 16	SZSEL[2:0]	Undefined	R/W	Transfer Data Size Selection These bits are used to specify the number of bits transferred in each single data transfer. The unit for transfer can be selected as byte (8 bit), word (16 bit), or longword (32 bit). For details, see section 11.9, Units of Transfer and Positioning of Bytes for Transfer. Set the transfer size so that it doesn't exceed the widths of the data buses supported by the source and destination for DMA transfer. The bus widths of the data buses are fixed by hardware. 000: Byte (8 bits) 001: Word (16 bits) 010: Longword (32 bits) 011 to 111: Setting prohibited
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	SAMOD [2:0]	Undefined	R/W	Source Address Direction Control These bits are used to specify the direction of counting for the source address. 000: Fixed 001: Incrementation 010: Decrementation 011: Rotation 100 to 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	DAMOD [2:0]	Undefined	R/W	Destination Address Direction Control These bits are used to specify the direction of counting for the source address. 000: Fixed 001: Incrementation 010: Decrementation 011: Rotation 100 to 111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
17, 16	STRG[1:0]	00	R/W	Input Sense Mode Selection These bits specify input sense modes for DMA request signals input to the DMAC. The requesting source is that selected from among the possible sources by the DMA request source selection bits (DCTG). Select rising edge sense by setting these bits to "00" if the software trigger (DCTG = "000000") and pins DREQ0 to DREQ3 are selected as the source for DMA requests. Select falling edge sense by setting the bits to "10" when operation is with IIC3, SCIF, SSI, RCAN-ET, MTU2, or ADC (DCTG = "000101" to "100100"). Table 11.4 shows the relationships between DMA request sources and the possible input sense modes. 00: Rising edge 01: High level 10: Falling edge 11: Low level
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	BRLOD	0	R/W	DMA Byte Count Reload Function Enable This bit specifies whether to reload the byte counter or not when the DMA transfer end condition is detected. When this bit is cleared to "0", no reload is executed. When this bit is set to "1" and the DMA transfer end condition is detected, the DMA current byte counter register (DMCBCTn) is reloaded with the value in the DMA reload byte count register (DMRBCTn). 0: Byte count reload function disabled 1: Byte count reload function enabled

11.7.3 Sense Mode for DMA Requests

When pins DREQ0 to DREQ3 (DCTG = "000001" to "000100") are specified by the DMA request source selection bits (DTCG), either level sense or edge sense might be required. Make the appropriate setting ("01" or "11" for level sense and "00" or "10" for edge sense) in the input sense selection bits (STRG) of DMA control register A (DMCNTAn).

When the software trigger (DCTG = "000000") is selected as a DMA request source, set these bits to "00" to select the rising-edge sense. When IIC3, SCIF, SSI, RCAN-ET, MTU2, or ADC (DCTG = "000101" to "100101") is selected, set the bits to "10" to select the falling-edge sense. Table 11.4 shows the relationships between the DMA request sources and input sense mode.

Below are further details on level- and edge-sense operation.

(1) Level Sense

When a level sense is specified (STRG = "01" or "11"), one level of the DMA request signal indicates the DMA request. Since DMA requests detected in this way are not retained in the DMAC, maintain the requesting level until acceptance of the DMA request has been confirmed.

Figure 11.7 is an example of DMA request reception processing when a level sense has been selected.

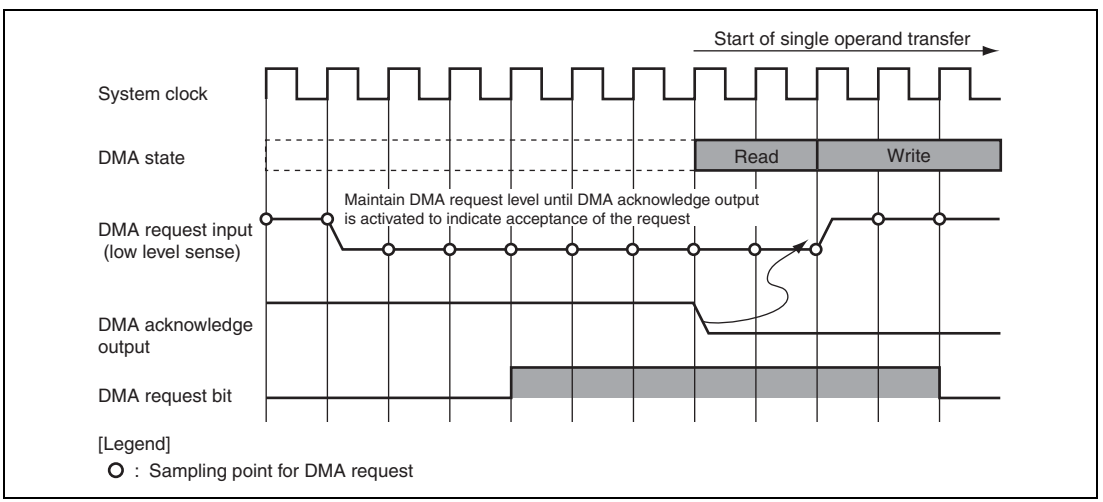

Figure 11.7 Example of DMA Request Reception Processing for a Level Sense

When a level sense has been selected, DMA request bit for the channel is masked over the period from the start of the last write access of single operand transfer until four clock pulses (system

- TIER_5

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TGIE5U	0	R/W	TGR Interrupt Enable 5U Enables or disables interrupt requests (TGIU_5) by compare match between TCNTU_5 and TGRU_5. 0: Interrupt requests (TGIU_5) disabled 1: Interrupt requests (TGIU_5) enabled
1	TGIE5V	0	R/W	TGR Interrupt Enable 5V Enables or disables interrupt requests (TGIV_5) by compare match between TCNTV_5 and TGRV_5. 0: Interrupt requests (TGIV_5) disabled 1: Interrupt requests (TGIV_5) enabled
0	TGIE5W	0	R/W	TGR Interrupt Enable 5W Enables or disables interrupt requests (TGIW_5) by compare match between TCNTW_5 and TGRW_5. 0: Interrupt requests (TGIW_5) disabled 1: Interrupt requests (TGIW_5) enabled

Bit	Bit Name	Initial Value	R/W	Description
4	TCFV	0	R/(W)*1	Overflow Flag Status flag that indicates that TCNT overflow has occurred. Only 0 can be written, for flag clearing. [Setting condition] • When the TCNT value overflows (changes from H'FFFF to H'0000) In channel 4, when the TCNT_4 value underflows (changes from H'0001 to H'0000) in complementary PWM mode, this flag is also set. [Clearing condition] • When 0 is written to TCFV after reading TCFV = 1*2
3	TGFD	0	R/(W)*1	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channels 0, 3, and 4. Only 0 can be written, for flag clearing. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and the write value should always be 0. [Setting conditions] • When TCNT = TGRD and TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal and TGRD is functioning as input capture register [Clearing condition] • When 0 is written to TGFD after reading TGFD = 1*2

Bit	Bit Name	Initial Value	R/W	Description
13 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	UT4AE	0	R/W	Up-Count TRG4AN Enable Enables or disables A/D converter start requests (TRG4AN) during TCNT_4 up-count operation. 0: A/D converter start requests (TRG4AN) disabled during TCNT_4 up-count operation 1: A/D converter start requests (TRG4AN) enabled during TCNT_4 up-count operation
6	DT4AE	0*	R/W	Down-Count TRG4AN Enable Enables or disables A/D converter start requests (TRG4AN) during TCNT_4 down-count operation. 0: A/D converter start requests (TRG4AN) disabled during TCNT_4 down-count operation 1: A/D converter start requests (TRG4AN) enabled during TCNT_4 down-count operation
5	UT4BE	0	R/W	Up-Count TRG4BN Enable Enables or disables A/D converter start requests (TRG4BN) during TCNT_4 up-count operation. 0: A/D converter start requests (TRG4BN) disabled during TCNT_4 up-count operation 1: A/D converter start requests (TRG4BN) enabled during TCNT_4 up-count operation
4	DT4BE	0*	R/W	Down-Count TRG4BN Enable Enables or disables A/D converter start requests (TRG4BN) during TCNT_4 down-count operation. 0: A/D converter start requests (TRG4BN) disabled during TCNT_4 down-count operation 1: A/D converter start requests (TRG4BN) enabled during TCNT_4 down-count operation
3	ITA3AE	0*	R/W	TGIA_3 Interrupt Skipping Link Enable Select whether to link A/D converter start requests (TRG4AN) with TGIA_3 interrupt skipping operation. 0: Does not link with TGIA_3 interrupt skipping 1: Links with TGIA_3 interrupt skipping

12.4 Operation

12.4.1 Basic Functions

Each channel has a TCNT and TGR register. TCNT performs up-counting, and is also capable of free-running operation, cycle counting, and external event counting.

Each TGR can be used as an input capture register or output compare register.

Always select MTU2 external pins set function using the pin function controller (PFC).

(1) Counter Operation

When one of bits CST0 to CST4 in TSTR or bits CSTU5, CSTV5, and CSTW5 in TSTR_5 is set to 1, the TCNT counter for the corresponding channel begins counting. TCNT can operate as a free-running counter, periodic counter, for example.

(a) Example of Count Operation Setting Procedure

Figure 12.4 shows an example of the count operation setting procedure.

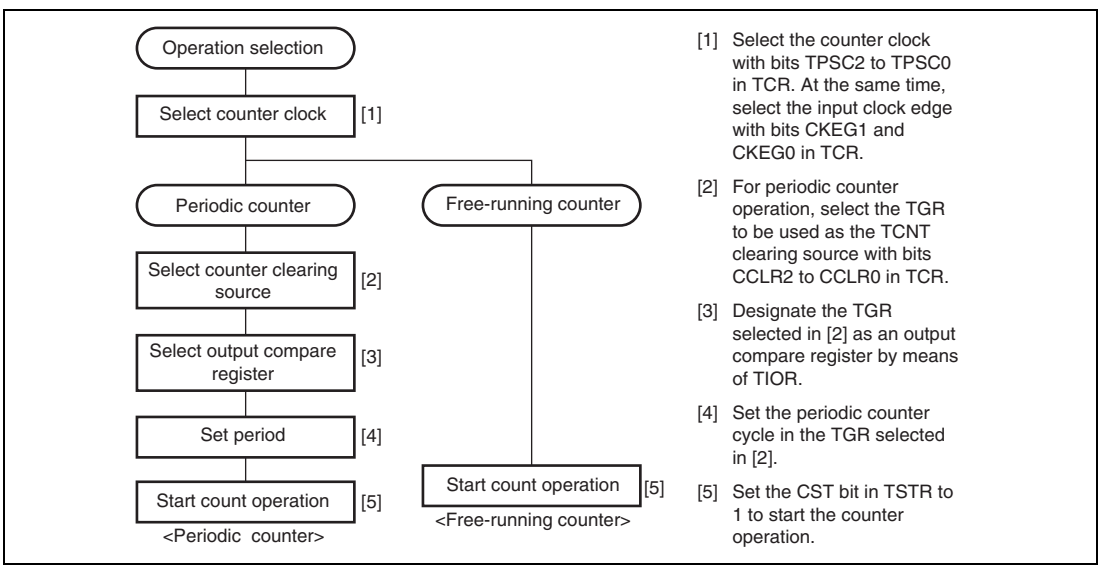

Figure 12.4 Example of Counter Operation Setting Procedure

(7) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Normal Mode

Figure 12.133 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in normal mode after re-setting.

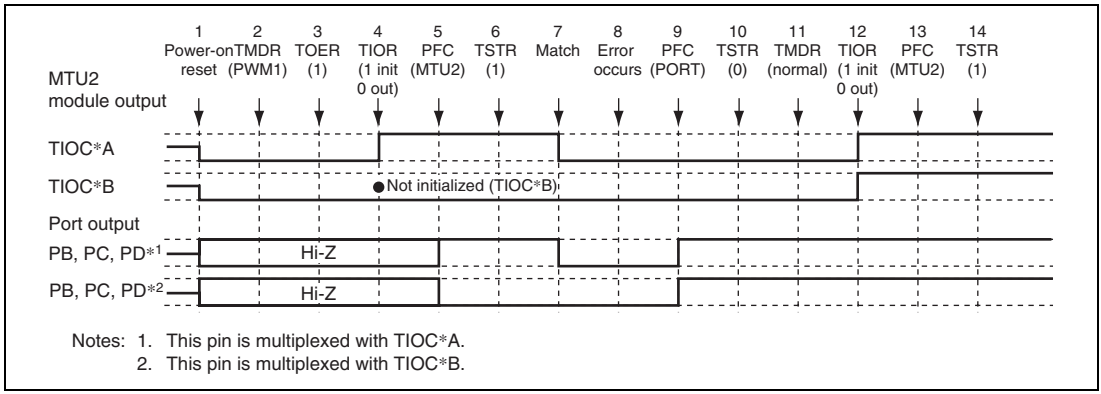

Figure 12.133 Error Occurrence in PWM Mode 1, Recovery in Normal Mode

1. After a power-on reset, MTU2 output is low and ports are in the high-impedance state.
2. Set PWM mode 1.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TIOR.
4. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence. In PWM mode 1, the TIOC*B side is not initialized.)
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Set normal mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

19.1.4 References

1. CAN License Specification, Robert Bosch GmbH, 1992
2. CAN Specification Version 2.0 part A, Robert Bosch GmbH, 1991
3. CAN Specification Version 2.0 part B, Robert Bosch GmbH, 1991
4. Implementation Guide for the CAN Protocol, CAN Specification 2.0 Addendum, CAN In Automation, Erlangen, Germany, 1997
5. Road vehicles - Controller area network (CAN): Part 1: Data link layer and physical signalling (ISO-11898-1, 2002)

19.1.5 Features

- Supports CAN specification 2.0B
- Bit timing compliant with ISO-11898-1
- 16 Mailbox version
- Clock 16 to 40 MHz
- 15 programmable Mailboxes for transmit/receive + 1 receive-only mailbox
- Sleep mode for low power consumption and automatic recovery from sleep mode by detecting CAN bus activity
- Programmable receive filter mask (standard and extended identifier) supported by all Mailboxes
- Programmable CAN data rate up to 1MBit/s
- Transmit message queuing with internal priority sorting mechanism against the problem of priority inversion for real-time applications
- Data buffer access without SW handshake requirement in reception
- Flexible micro-controller interface
- Flexible interrupt structure

Bit 0 — Bit Sample Point (BSP = BCR1[0]): Sets the point at which data is sampled. Three-time sampling is only available when the BRP is programmed to be greater than 4.

Bit 0: BSP	Description
0	Bit sampling at one point (end of time segment 1) (Initial value)
1	Bit sampling at three points (rising edge of the last three clock cycles of PHSEG1)

- BCR0 (Address = H'006)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BRP[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 8 to 15 : Reserved. The written value should always be '0' and the returned value is '0'.

Bits 7 to 0—Baud Rate Pre-scale (BRP[7:0] = BCR0 [7:0]): These bits are used to define the peripheral clock periods contained in a Time Quantum.

Bit 7: BRP[7]	Bit 6: BRP[6]	Bit 5: BRP[5]	Bit 4: BRP[4]	Bit 3: BRP[3]	Bit 2: BRP[2]	Bit 1: BRP[1]	Bit 0: BRP[0]	Description
0	0	0	0	0	0	0	0	2 × peripheral clock (Initial value)
0	0	0	0	0	0	0	1	4 × peripheral clock
0	0	0	0	0	0	1	0	6 × peripheral clock
: :	: :	: :	: :	: :	: :	: :	: :	2 × (register value+1) × peripheral clock
1	1	1	1	1	1	1	1	512 × peripheral clock

20.2 Input/Output Pins

Table 20.1 summarizes the A/D converter's input pins.

Table 20.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Analog power supply pin	AVcc	Input	Analog power supply pin
Analog ground pin	AVss	Input	Analog ground pin and A/D conversion reference ground
Reference power supply pin	AVref	Input	A/D converter reference voltage pin
Analog input pin 0	AN0	Input	Analog input
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger input to start A/D conversion

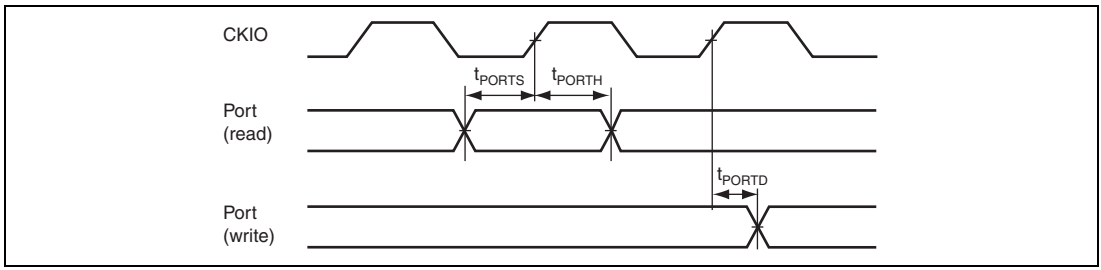

Figure 29.42 I/O Port Timing

29.3.15 H-UDI-Related Pin Timing

Table 29.19 H-UDI-Related Pin Timing

Conditions: $PV_{CC} = V_{CC}R = PLLV_{CC} = 3.0$ V to 3.6 V, $AV_{CC} = 3.0$ V to 3.6 V,
$PV_{CC} - 0.3$ V $\leq AV_{CC} \leq PV_{CC}$, $AV_{ref} = 3.0$ V to AV_{CC},
$PV_{SS} = V_{SS}R = PLLV_{SS} = AV_{SS} = 0$ V

Item	Symbol	Min.	Max.	Unit	Figure
UDTCK cycle time	t_{TCKcyc}	50*	—	ns	Figure 29.43
UDTCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
UDTCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
$\overline{\text{UDTRST}}$ pulse width	t_{TRSW}	20	—	t_{TCKcyc}	Figure 29.44
$\overline{\text{UDTRST}}$ setup time	t_{TRSS}	200	—	ns	
UDTDI setup time	t_{TDIS}	10	—	ns	Figure 29.45
UDTDI hold time	t_{TDIH}	10	—	ns	
UDTMS setup time	t_{TMSS}	10	—	ns	
UDTMS hold time	t_{TMSH}	10	—	ns	
UDTDO delay time	t_{TDOD}	—	16	ns	

Note: * Should be greater than the peripheral clock (Pϕ) cycle time.