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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	42-SDIP (0.600", 15.24mm)
Supplier Device Package	42-PDIP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc705c8ab

MC68HC705C8A
MC68HSC705C8A

Technical Data

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

List of Figures

CME — Clock Monitor Enable Bit

This read/write bit enables the clock monitor. The clock monitor sets the COPF bit and generates a reset if it detects an absent internal clock for a period of from 5 µs to 100 µs. CME is readable and writable at any time. Reset clears the CME bit.

1 = Clock monitor enabled
0 = Clock monitor disabled

NOTE: *Do not enable the clock monitor in applications with an internal clock frequency of 200 kHz or less.*

If the clock monitor detects a slow clock, it drives the bidirectional $\overline{\text{RESET}}$ pin low for four clock cycles. If the clock monitor detects an absent clock, it drives the $\overline{\text{RESET}}$ pin low until the clock recovers.

PCOPE — Programmable COP Enable Bit

This read/write bit enables the programmable COP watchdog. PCOPE is readable at any time but can be written only once after reset. Reset clears the PCOPE bit.

1 = Programmable COP watchdog enabled
0 = Programmable COP watchdog disabled

NOTE: *Programming the non-programmable COP enable bit (NCOPE) in mask option register 2 (MOR2) to logic 1 enables the non-programmable COP watchdog. Setting the PCOPE bit while the NCOPE bit is programmed to logic 1 enables both COP watchdogs to operate at the same time. (See **9.5.3 Mask Option Register 2**.)*

CM1 and CM0 — COP Mode Bits

These read/write bits select the timeout period of the programmable COP watchdog. (See **Table 5-1**.) CM1 and CM0 can be read anytime but can be written only once. They can be cleared only by reset.

Bits 7–5 — Unused

Bits 7–5 always read as logic 0s. Reset clears bits 7–5.

6.3.4 Non-Programmable COP Watchdog in Stop Mode

The STOP instruction has these effects on the non-programmable COP watchdog:

- Turns off the oscillator and the COP watchdog counter
- Clears the COP watchdog counter

If the $\overline{\text{RESET}}$ pin brings the MCU out of stop mode, the COP watchdog begins counting immediately. The reset function clears the COP counter again after the 4064-t_{CYC} clock stabilization delay.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of stop mode, the COP watchdog begins counting immediately. The IRQ function does not clear the COP counter again after the 4064-t_{CYC} clock stabilization delay. See **Figure 6-3**.

NOTE: *If the clock monitor is enabled (CME = 1), the STOP instruction causes it to time out and reset the MCU.*

6.4 Wait Mode

The WAIT instruction places the MCU in an intermediate power consumption mode. All central processor unit (CPU) activity is suspended, but the oscillator, capture/compare timer, SCI, and SPI remain active. Any interrupt or reset brings the MCU out of wait mode. See **Figure 6-1**.

The WAIT instruction has these effects on the CPU:

- Clears the I bit in the condition code register, enabling interrupts
- Stops the CPU clock, but allows the internal clock to drive the capture/compare timer, SCI, and SPI

The WAIT instruction does not affect any other registers or I/O lines. The capture/compare timer, SCI, and SPI can be enabled to allow a periodic exit from wait mode.

Section 7. Parallel Input/Output (I/O)

7.1 Contents

7.2 Introduction

This section describes the programming of ports A, B, C, and D.

TOF — Timer Overflow Flag

The TOF bit is automatically set when the 16-bit counter rolls over from $FFFF to $0000. Clear the TOF bit by reading the timer status register with TOF set and then reading the low byte ($0019) of the timer registers. Reset has no effect on TOF.

1 = Timer overflow
0 = No timer overflow

Bits 4–0 — Not used; these bits always read 0

8.4.3 Timer Registers

The read-only timer registers (TRH and TRL) shown in **Figure 8-7** contain the current high and low bytes of the 16-bit counter. Reading TRH before reading TRL causes TRL to be latched until TRL is read. Reading TRL after reading the timer status register clears the timer overflow flag bit (TOF). Writing to the timer registers has no effect.

	Bit 7	6	5	4	3	2	1	Bit 0
Register Name and Address: Timer Register High — $0018								
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Reset initializes TRH to $FF							
Register Name and Address: Timer Register Low — $0019								
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Reset initializes TRL to $FC							

= Unimplemented

Figure 8-7. Timer Registers (TRH and TRL)

8.4.6 Output Compare Registers

When the value of the 16-bit counter matches the value in the read/write output compare registers (OCRH and OCRL) shown in **Figure 8-12**, the planned TCMP pin action takes place. Writing to OCRH before writing to OCRL inhibits timer compares until OCRL is written. Reading or writing to OCRL after reading the timer status register clears the output compare flag (OCF).

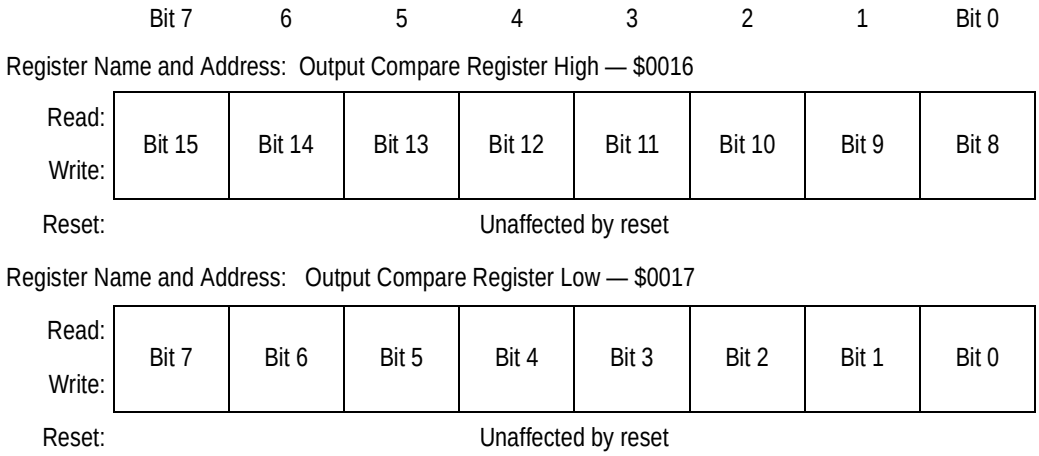


Figure 8-12. Output Compare Registers (OCRH and OCRL)

To prevent OCF from being set between the time it is read and the time the output compare registers are updated, use this procedure:

1. Disable interrupts by setting the I bit in the condition code register.
2. Write to OCRH. Compares are now inhibited until OCRL is written.
3. Clear bit OCF by reading the timer status register (TSR).
4. Enable the output compare function by writing to OCRL.
5. Enable interrupts by clearing the I bit in the condition code register.

Section 9. EPROM/OTPROM (PROM)

9.1 Contents

9.2 Introduction

This section describes erasable, programmable read-only memory/one-time programmable read-only memory (EPROM/OTPROM (PROM)) programming.

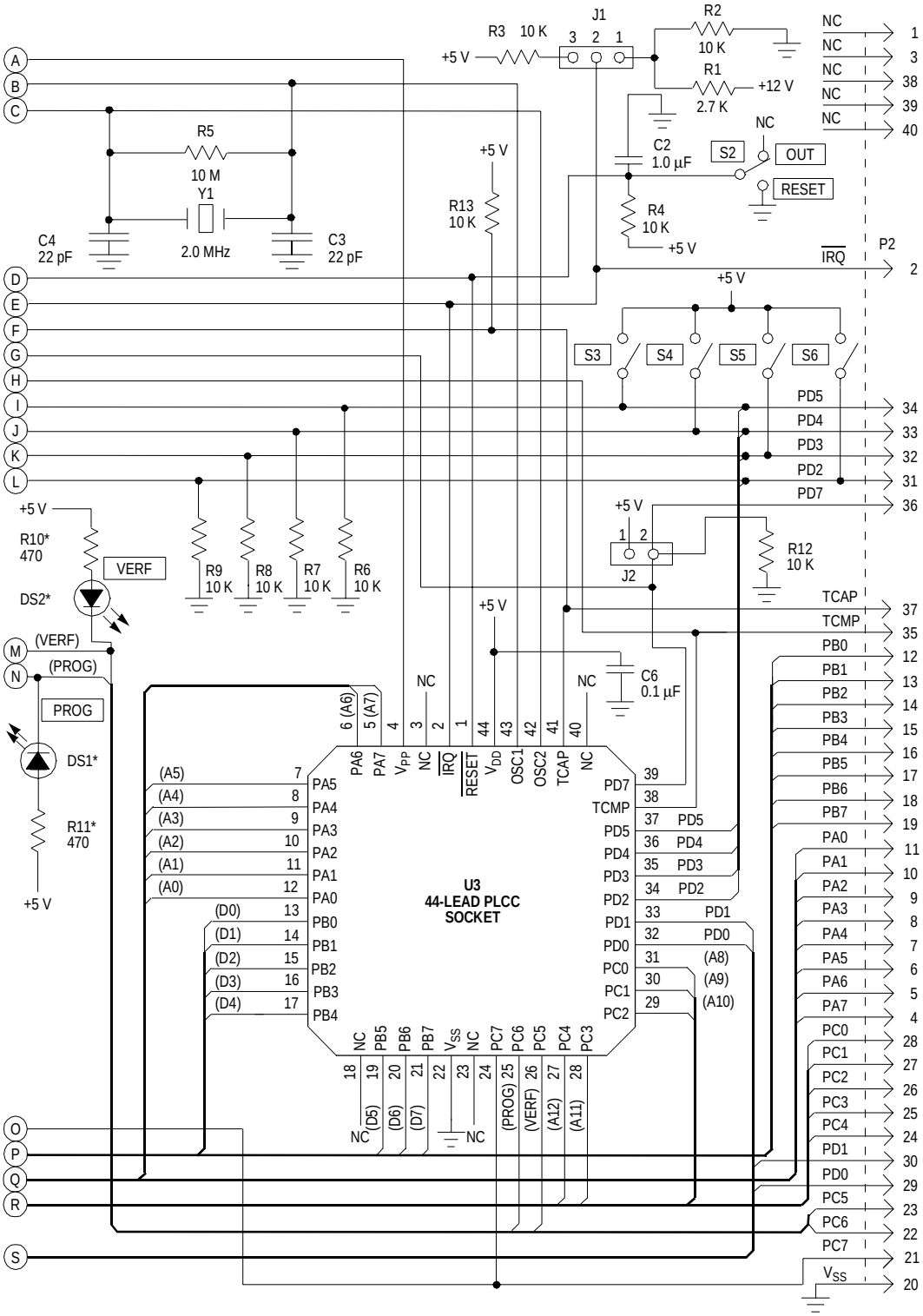


Figure 9-2. PROM Programming Circuit (Continued)

9.6 EPROM Erasing

The erased state of an EPROM or OTPROM byte is $00. EPROM devices can be erased by exposure to a high intensity ultraviolet (UV) light with a wave length of 2537 Å. The recommended erasure dosage (UV intensity on a given surface area x exposure time) is 15 Ws/cm^2. UV lamps should be used without short-wave filters, and the EPROM device should be positioned about one inch from the UV source.

OTPROM devices are shipped in an erased state. Once programmed, they cannot be erased. Electrical erasing procedures cannot be performed on either EPROM or OTPROM devices.

10.3 Features

Features of the SCI module include:

- Standard mark/space non-return-to-zero format
- Full-duplex operation
- 32 programmable baud rates
- Programmable 8-bit or 9-bit character length
- Separately enabled transmitter and receiver
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation capability with five interrupt flags:
  - Transmitter data register empty
  - Transmission complete
  - Receiver data register full
  - Receiver overrun
  - Idle receiver input
- Receiver framing error detection
- 1/16 bit-time noise detection

10.4 SCI Data Format

The SCI uses the standard non-return-to-zero mark/space data format illustrated in **Figure 10-1**.

WAKE — Wakeup Bit

This read/write bit determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received character or an idle condition of the PD0/RDI pin. Reset has no effect on the WAKE bit.

1 = Address mark wakeup
0 = Idle line wakeup

10.6.3 SCI Control Register 2

SCI control register 2 (SCCR2) shown in **Figure 10-7** has these functions:

- Enables the SCI receiver and SCI receiver interrupts
- Enables the SCI transmitter and SCI transmitter interrupts
- Enables SCI receiver idle interrupts
- Enables SCI transmission complete interrupts
- Enables SCI wakeup
- Transmits SCI break characters

Address: $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

Figure 10-7. SCI Control Register 2 (SCCR2)

TIE — Transmit Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the TDRE bit becomes set. Reset clears the TIE bit.

1 = TDRE interrupt requests enabled
0 = TDRE interrupt requests disabled

11.3 Features

Features of the SPI include:

- Full-duplex operation
- Master and slave modes
- Four programmable master mode frequencies (1.05 MHz maximum)
- 2.1-MHz maximum slave mode frequency
- Serial clock with programmable polarity and phase
- End of transmission interrupt flag
- Write collision error flag
- Bus contention error flag

Figure 11-1 shows the structure of the SPI module. **Figure 11-2** is a summary of the SPI input/output (I/O) registers.

12.3.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

12.3.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

12.3.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address.

12.3.4 Extended

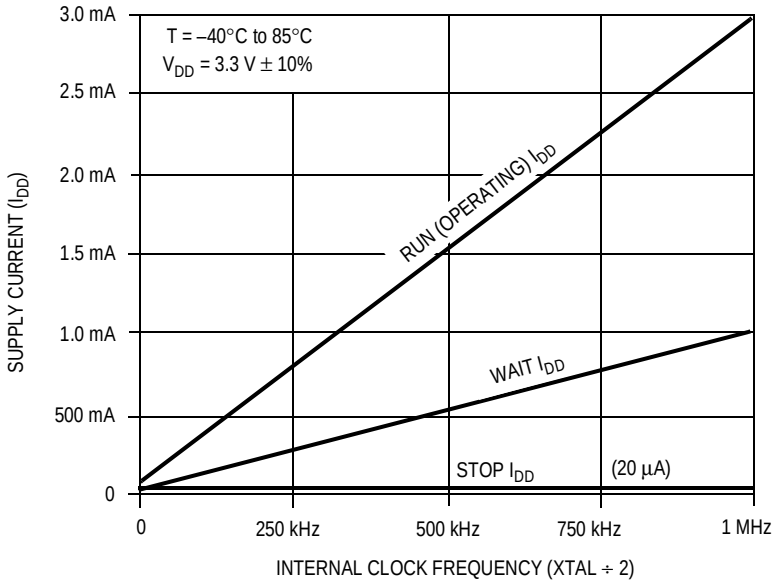
Extended instructions use three bytes and can access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Motorola assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

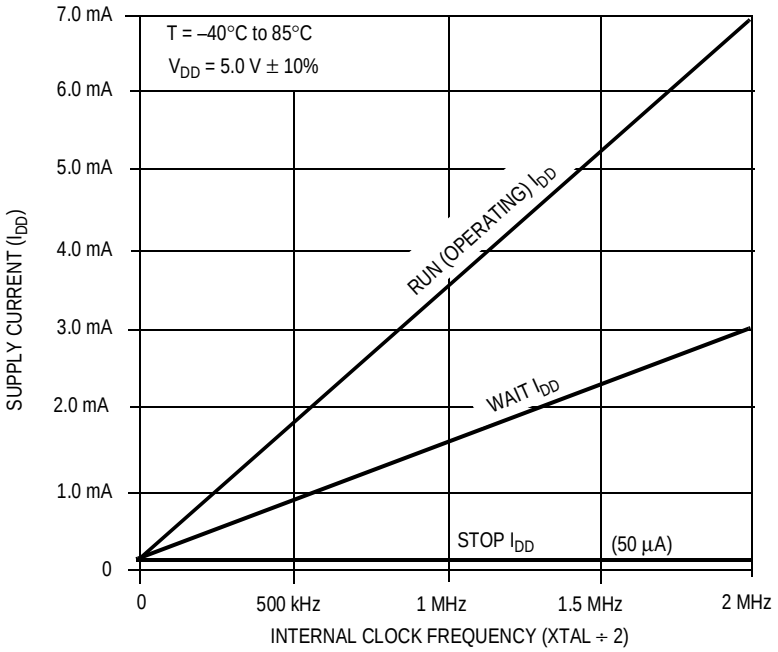
13.8 3.3-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage, $I_{Load} \leq 10.0\ \mu A$	V_{OL} V_{OH}	— $V_{DD} - 0.1$	— —	0.1 —	V
Output high voltage I_{Load} = –0.2 mA PA7–PA0, PB7–PB0, PC6–PC0, TCMP (see **Figure 13-2**) I_{Load} = –0.4 mA PD4–PD1 (see **Figure 13-3**) I_{Load} = –1.5 mA PC7	V_{OH}	$V_{DD} - 0.3$	— — —	— — —	V
Output low voltage (see **Figure 13-4**) I_{Load} = 0.4 mA PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1 I_{Load} = 6.0 mA PC7	V_{OL}	— —	— —	0.3 0.3	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSCI	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
Data-retention mode (0°C to 70°C)	V_{RM}	2.0	—	—	V
Supply current[3] Run[4] Wait[5] Stop[6]	I_{DD}	— — —	1.53 0.711 2.0	3.0 1.0 20	mA mA µA
I/O ports hi-z leakage current PA7–PA0, PB7–PB0, PC7–PC0, PD4–PD1, PD7, $\overline{RESET}$	I_{IL}	—	—	± 10	µA
Input current $\overline{IRQ}$, TCAP, OSC1, PD5, PD0	I_{In}	—	—	± 1	µA

1. V_{DD} = 3.3 V ± 10%; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only.
3. I_{DD} measured with port B pullup devices disabled.
4. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. OSC2 capacitance linearly affects run I_{DD}.
5. Wait I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects wait I_{DD}.
6. Stop I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V; $V_{IH} = V_{DD} - 0.2$ V.

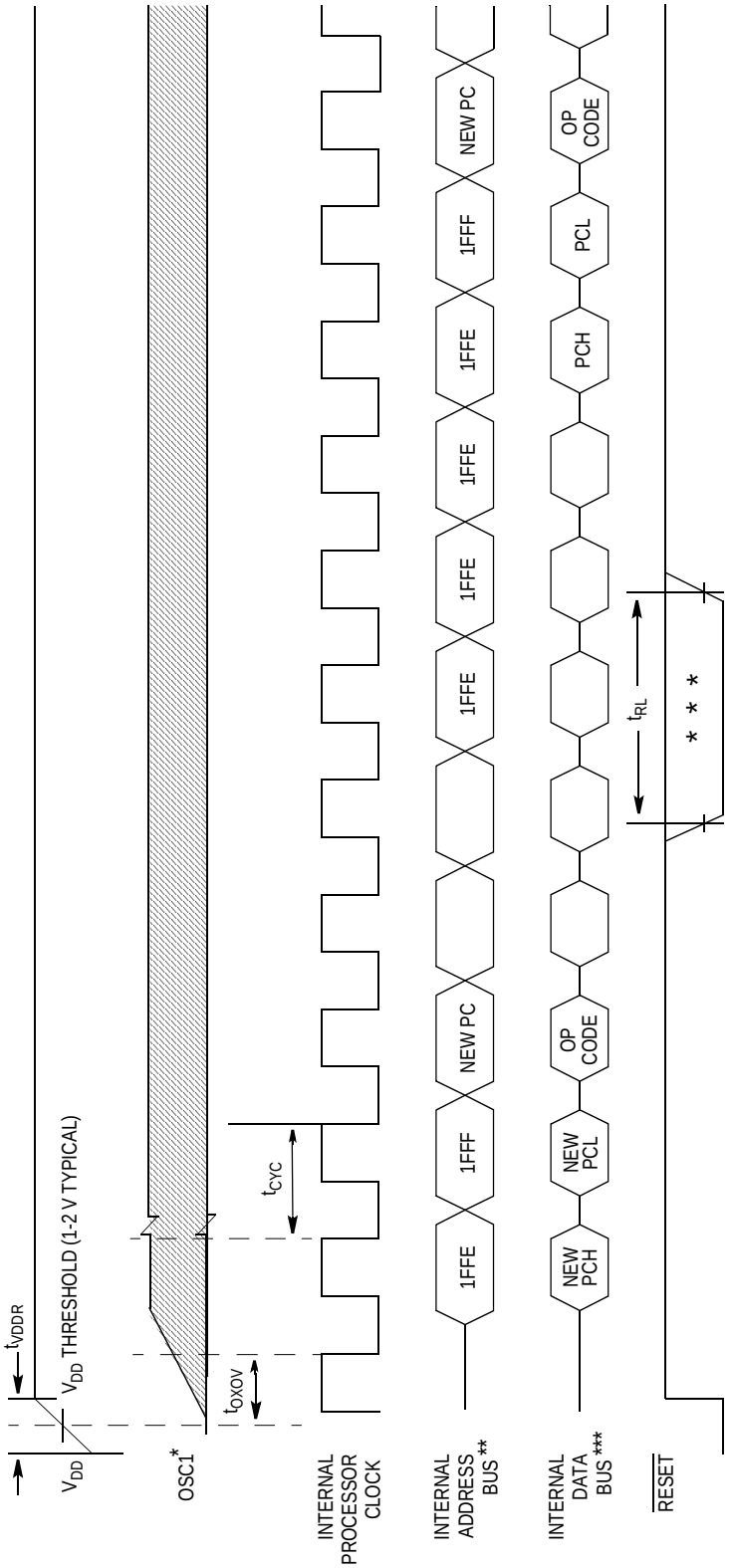


(a) Maximum Current Drain versus Frequency @ 3.3 V ± 10 %



(b) Maximum Current Drain versus Frequency @ 5 V ± 10%

Figure 13-4. Total Current Drain versus Frequency



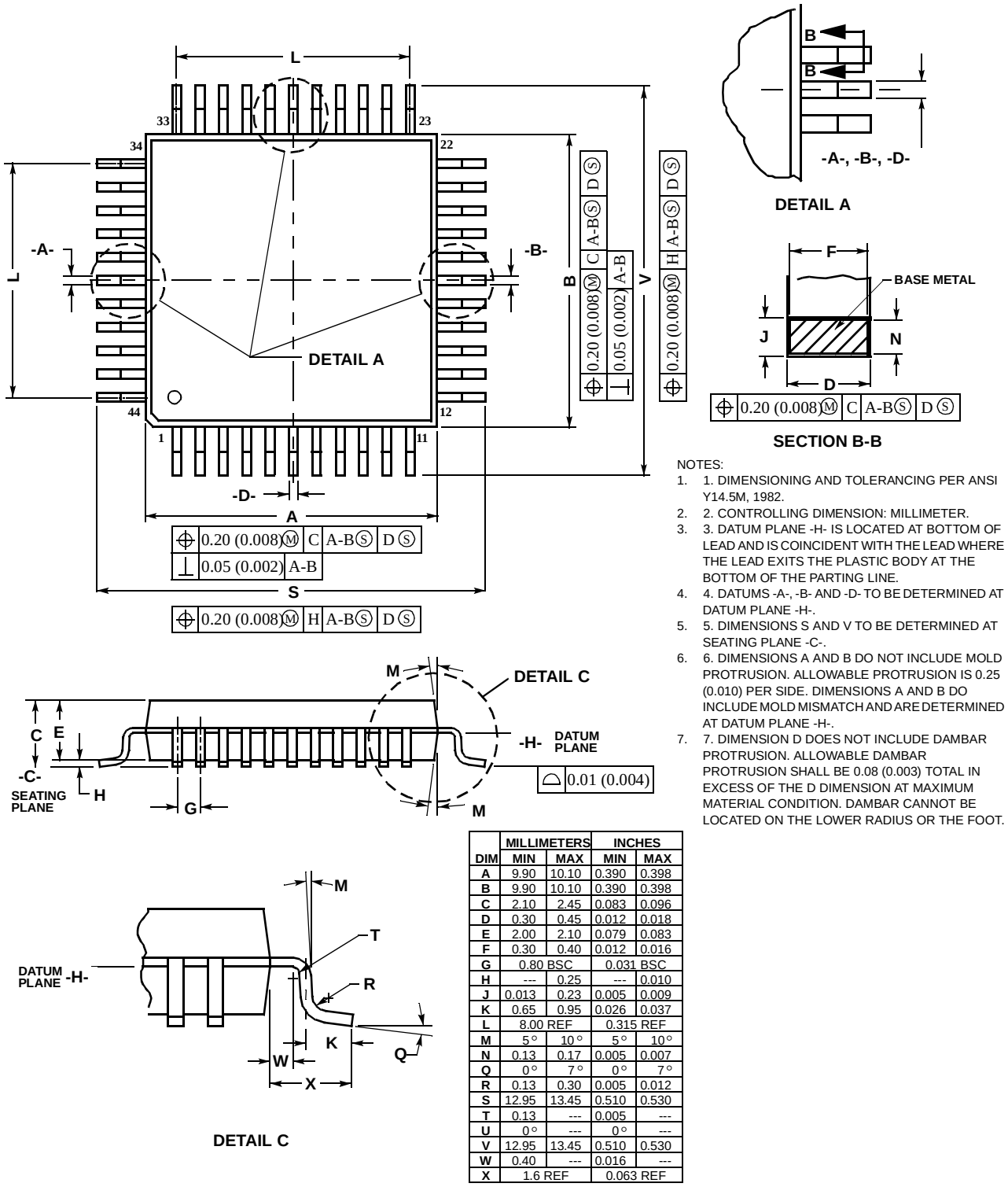
* OSC1 line is not meant to represent frequency. It is only used to represent time.

** Internal timing signal and bus information are not available externally.

***The next rising edge of the internal processor clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 13-7. Power-On Reset and External Reset Timing Diagram

14.7 44-Pin Quad Flat Pack (QFP)



NOTES:
1. 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. 2. CONTROLLING DIMENSION: MILLIMETER.
3. 3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. 4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. 5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. 6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. 7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	---	0.25	---	0.010
J	0.013	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	---	0.005	---
U	0°	---	0°	---
V	12.95	13.45	0.510	0.530
W	0.40	---	0.016	---
X	1.6 REF		0.063 REF	

Figure 14-5. MC68HC705C8AFB Package Dimensions (Case #824A)

M

O