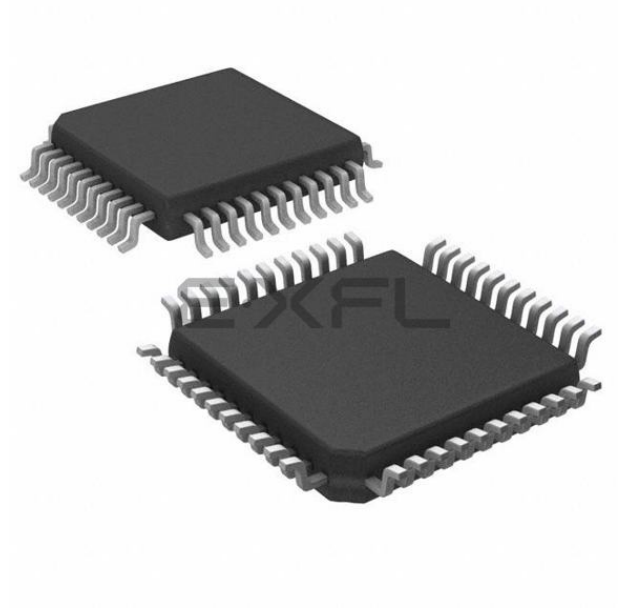

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705c8acfb

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 78.	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 81.	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Reset:	Unaffected by reset							
$0002	Port C Data Register (PORTC) See page 85.	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Unaffected by reset							
$0003	Port D Fixed Input Register (PORTD) See page 88.	Read:	PD7		SS	SCK	MOSI	MISO	TDO	RDI
		Write:								
		Reset:	Unaffected by reset							
$0004	Port A Data Direction Register (DDRA) See page 79.	Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Reset:	0	0	0	0	0	0	0	0
$0005	Port B Data Direction Register (DDRB) See page 82.	Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Reset:	0	0	0	0	0	0	0	0
$0006	Port C Data Direction (DDRC) See page 86.	Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Reset:	0	0	0	0	0	0	0	0
$0007	Unimplemented									
$0008	Unimplemented									
$0009	Unimplemented									

= Unimplemented U = Unaffected

Figure 2-2. I/O Register Summary (Sheet 1 of 4)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001C	EPROM Programming Register (PROG) See page 109.	Read:	0	0	0	0	0	LAT	0	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001D	Programmable COP Reset Register (COPRST) See page 64.	Read:								
		Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	U	U	U	U	U	U	U	U
$001E	Programmable COP Control Register (COPCR) See page 64.	Read:	0	0	0	COPF	CME	PCOPE	CM1	CM0
		Write:								
		Reset:	0	0	0	U	0	0	0	0
$001F	Unimplemented									
$1FDF	Option Register (Option) See page 116.	Read:	RAM0	RAM1	0	0	SEC*		IRQ	0
		Write:								
		Reset:	0	0	0	0	*	U	1	0
$1FF0	Mask Option Register 1 (MOR1) See page 117.	Read:	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0/ COPC
		Write:								
		Reset:	Unaffected by reset							
$1FF1	Mask Option Register 2 (MOR2) See page 118.	Read:								NCOPE
		Write:								
		Reset:	Unaffected by reset							

*Implemented as an EPROM cell

= Unimplemented U = Unaffected

Figure 2-2. I/O Register Summary (Sheet 4 of 4)

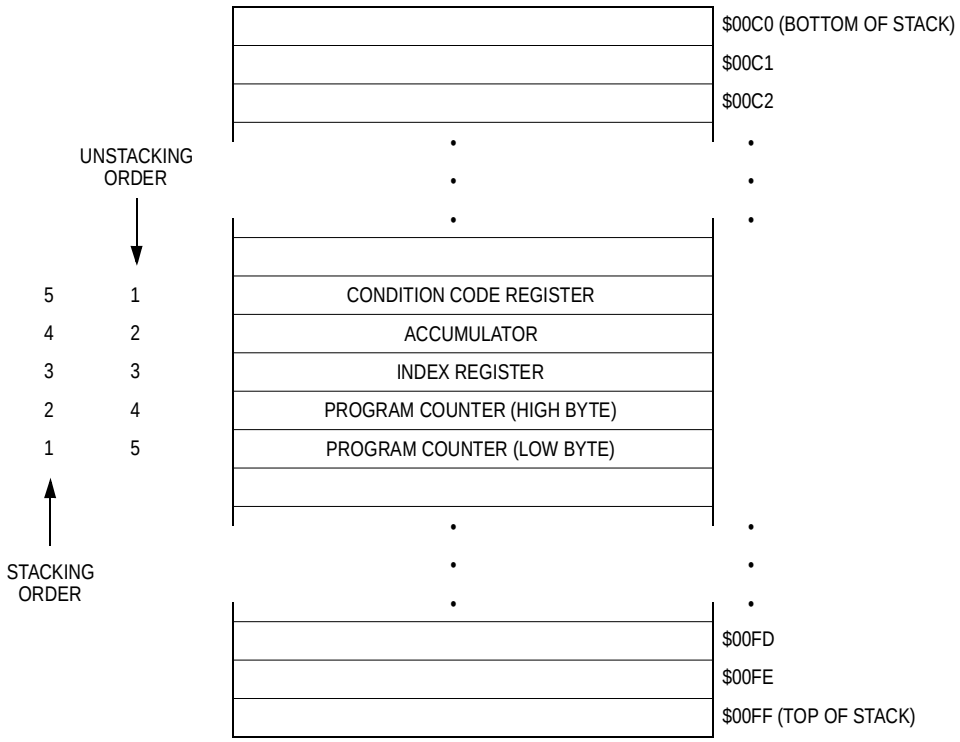

Figure 4-4. Interrupt Stacking Order

NOTE: *If more than one interrupt request is pending, the CPU fetches the vector of the higher priority interrupt first. A higher priority interrupt does not interrupt a lower priority interrupt service routine unless the lower priority interrupt service routine clears the I bit. See **Table 4-1** for a priority listing.*

Figure 4-5 shows the sequence of events caused by an interrupt.

7.3.3 Port A Logic

Figure 7-3 is a diagram of the port A I/O logic.

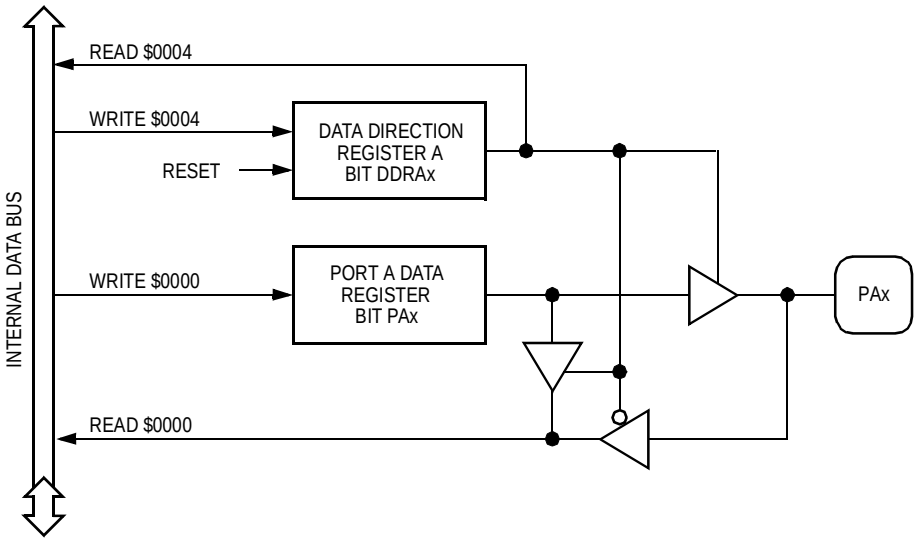

Figure 7-3. Port A I/O Logic

When a port A pin is programmed to be an output, the state of its data register bit determines the state of the output pin. When a port A pin is programmed to be an input, reading the port A data register returns the logic state of the pin.

The data latch can always be written, regardless of the state of its DDRA bit. Table 7-1 summarizes the operation of the port A pins.

Table 7-1. Port A Pin Functions

DDRA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PORTA	
		Read/Write	Read	Write
0	Input, Hi-Z(1)	DDRA7–DDRA0	Pin	PA7–PA0(2)
1	Output	DDRA7–DDRA0	PA7–PA0	PA7–PA0

1. Hi-Z = high impedance
2. Writing affects data register but does not affect input.

NOTE: *To avoid excessive current draw, tie all unused input pins to V_{DD} or V_{SS}, or change I/O pins to outputs by writing to DDRA in user code as early as possible.*

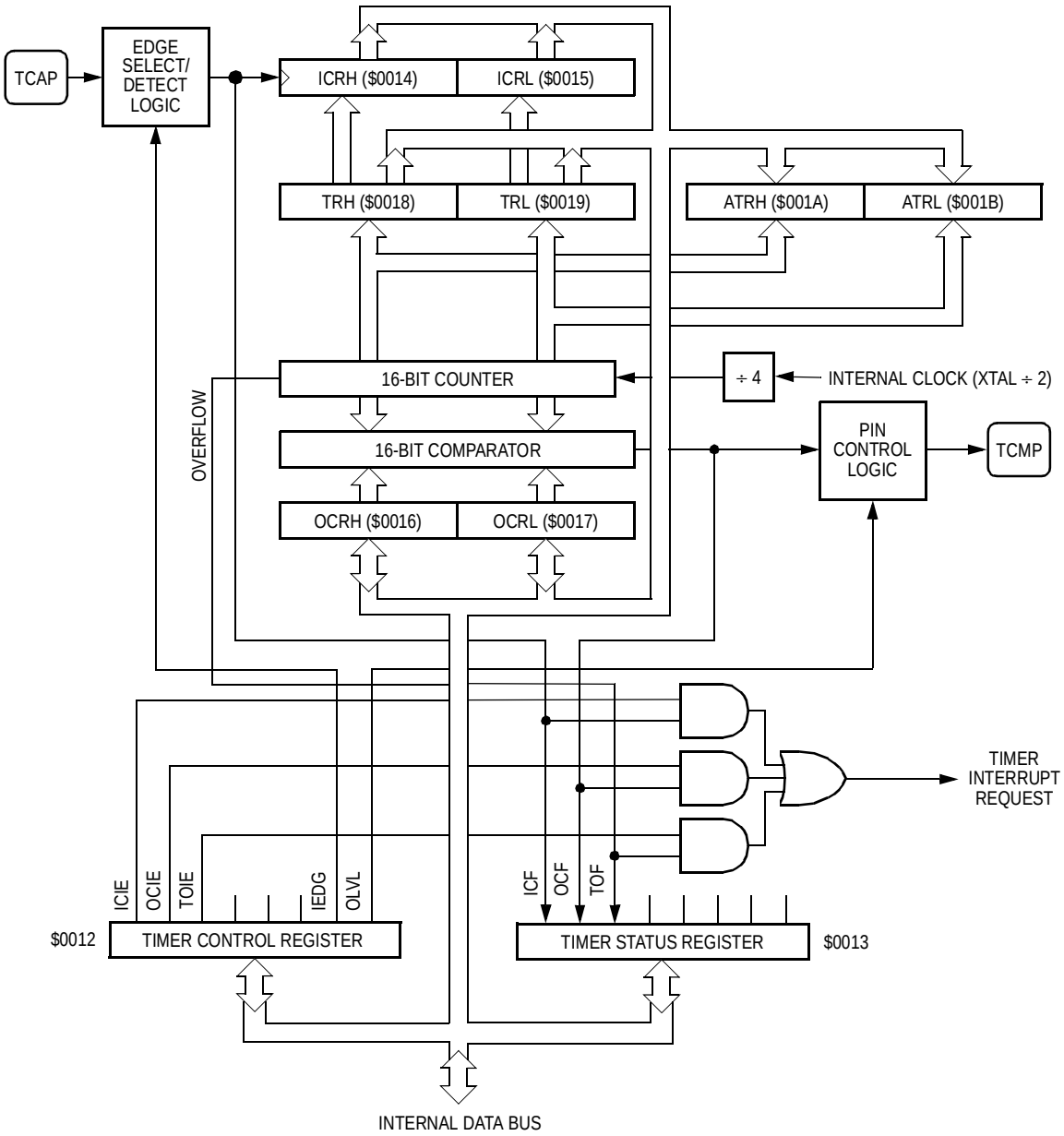

Figure 8-1. Timer Block Diagram

	Bit 7	6	5	4	3	2	1	Bit 0
Register Name and Address: Alternate Timer Register High — $001A								
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Reset initializes ATRH to $FF							
Register Name and Address: Alternate Timer Register Low — $001B								
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Reset initializes ATRL to $FC							

= Unimplemented

Figure 8-9. Alternate Timer Registers (ATRH and ATRL)

Reading ATRH returns the current value of the high byte of the counter and causes the low byte to be latched into a buffer, as shown in **Figure 8-10**.

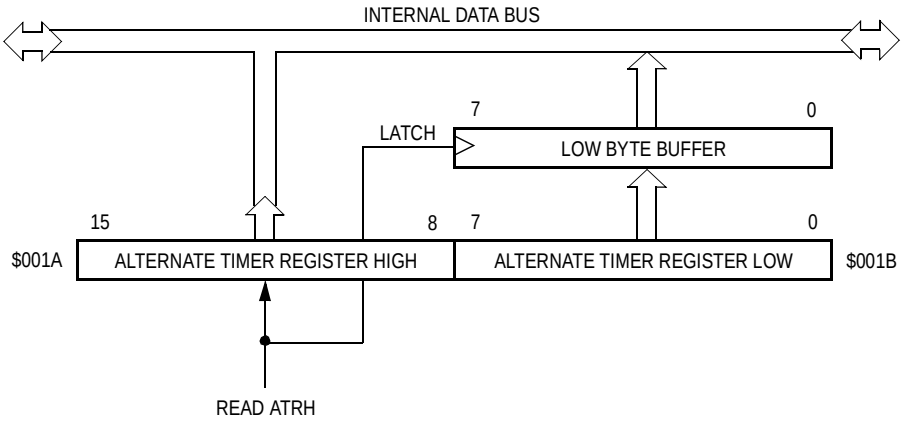

Figure 8-10. Alternate Timer Register Reads

NOTE: *To prevent interrupts from occurring between readings of ATRH and ATRL, set the interrupt mask (I bit) in the condition code register before reading ATRH, and clear the mask after reading ATRL.*

8.4.5 Input Capture Registers

When a selected edge occurs on the TCAP pin, the current high and low bytes of the 16-bit counter are latched into the read-only input capture registers (ICRH and ICRL) shown in **Figure 8-11**. Reading ICRH before reading ICRL inhibits further captures until ICRL is read. Reading ICRL after reading the timer status register clears the input capture flag (ICF). Writing to the input capture registers has no effect.

	Bit 7	6	5	4	3	2	1	Bit 0
Register Name and Address: Input Capture Register High — $0014								
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Unaffected by reset							
Register Name and Address: Input Capture Register Low — $0015								
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							

= Unimplemented

Figure 8-11. Input Capture Registers (ICRH and ICRL)

NOTE: *To prevent interrupts from occurring between readings of ICRH and ICRL, set the interrupt mask (I bit) in the condition code register before reading ICRH and clear the mask after reading ICRL.*

9.4.7 Execute Program in RAM

This routine allows the MCU to transfer control to a program previously loaded in RAM. This program is executed once bootstrap mode is entered, if switch S6 is in the ON position and switch 2 is in the OUT position, without any firmware initialization. The program must start at location $0051 to be compatible with the load program in RAM routine.

To run the execute program in RAM routine, take these steps:

1. Set switch 1 in the ON position (restores V_{DD}).
2. Connect V_{PP} to V_{DD}.
3. Set switch S6 in the OFF position.
4. Switches S3, S4, and S5 can be in either position.
5. Set switch 2 in the OUT position (routine is activated).

NOTE: *The non-programmable watchdog COP is disabled in bootloader mode, even if the NCOPE bit is programmed.*

9.4.8 Dump PROM Contents

In the dump PROM contents routine, the PROM contents are dumped sequentially to the SCI output, provided the PROM has not been secured. The first location sent is $0020 and the last location sent is $1FFF. Unused locations are skipped so that no gaps exist in the data stream. The external memory address lines indicate the current location being sent. Data is sent with eight data bits and one stop bit at 4800 baud with a 2-MHz crystal or 9600 baud with a 4-MHz crystal.

To run the dump PROM contents routine, take these steps:

1. Set switch 1 in the ON position (restores V_{DD}).
2. Connect V_{PP} to V_{DD}.
3. Set switches S3 and S6 in the OFF position.
4. Set switches S4 and S5 in the ON position.
5. Set switch 2 in the OUT position (routine is activated).
6. Once PROM dumping is complete, set switch 2 in the RESET position.

NOTE: *PBPU0/COPC programmed to a 1 enables the port B pullup bit. This bit is also used to clear the non-programmable COP (MC68HC05C4A type). Writing to this bit to clear the COP will not affect the state of the port B pull-up (bit 0). See* ***5.3.3 Programmable and Non-Programmable COP Watchdog Resets***.

When using the MC68HC705C8A in an MC68HC705C8 or MC68HSC705C8 application, program locations $1FF0 and $1FF1 to $00.

9.5.3 Mask Option Register 2

Mask option register 2 (MOR2) shown in **Figure 9-6** is an EPROM register that enables the non-programmable COP watchdog. Data from MOR2 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin. See **5.3.3 Programmable and Non-Programmable COP Watchdog Resets**.

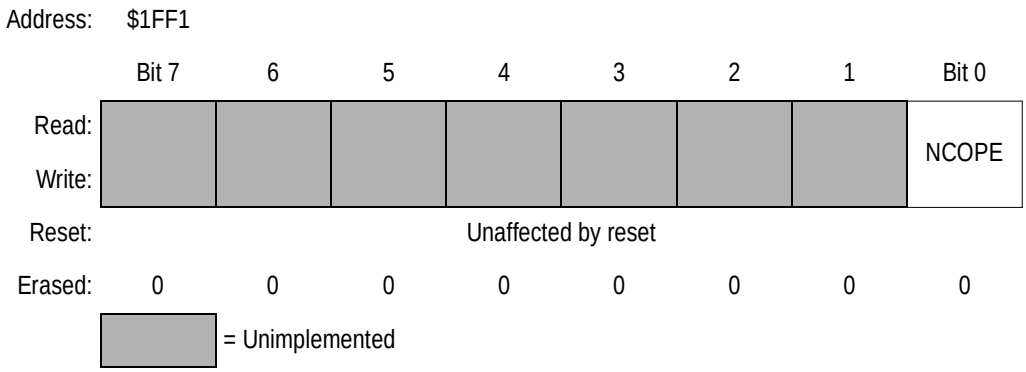

Figure 9-6. Mask Option Register 2 (MOR2)

NCOPE — Non-Programmable COP Watchdog Enable Bit

This EPROM bit enables the non-programmable COP watchdog.

1 = Non-programmable COP watchdog enabled
0 = Non-programmable COP watchdog disabled

OR — Receiver Overrun Bit

This clearable, read-only bit is set if the SCDR is not read before the receive shift register receives the next word. OR generates an interrupt request if the RIE bit in SCCR2 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading the SCSR with OR set and then reading the SCDR. Reset clears the OR bit.

1 = Receiver shift register full and RDRF = 1
0 = No receiver overrun

NF — Receiver Noise Flag Bit

This clearable, read-only bit is set when noise is detected in data received in the SCI data register. Clear the NF bit by reading the SCSR and then reading the SCDR. Reset clears the NF bit.

1 = Noise detected in SCDR
0 = No noise detected in SCDR

FE — Receiver Framing Error Bit

This clearable, read-only flag is set when a logic 0 is located where a stop bit should be in the character shifted into the receive shift register. If the received word causes both a framing error and an overrun error, the OR bit is set and the FE bit is not set. Clear the FE bit by reading the SCSR and then reading the SCDR. Reset clears the FE bit.

1 = Framing error
0 = No framing error

Section 11. Serial Peripheral Interface (SPI)

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11.2 Introduction

The serial peripheral interface (SPI) module allows full-duplex, synchronous, serial communication with peripheral devices.

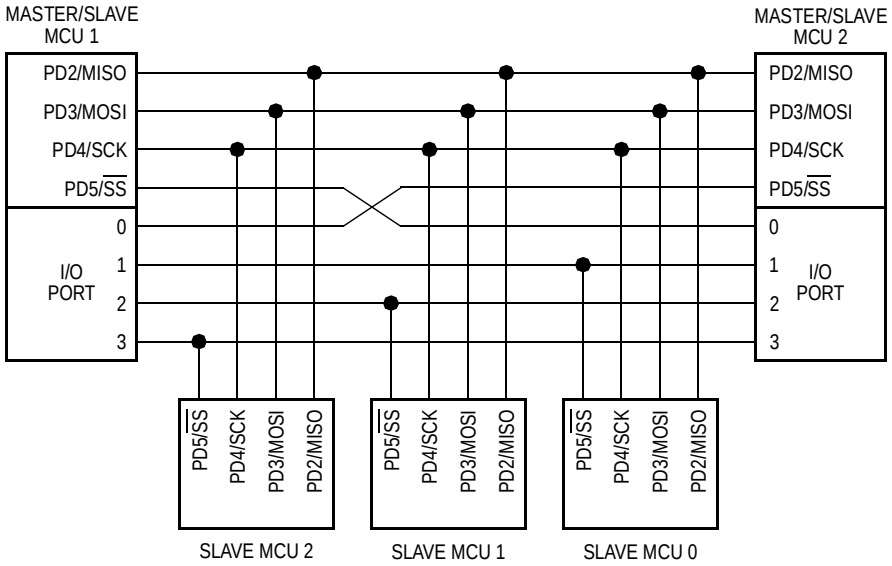


Figure 11-5. Two Master/Slaves and Three Slaves Block Diagram

11.6 Serial Clock Polarity and Phase

To accommodate the different serial communication requirements of peripheral devices, software can change the phase and polarity of the SPI serial clock. The clock polarity bit (CPOL) and the clock phase bit (CPHA), both in the SPCR, control the timing relationship between the serial clock and the transmitted data. **Figure 11-6** shows how the CPOL and CPHA bits affect the clock/data timing.

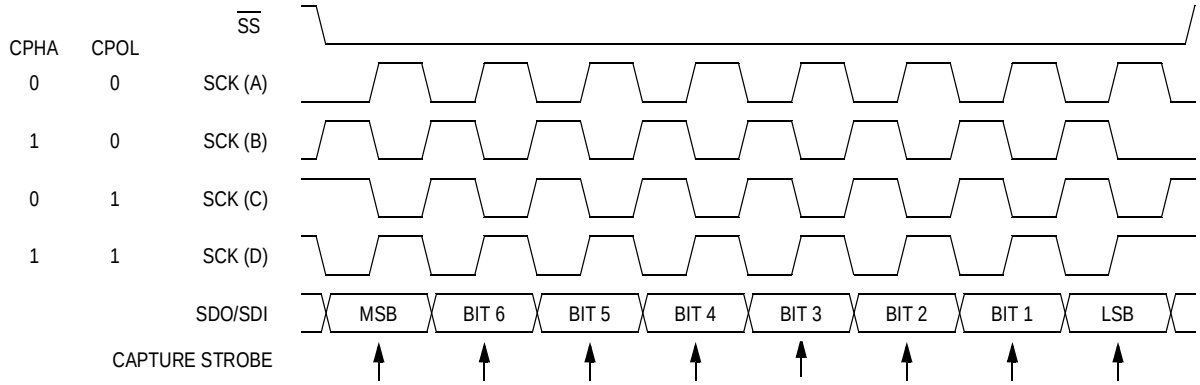


Figure 11-6. SPI Clock/Data Timing

Table 12-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if carry bit clear	BCC
Branch if carry bit set	BCS
Branch if equal	BEQ
Branch if half-carry bit clear	BHCC
Branch if half-carry bit set	BHCS
Branch if higher	BHI
Branch if higher or same	BHS
Branch if $\overline{\text{IRQ}}$ pin high	BIH
Branch if $\overline{\text{IRQ}}$ pin low	BIL
Branch if lower	BLO
Branch if lower or same	BLS
Branch if interrupt mask clear	BMC
Branch if minus	BMI
Branch if interrupt mask set	BMS
Branch if not equal	BNE
Branch if plus	BPL
Branch always	BRA
Branch if bit clear	BRCLR
Branch never	BRN
Branch if bit set	BRSET
Branch to subroutine	BSR
Unconditional jump	JMP
Jump to subroutine	JSR

13.6 Power Considerations

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where:

T_A = ambient temperature in °C
θ_{JA} = package thermal resistance, junction to ambient in °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$ = chip internal power dissipation
$P_{I/O}$ = power dissipation on input and output pins (user-determined)

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

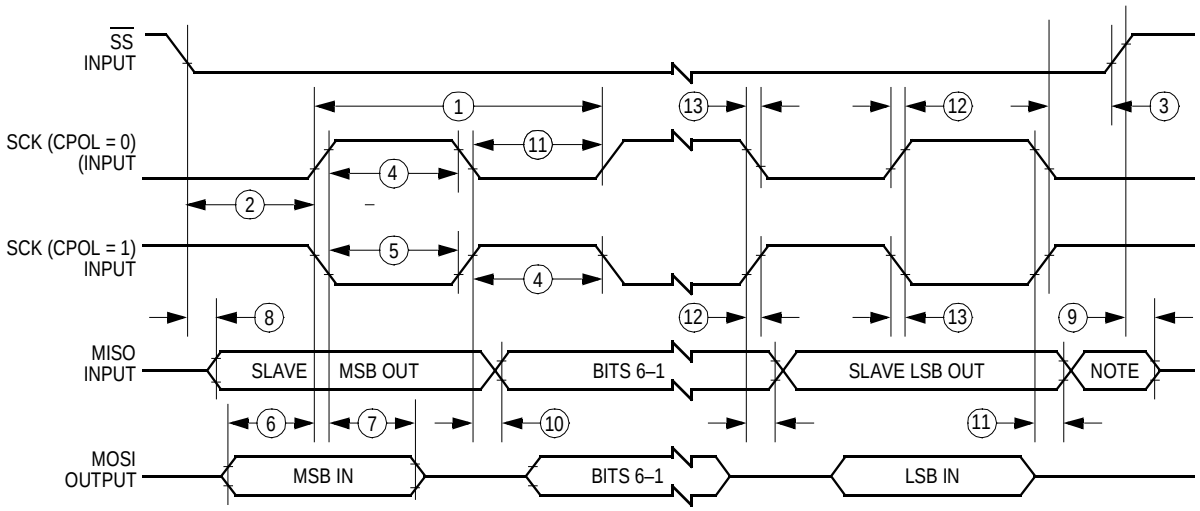
Ignoring $P_{I/O}$, the relationship between P_D and T_J is approximately:

$$P_D = \frac{K}{T_J + 273°C} \quad (2)$$

Solving equations (1) and (2) for K gives:

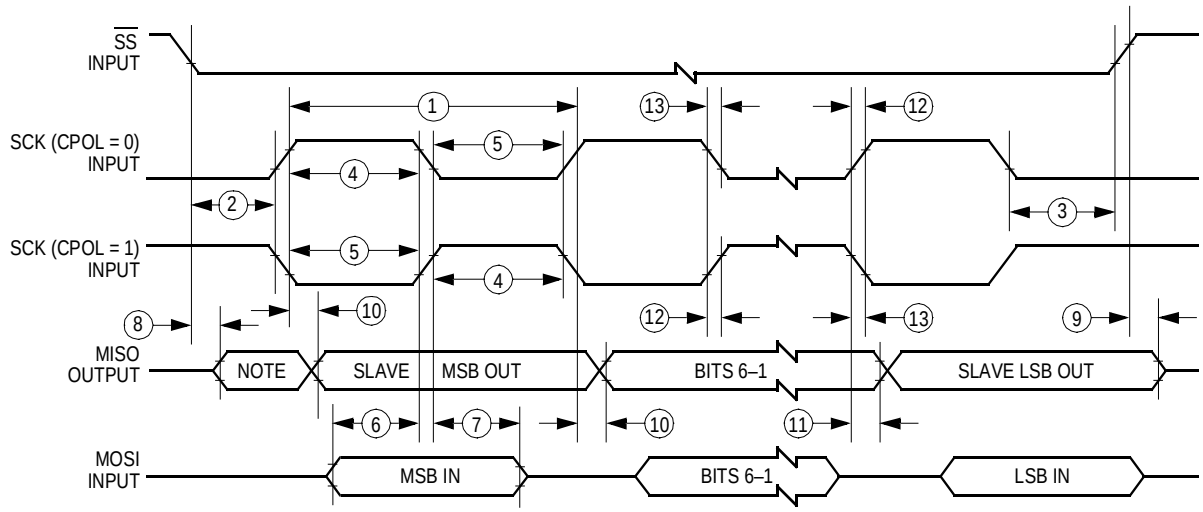
$$= P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.



Note: Not defined, but normally MSB of character just received

a) SPI Slave Timing (CPHA = 0)

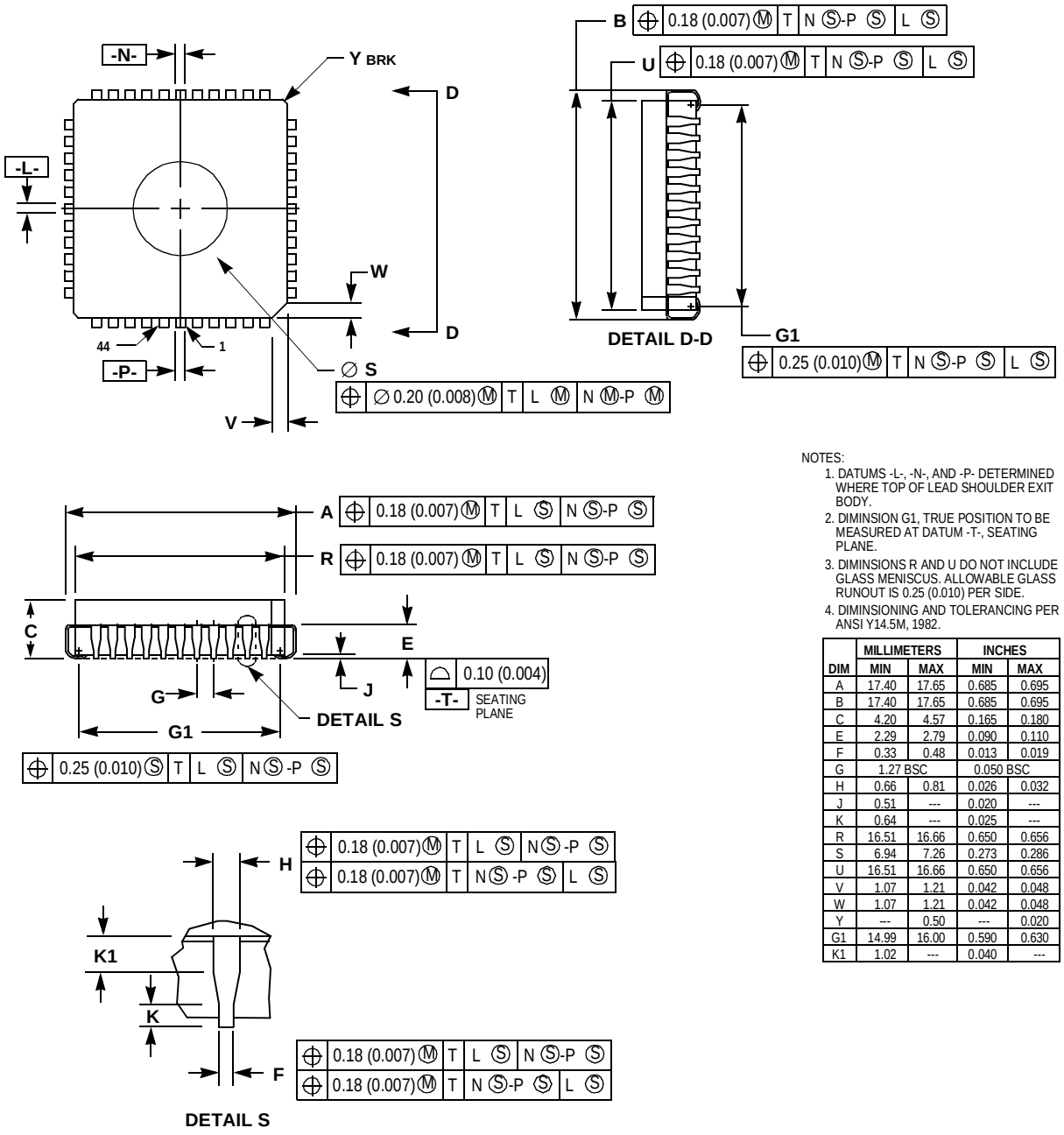


Note: Not defined, but normally LSB of character previously transmitted

b) SPI Slave Timing (CPHA = 1)

Figure 13-9. SPI Slave Timing

14.6 44-Lead Ceramic-Leaded Chip Carrier (CLCC)



NOTES:
1. DATUMS -L-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT BODY.
2. DIMINSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMINSIONS R AND U DO NOT INCLUDE GLASS MENISCUS. ALLOWABLE GLASS RUNOUT IS 0.25 (0.010) PER SIDE.
4. DIMINSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	---	0.020	---
K	0.64	---	0.025	---
R	16.51	16.66	0.650	0.656
S	6.94	7.26	0.273	0.286
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
Y	---	0.50	---	0.020
G1	14.99	16.00	0.590	0.630
K1	1.02	---	0.040	---

Figure 14-4. MC68HC705C8AFS Package Dimensions (Case #777B)

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