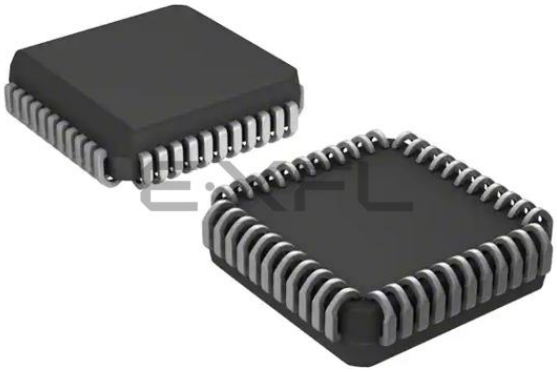

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705c8acfn

Section 1. General Description

1.1 Contents

1.7.7 Output Compare Pin (TCMP)

The TCMP pin is the output compare pin for the on-chip capture/compare timer. See Section 8. Capture/Compare Timer .

1.7.8 Port A I/O Pins (PA7 –PA0)

These eight I/O lines comprise port A, a general-purpose, bidirectional I/O port. The pins are programmable as either inputs or outputs under software control of the data direction registers. See 7.3 Port A .

1.7.9 Port B I/O Pins (PB7 –PB0)

These eight I/O pins comprise port B, a general-purpose, bidirectional I/O port. The pins are programmable as either inputs or outputs under software control of the data direction registers. Port B pins also can be configured to function as external interrupts. See 7.4 Port B .

1.7.10 Port C I/O Pins (PC7 –PC0)

These eight I/O pins comprise port C, a general-purpose, bidirectional I/O port. The pins are programmable as either inputs or outputs under software control of the data direction registers. PC7 has a high current sink and source capability. See 7.5 Port C .

1.7.11 Port D I/O Pins (PD7 and PD5 –PD0)

These seven lines comprise port D, a fixed input port. All special functions that are enabled (SPI and SCI) affect this port. See 7.6 Port D .

3.3.5 Condition Code Register

The condition code register (CCR) shown in Figure 3-6 is an 8-bit register whose three most significant bits are permanently fixed at 111. The condition code register contains the interrupt mask and four bits that indicate the results of prior instructions.

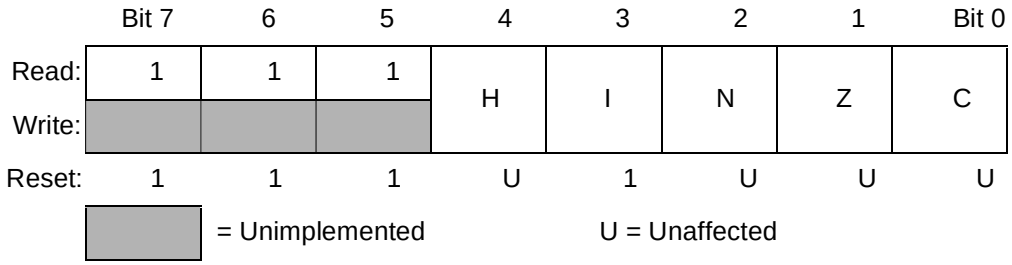

Figure 3-6. Condition Code Register (CCR)

H — Half-Carry Bit

The CPU sets the half-carry flag when a carry occurs between bits 3 and 4 of the accumulator during an add without carry (ADD) or add with carry (ADC) operation. The half-carry bit is required for binary-coded decimal (BCD) arithmetic operations. Reset has no affect on the half-carry flag.

I — Interrupt Mask Bit

Setting the interrupt mask (I) disables interrupts. If an interrupt request occurs while the interrupt mask is a logic 0, the CPU saves the CPU registers on the stack, sets the interrupt mask, and then fetches the interrupt vector. If an interrupt request occurs while the interrupt mask is set, the interrupt request is latched. The CPU processes the latched interrupt as soon as the interrupt mask is cleared again.

A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack, restoring the interrupt mask to its cleared state. After a reset, the interrupt mask is set and can be cleared only by a CLI, STOP, or WAIT instruction.

N — Negative Flag

The CPU sets the negative flag when an arithmetic operation, logical operation, or data manipulation produces a negative result (bit 7 in the results is a logic 1). Reset has no effect on the negative flag.

Z — Zero Flag

The CPU sets the zero flag when an arithmetic operation, logical operation, or data manipulation produces a result of $00. Reset has no effect on the zero flag.

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow bit. Reset has no effect on the carry/borrow flag.

3.4 Arithmetic/Logic Unit (ALU)

The arithmetic/logic unit (ALU) performs the arithmetic and logical operations defined by the instruction set. The binary arithmetic circuits decode instructions and set up the ALU for the selected operation. Most binary arithmetic is based on the addition algorithm, carrying out subtraction as negative addition. Multiplication is not performed as a discrete operation but as a chain of addition and shift operations within the ALU. The multiply instruction requires 11 internal clock cycles to complete this chain of operations.

Section 4. Interrupts

4.1 Contents

4.2 Introduction

This section describes how interrupts temporarily change the normal processing sequence.

4.3.2 External Interrupt ($\overline{\text{IRQ}}$)

An interrupt signal on the $\overline{\text{IRQ}}$ pin latches an external interrupt request. After completing the current instruction, the CPU tests these bits:

- IRQ latch
- I bit in the CCR

Setting the I bit in the CCR disables external interrupts.

If the IRQ latch is set and the I bit is clear, the CPU then begins the interrupt sequence. The CPU clears the IRQ latch while it fetches the interrupt vector, so that another external interrupt request can be latched during the interrupt service routine. As soon as the I bit is cleared during the return-from-interrupt (RTI) instruction, the CPU can recognize the new interrupt request. Figure 4-1 shows the logic for external interrupts.

Figure 4-1 shows an external interrupt functional diagram. Figure 4-2 shows an external interrupt timing diagram for the interrupt line. The tiL15( )v9 Tc6(r)-4(upt)21(func012 111015( )v9 e)18(ter)4(u)15(he)]TJon, i7.44.

2. COP clear bit (COPC) at address $1FF0

   To clear the non-programmable COP watchdog and start a new COP timeout period, write a logic 0 to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. See 9.5.2 Mask Option Register 1 .

NOTE: The non-programmable watchdog COP is disabled in bootloader mode, even if the NCOPE bit is programmed.

Figure 5-4 is a diagram of the non-programmable COP.

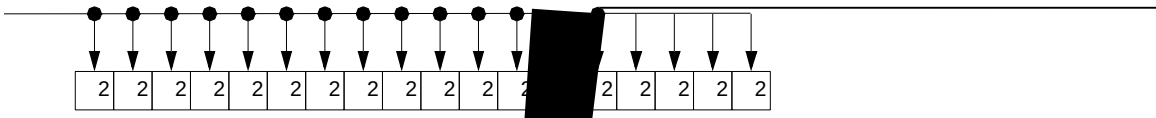

Figure 5-4. Non-Programmable COP Watchdog Diagram

5.3.4 Clock Monitor Reset

When the CME bit in the COP control register is set, the clock monitor detects the absence of the internal bus clock for a certain period of time. The timeout period depends on processing parameters and varies from 5 s to 100 s, which implies that systems using a bus clock rate of 200 kHz or less should not use the clock monitor function.

If a slow or absent clock is detected, the clock monitor causes a system reset. The reset is issued to the external system for four bus cycles using the bidirectional $\overline{\text{RESET}}$ pin.

Special consideration is required when using the STOP instruction with the clock monitor. Since STOP causes the system clocks to halt, the clock monitor issues a system reset when STOP is executed.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0012	Timer Control Register (TCR) See page 94	Read:	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
		Write:								
		Reset:	0	0	0	0	0	0	U	0
$0013	Timer Status Register (TSR) See page 96	Read:	ICF	OCF	TOF	0	0	0	0	0
		Write								
		Reset:	U	U	U	0	0	0	0	0
$0014	Input Capture Register High (ICRH) See page 100	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write								
		Reset:	Unaffected by reset							
$0015	Input Capture Register Low (ICRL) See page 100	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write								
		Reset:	Unaffected by reset							
$0016	Output Compare Register High (OCRH) See page 101.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Unaffected by reset							
$0017	Output Compare Register Low (OCRL) See page 101	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							
$0018	Timer Register High (TRH) See page 97	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write								
		Reset:	Reset initializes TRH to $FF							
$0019	Timer Register Low (TRL) See page 97	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write								
		Reset:	Reset initializes TRL to $FC							
$001A	Alternate Timer Register High (ATRH) See page 99	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write								
		Reset:	Reset initializes ATRH to $FF							
$001B	Alternate Timer Register Low (ATRL) See page 99	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write								
		Reset:	Reset initializes ATRL to $FC							

= Unimplemented U = Unaffected

Figure 8-2. Timer I/O Register Summary