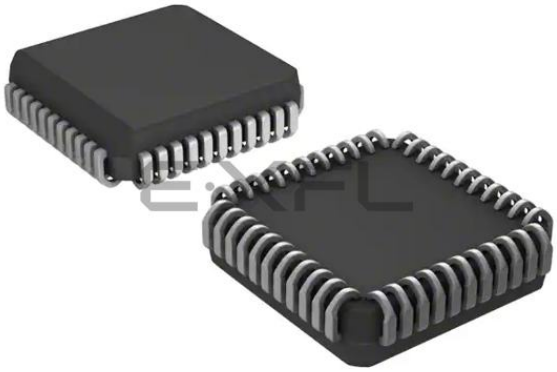

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705c8acfne

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3.3 CPU Registers

Figure 3-1 shows the five CPU registers. These are hard-wired registers within the CPU and are not part of the memory map.

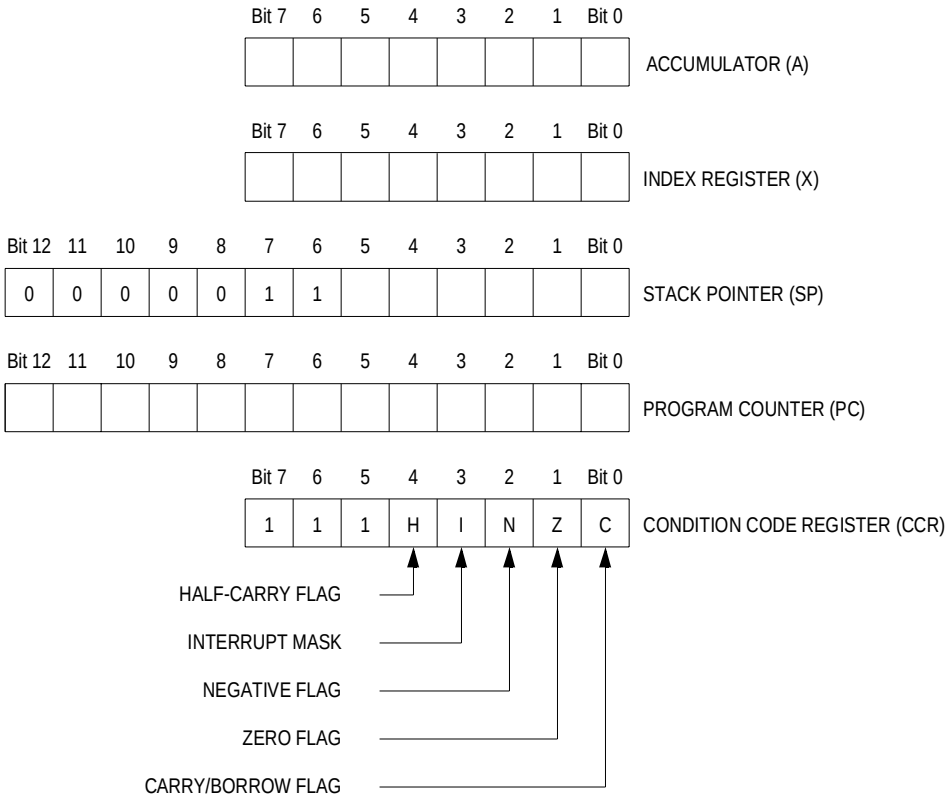

Figure 3-1. Programming Model

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2. COP clear bit (COPC) at address $1FF0

   To clear the non-programmable COP watchdog and start a new COP timeout period, write a logic 0 to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. See **9.5.2 Mask Option Register 1**.

NOTE: *The non-programmable watchdog COP is disabled in bootloader mode, even if the NCOPE bit is programmed.*

Figure 5-4 is a diagram of the non-programmable COP.

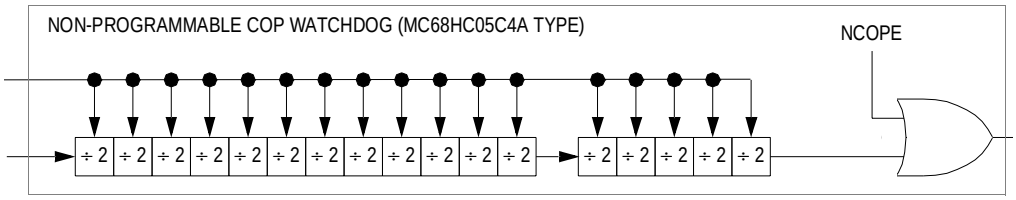

Figure 5-4. Non-Programmable COP Watchdog Diagram

5.3.4 Clock Monitor Reset

When the CME bit in the COP control register is set, the clock monitor detects the absence of the internal bus clock for a certain period of time. The timeout period depends on processing parameters and varies from 5 µs to 100 µs, which implies that systems using a bus clock rate of 200 kHz or less should not use the clock monitor function.

If a slow or absent clock is detected, the clock monitor causes a system reset. The reset is issued to the external system for four bus cycles using the bidirectional $\overline{\text{RESET}}$ pin.

Special consideration is required when using the STOP instruction with the clock monitor. Since STOP causes the system clocks to halt, the clock monitor issues a system reset when STOP is executed.

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6.4.1 Programmable COP Watchdog in Wait Mode

The programmable COP watchdog is active during wait mode. Software must periodically bring the MCU out of wait mode to clear the programmable COP watchdog.

6.4.2 Non-Programmable COP Watchdog in Wait Mode

The non-programmable COP watchdog is active during wait mode. Software must periodically bring the MCU out of wait mode to clear the non-programmable COP watchdog.

6.5 Data-Retention Mode

In data-retention mode, the MCU retains random-access memory (RAM) contents and CPU register contents at V_{DD} voltages as low as 2.0 Vdc. The data-retention feature allows the MCU to remain in a low power-consumption state during which it retains data, but the CPU cannot execute instructions.

To put the MCU in data-retention mode:

1. Drive the $\overline{\text{RESET}}$ pin to logic 0.
2. Lower V_{DD} voltage. The $\overline{\text{RESET}}$ pin must remain low continuously during data-retention mode.

To take the MCU out of data-retention mode:

1. Return V_{DD} to normal operating voltage.
2. Return the $\overline{\text{RESET}}$ pin to logic 1.

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7.3.2 Data Direction Register A

The contents of data direction register A (DDRA) shown in **Figure 7-2** determine whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the associated port A pin; a logic 0 disables the output buffer. A reset clears all DDRA bits, configuring all port A pins as inputs.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 7-2. Data Direction Register A (DDRA)

DDRA7–DDRA0 — Port A Data Direction Bits

These read/write bits control port A data direction. Reset clears bits DDRA7–DDRA0.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE: *Avoid glitches on port A pins by writing to the port A data register before changing DDRA bits from logic 0 to logic 1.*

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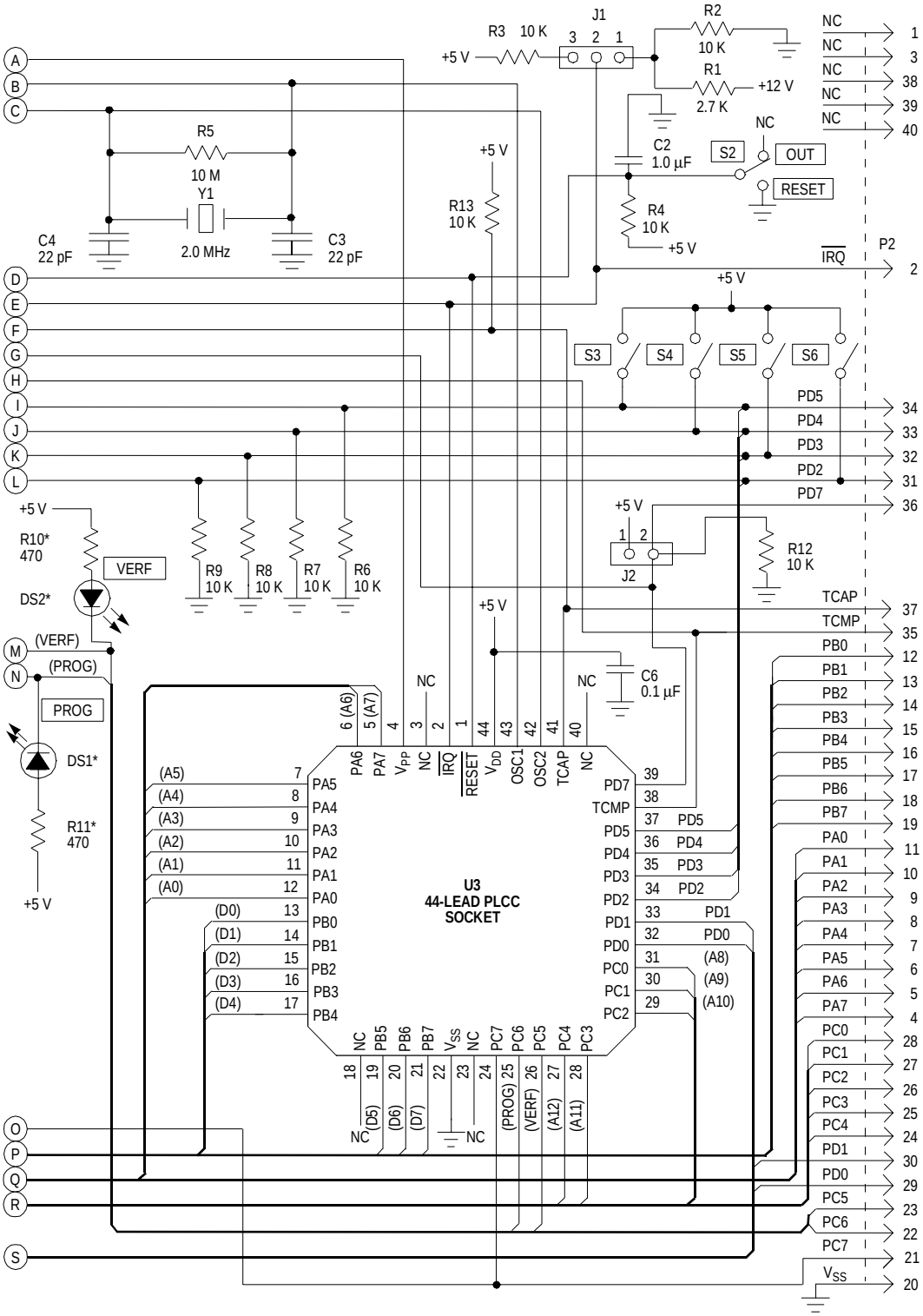

Figure 9-2. PROM Programming Circuit (Continued)

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To program the PROM MCU, the MCU is installed in the PCB, along with an EPROM device programmed with user code; the MCU is then subjected to a series of routines. The routines necessary to program, verify, and secure the PROM MCU are:

- Program and verify PROM
- Verify PROM contents only
- Secure PROM and verify
- Secure PROM and dump through the serial communications interface (SCI)

Other board routines available to the user are:

- Load program into random-access memory (RAM) and execute
- Execute program in RAM
- Dump PROM contents (binary upload)

The user first configures the MCU for the bootstrap mode of operations by installing a fabricated jumper across pins 1 and 2 of the board's mode select header, J1. Next, the board's mode switches (S3, S4, S5, and S6) are set to determine the routine to be executed after the next reset, as shown in **Table 9-2**.

Table 9-2. PROM Programming Routines

Routine	S3	S4	S5	S6
Program and verify PROM	Off	Off	Off	Off
Verify PROM contents only	Off	Off	On	Off
Secure PROM contents and verify	On	Off	On	Off
Secure PROM contents and dump	On	On	On	Off
Load program into RAM and execute	Off	On	Off	Off
Execute program in RAM	Off	Off	Off	On
Dump PROM contents	Off	On	On	Off

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9.5 Control Registers

This subsection describes the three registers that control memory configuration, PROM security, and IRQ edge or level sensitivity; port B pullups; and non-programmable COP enable/disable.

9.5.1 Option Register

The option register shown in **Figure 9-4** is used to select the IRQ sensitivity, enable the PROM security, and select the memory configuration.

Address: $1FDF

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RAM0	RAM1	0	0	SEC*		IRQ	0
Reset:	0	0	0	0	*	U	1	0

*Implemented as an EPROM cell

= Unimplemented U = Unaffected

Figure 9-4. Option Register (Option)

RAM0 — Random-Access Memory Control Bit 0

1 = Maps 32 bytes of RAM into page zero starting at address $0030. Addresses from $0020 to $002F are reserved. This bit can be read or written at any time, allowing memory configuration to be changed during program execution.

0 = Provides 48 bytes of PROM at location $0020–$005F.

RAM1 — Random-Access Memory Control Bit 1

1 = Maps 96 bytes of RAM into page one starting at address $0100. This bit can be read or written at any time, allowing memory configuration to be changed during program execution.

0 = Provides 96 bytes of PROM at location $0100.

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9.6 EPROM Erasing

The erased state of an EPROM or OTPROM byte is $00. EPROM devices can be erased by exposure to a high intensity ultraviolet (UV) light with a wave length of 2537 Å. The recommended erasure dosage (UV intensity on a given surface area x exposure time) is 15 Ws/cm^2. UV lamps should be used without short-wave filters, and the EPROM device should be positioned about one inch from the UV source.

OTPROM devices are shipped in an erased state. Once programmed, they cannot be erased. Electrical erasing procedures cannot be performed on either EPROM or OTPROM devices.

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Section 10. Serial Communications Interface (SCI)

10.1 Contents

10.2 Introduction

The serial communications interface (SCI) module allows high-speed asynchronous communication with peripheral devices and other microcontroller units (MCUs).

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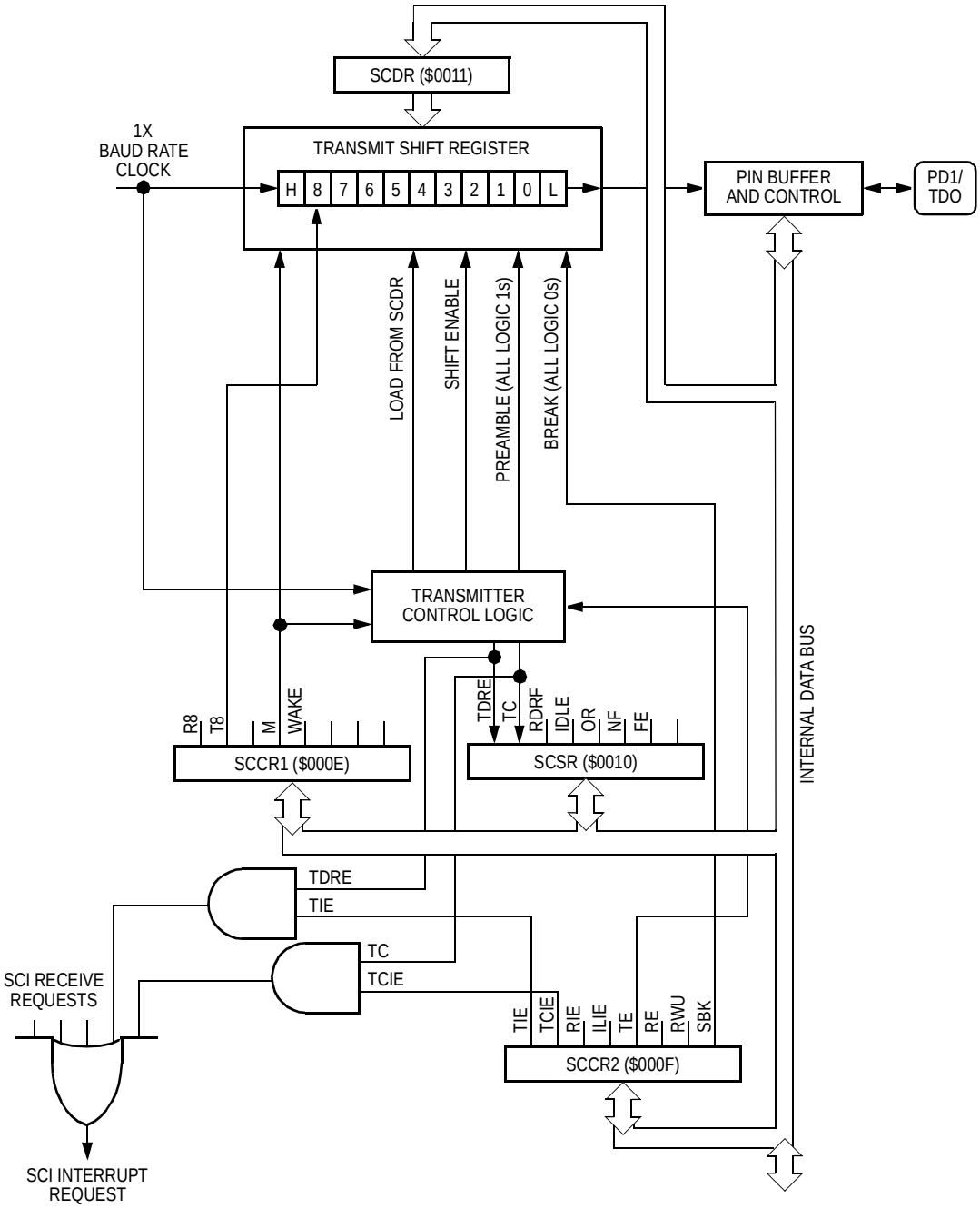

Figure 10-2. SCI Transmitter

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000D	Baud Rate Register (Baud) See page 136.	Read:			SCP1	SCP0		SCR2	SCR1	SCR0
		Write:								
		Reset:	U	U	0	0	U	U	U	U
$000E	SCI Control Register 1 (SCCR1) See page 130.	Read:	R8	T8		M	WAKE			
		Write:								
		Reset:	U	U		U	U			
$000F	SCI Control Register 2 (SCCR2) See page 131.	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0010	SCI Status Register (SCSR) See page 133.	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	
		Write:								
		Reset:	1	1	0	0	0	0	0	U
$0011	SCI Data Register (SCDR) See page 129.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented U = Unaffected

Figure 10-3. SCI Transmitter I/O Register Summary

Writing a logic 1 to the TE bit in SCI control register 2 (SCCR2) and then writing data to the SCDR begins the transmission. At the start of a transmission, transmitter control logic automatically loads the transmit shift register with a preamble of logic 1s. After the preamble shifts out, the control logic transfers the SCDR data into the shift register. A logic 0 start bit automatically goes into the least significant bit (LSB) position of the shift register, and a logic 1 stop bit goes into the most significant bit (MSB) position.

When the data in the SCDR transfers to the transmit shift register, the transmit data register empty (TDRE) flag in the SCI status register (SCSR) becomes set. The TDRE flag indicates that the SCDR can accept new data from the internal data bus.

When the shift register is not transmitting a character, the PD1/TDO pin goes to the idle condition, logic 1. If software clears the TE bit during the idle condition, and while TDRE is set, the transmitter relinquishes control of the PD1/TDO pin.

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Section 11. Serial Peripheral Interface (SPI)

11.1 Contents

11.2 Introduction

The serial peripheral interface (SPI) module allows full-duplex, synchronous, serial communication with peripheral devices.

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MODF — Mode Fault Bit

This clearable, read-only bit is set when a logic 0 occurs on the PD5/$\overline{SS}$ pin while the MSTR bit is set. MODF generates an interrupt request if the SPIE bit is also set. Clear the MODF bit by reading the SPSR with MODF set and then writing to the SPCR. Reset clears MODF.

1 = PD5/$\overline{SS}$ pulled low while MSTR bit set
0 = PD5/$\overline{SS}$ not pulled low while MSTR bit set

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Table 12-7. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSB / LSB
0	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0
1	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1
2	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2
3	5 BRCLR1 3 DIR	5 BCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3
4	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4
5	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS/BLO 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5
6	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6
7	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7
8	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 ASL/LSL 2 DIR	3 ASLA/LSLA 1 INH	3 ASLX/LSLX 1 INH	6 ASL/LSL 2 IX1	5 ASL/LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8
9	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9
A	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A
B	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B
C	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C
D	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D
E	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E
F	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended

REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

LSB of Opcode in Hexadecimal

MSB / LSB	0
0	5 BRSET0 3 DIR

MSB of Opcode in Hexadecimal
Number of Cycles
Opcode Mnemonic
Number of Bytes/Addressing Mode

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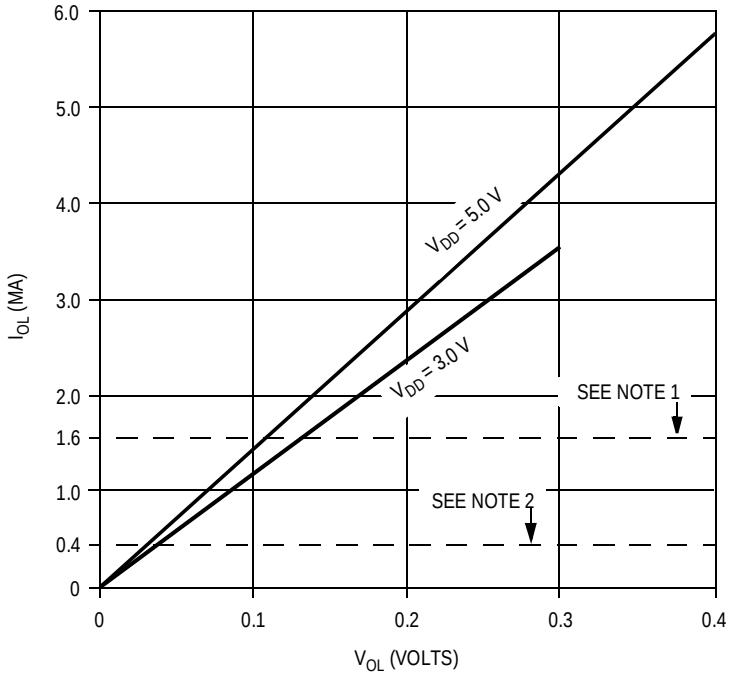

Notes:

1. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 400$ mV @ I_{OL} = 1.6 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 300$ mV @ I_{OL} = 0.4 mA.

(c) V_{OL} versus I_{OL} for All Ports Except PC7

Figure 13-2. Typical Voltage Compared to Current (Continued)

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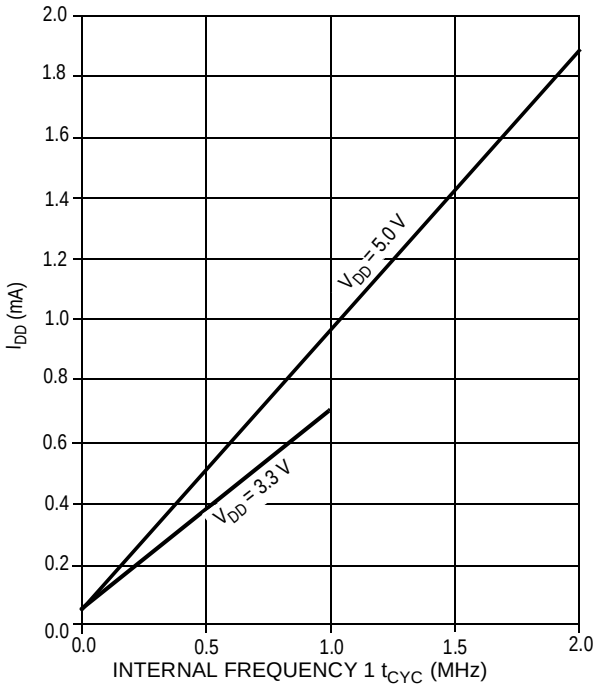
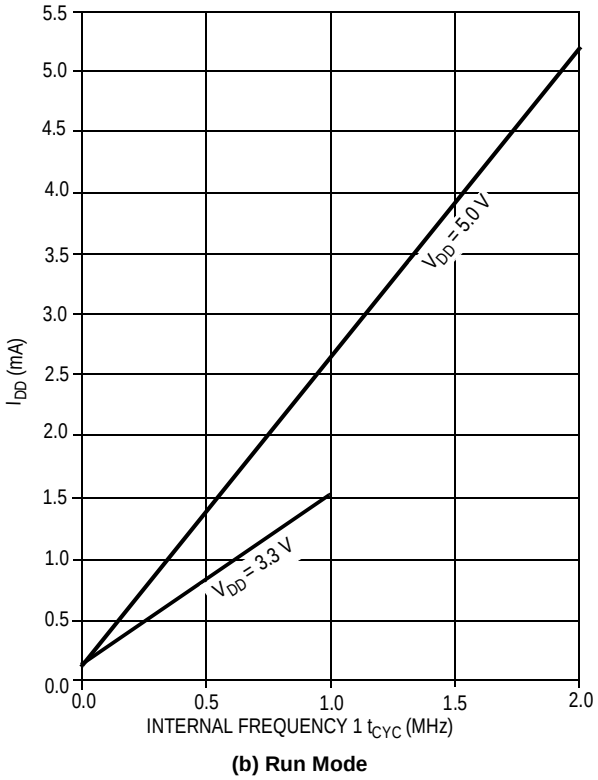


(a) Wait Mode



(b) Run Mode

Figure 13-3. Typical Current versus Internal Frequency for Run and Wait Modes

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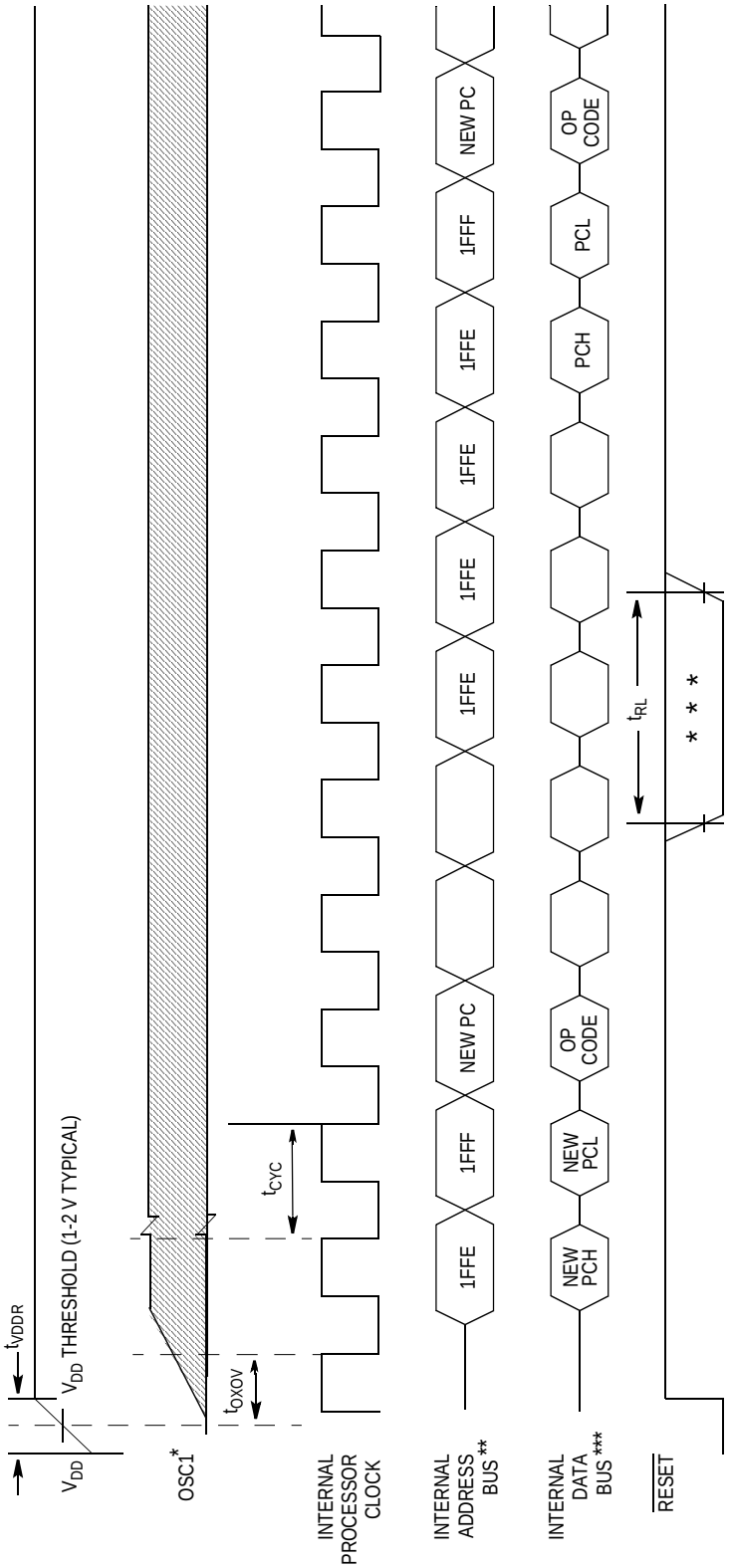

* OSC1 line is not meant to represent frequency. It is only used to represent time.

** Internal timing signal and bus information are not available externally.

***The next rising edge of the internal processor clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 13-7. Power-On Reset and External Reset Timing Diagram

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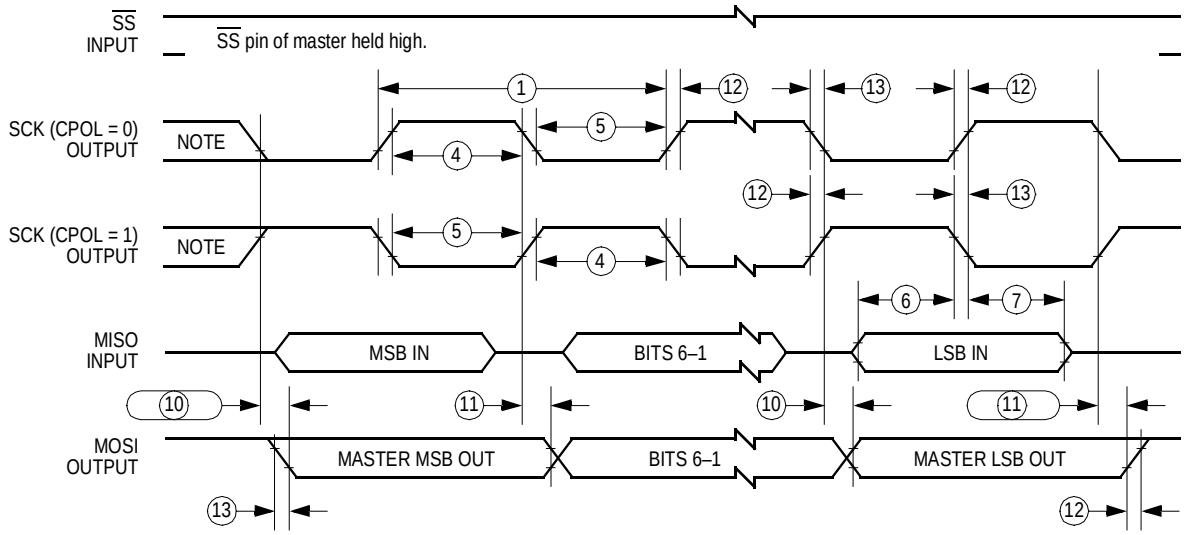
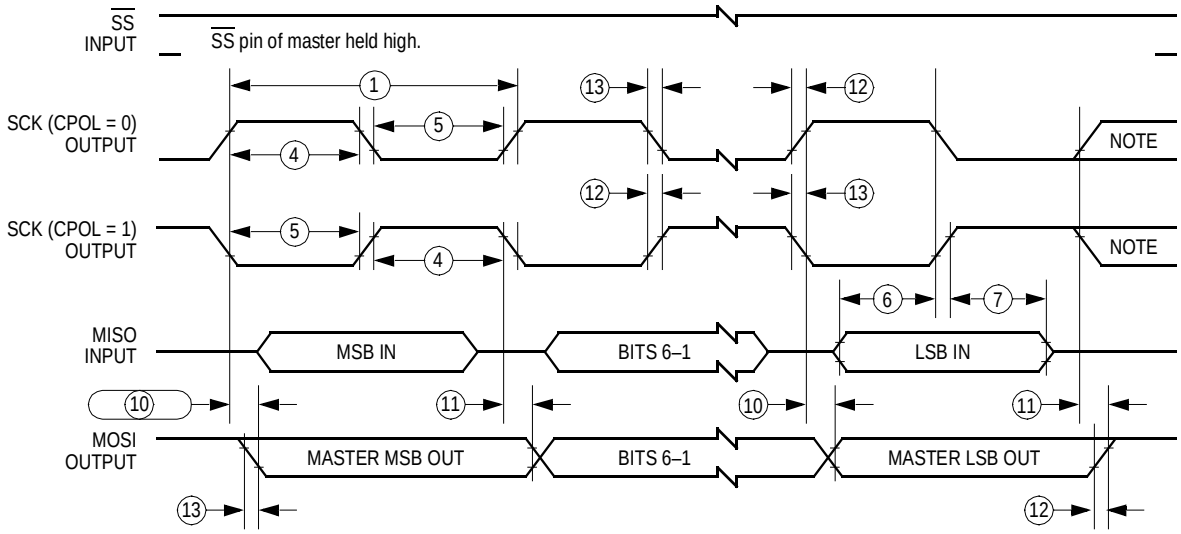


Note: This first clock edge is generated internally, but is not seen at the SCK pin.

a) SPI Master Timing (CPHA = 0)



Note: This last clock edge is generated internally, but is not seen at the SCK pin.

b) SPI Master Timing (CPHA = 1)

Figure 13-8. SPI Master Timing

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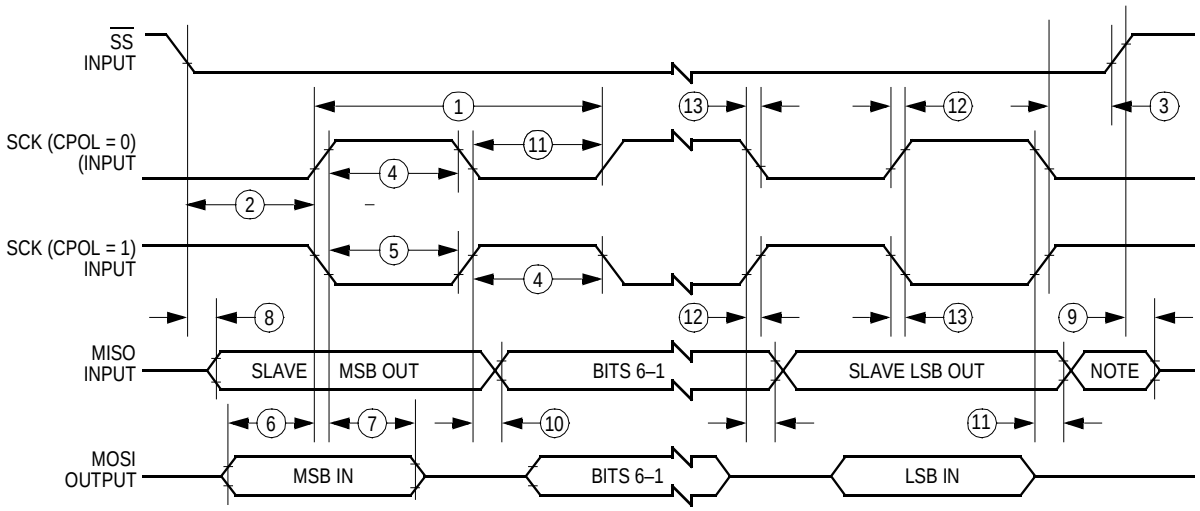
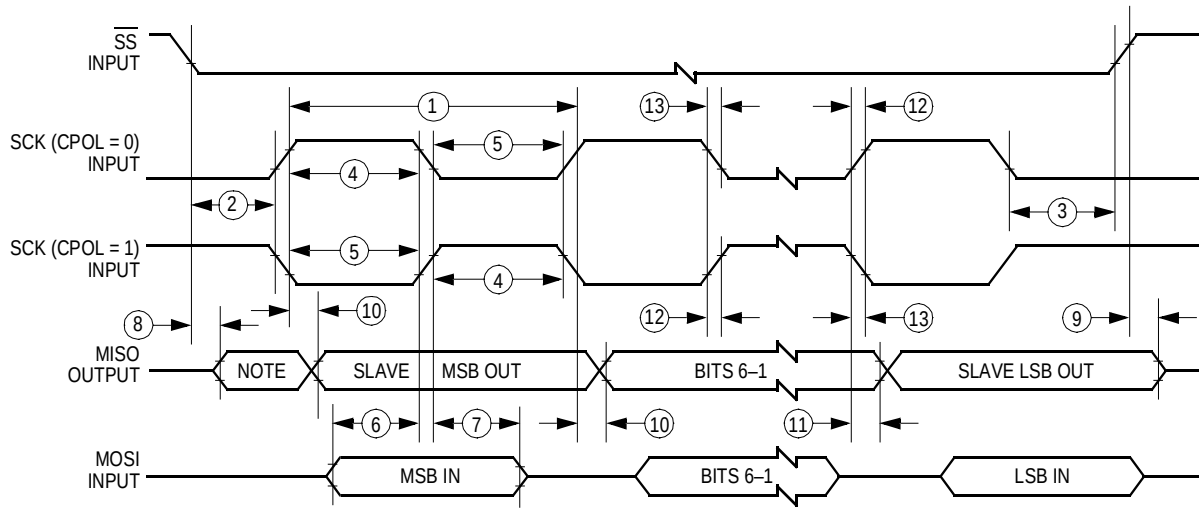


Note: Not defined, but normally MSB of character just received

a) SPI Slave Timing (CPHA = 0)



Note: Not defined, but normally LSB of character previously transmitted

b) SPI Slave Timing (CPHA = 1)

Figure 13-9. SPI Slave Timing

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