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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705c8acp

MC68HC705C8A

MC68HSC705C8A

Technical Data

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://www.freescale.com>

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.



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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0013	Timer Status Register (TSR) See page 96.	Read:	ICF	OCF	TOF	0	0	0	0	0
		Write:								
		Reset:	U	U	U	0	0	0	0	0
\$0014	Input Capture Register High (ICRH) See page 100.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Unaffected by reset							
\$0015	Input Capture Register Low (ICRL) See page 100.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							
\$0016	Output Compare Register High (OCRH) See page 101.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Unaffected by reset							
\$0017	Output Compare Register Low (OCRL) See page 101.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							
\$0018	Timer Register High (TRH) See page 97.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Reset initializes TRH to \$FF							
\$0019	Timer Register Low (TRL) See page 97.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Reset initializes TRL to \$FC							
\$001A	Alternate Timer Register High (ATRH) See page 99.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Reset initializes ATRH to \$FF							
\$001B	Alternate Timer Register Low (ATRL) See page 99.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Reset initializes ATRL to \$FC							
				= Unimplemented U = Unaffected						

Figure 2-2. I/O Register Summary (Sheet 3 of 4)



6.3.4 Non-Programmable COP Watchdog in Stop Mode

The STOP instruction has these effects on the non-programmable COP watchdog:

- Turns off the oscillator and the COP watchdog counter
- Clears the COP watchdog counter

If the $\overline{\text{RESET}}$ pin brings the MCU out of stop mode, the COP watchdog begins counting immediately. The reset function clears the COP counter again after the $4064\text{-}t_{\text{CYC}}$ clock stabilization delay.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of stop mode, the COP watchdog begins counting immediately. The IRQ function does not clear the COP counter again after the $4064\text{-}t_{\text{CYC}}$ clock stabilization delay. See [Figure 6-3](#).

NOTE: *If the clock monitor is enabled ($\text{CME} = 1$), the STOP instruction causes it to time out and reset the MCU.*

6.4 Wait Mode

The WAIT instruction places the MCU in an intermediate power consumption mode. All central processor unit (CPU) activity is suspended, but the oscillator, capture/compare timer, SCI, and SPI remain active. Any interrupt or reset brings the MCU out of wait mode. See [Figure 6-1](#).

The WAIT instruction has these effects on the CPU:

- Clears the I bit in the condition code register, enabling interrupts
- Stops the CPU clock, but allows the internal clock to drive the capture/compare timer, SCI, and SPI

The WAIT instruction does not affect any other registers or I/O lines. The capture/compare timer, SCI, and SPI can be enabled to allow a periodic exit from wait mode.

7.3 Port A

Port A is an 8-bit, general-purpose, bidirectional input/output (I/O) port.

7.3.1 Port A Data Register

The port A data register (PORTA) shown in [Figure 7-1](#) contains a data latch for each of the eight port A pins. When a port A pin is programmed to be an output, the state of its data register bit determines the state of the output pin. When a port A pin is programmed to be an input, reading the port A data register returns the logic state of the pin.

Address: \$0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Write:								
Reset:	Unaffected by reset							

Figure 7-1. Port A Data Register (PORTA)

PA7–PA0 — Port A Data Bits

These read/write bits are software programmable. Data direction of each bit is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

Parallel Input/Output (I/O)

7.6 Port D

Port D is a 7-bit, special-purpose, input-only port that has no data register. Reading address \$0003 returns the logic states of the port D pins.

Port D shares pins PD5–PD2 with the serial peripheral interface module (SPI). When the SPI is enabled, PD5–PD2 read as logic 0s. When the SPI is disabled, reading address \$0003 returns the logic states of the PD5–PD2 pins.

Port D shares pins PD1 and PD0 with the SCI module. When the SCI is enabled, PD1 and PD0 read as logic 0s. When the SCI is disabled, reading address \$0003 returns the logic states of the PD1 and PD0 pins.

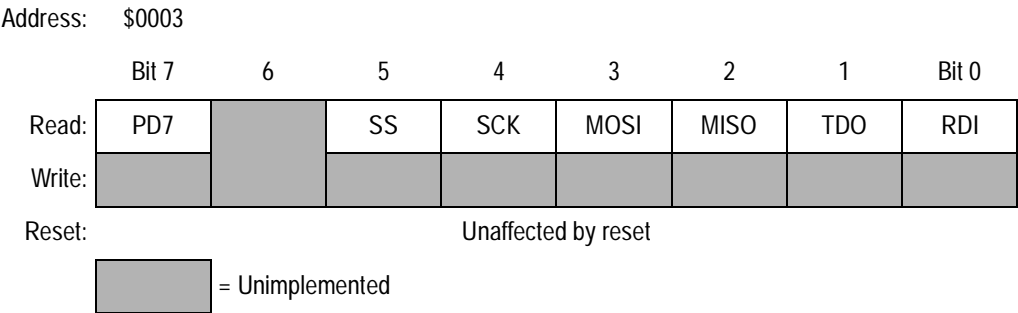


Figure 7-10. Port D Fixed Input Register (PORTD)

8.4.2 Timer Status Register

The timer status register (TSR) is a read-only register shown in **Figure 8-6** contains flags for these events:

- An active signal on the TCAP pin, transferring the contents of the timer registers to the input capture registers
- A match between the 16-bit counter and the output compare registers, transferring the OLVL bit to the TCMP pin
- A timer rollover from \$FFFF to \$0000

Address: \$0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ICF	OCF	TOF	0	0	0	0	0
Write:								
Reset:	U	U	U	0	0	0	0	0


 = Unimplemented U = Unaffected

Figure 8-6. Timer Status Register (TSR)

ICF — Input Capture Flag

The ICF bit is set automatically when an edge of the selected polarity occurs on the TCAP pin. Clear the ICF bit by reading the timer status register with ICF set and then reading the low byte (\$0015) of the input capture registers. Reset has no effect on ICF.

- 1 = Input capture
- 0 = No input capture

OCF — Output Compare Flag

The OCF bit is set automatically when the value of the timer registers matches the contents of the output compare registers. Clear the OCF bit by reading the timer status register with OCF set and then reading the low byte (\$0017) of the output compare registers. Reset has no effect on OCF.

- 1 = Output compare
- 0 = No output compare

Reading TRH returns the current value of the high byte of the counter and causes the low byte to be latched into a buffer, as shown in [Figure 8-8](#). The buffer value remains fixed even if the high byte is read more than once. Reading TRL reads the transparent low byte buffer and completes the read sequence of the timer registers.

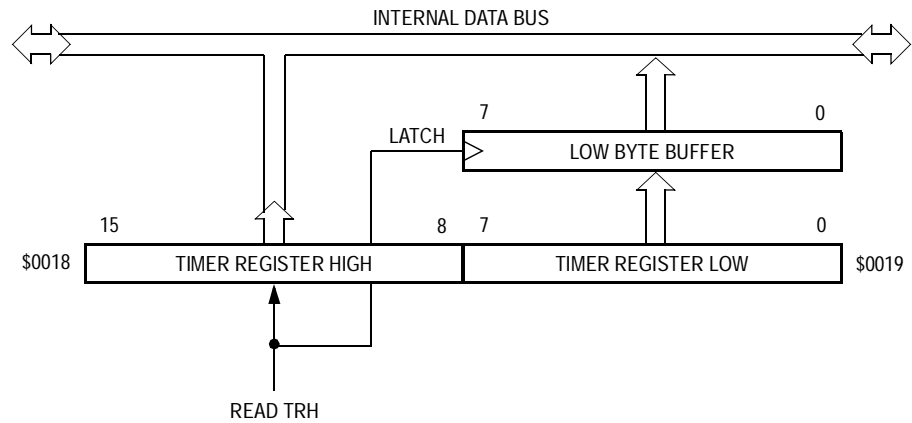


Figure 8-8. Timer Register Reads

NOTE: To prevent interrupts from occurring between readings of TRH and TRL, set the interrupt mask (I bit) in the condition code register before reading TRH, and clear the mask after reading TRL.

8.4.4 Alternate Timer Registers

The alternate timer registers (ATRH and ATRL) shown in [Figure 8-9](#) contain the current high and low bytes of the 16-bit counter. Reading ATRH before reading ATRL causes ATRL to be latched until ATRL is read. Reading does not affect the timer overflow flag (TOF). Writing to the alternate timer registers has no effect.



EPROM/OTPROM (PROM)

Freescale Semiconductor, Inc.

Serial Communications Interface (SCI)

10.6.2 SCI Control Register 1

SCI control register 1 (SCCR1) shown in [Figure 10-6](#) has these functions:

- Stores ninth SCI data bit received and ninth SCI data bit transmitted
- Controls SCI character length
- Controls SCI wakeup method

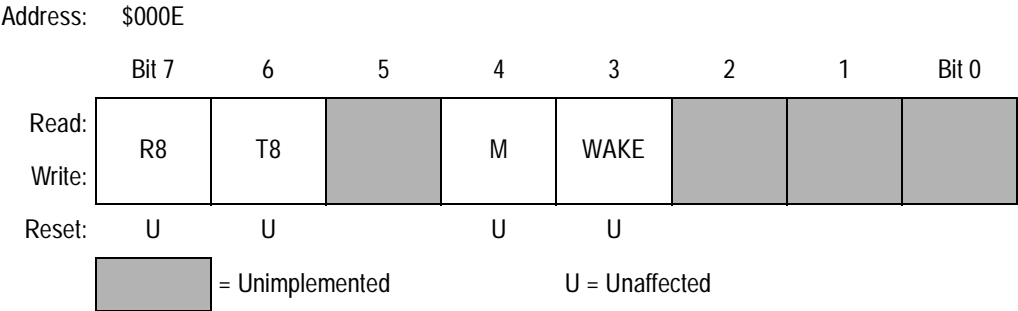


Figure 10-6. SCI Control Register 1 (SCCR1)

R8 — Bit 8 (Received)

When the SCI is receiving 9-bit characters, R8 is the ninth bit of the received character. R8 receives the ninth bit at the same time that the SCDR receives the other eight bits. Reset has no effect on the R8 bit.

T8 — Bit 8 (Transmitted)

When the SCI is transmitting 9-bit characters, T8 is the ninth bit of the transmitted character. T8 is loaded into the transmit shift register at the same time that SCDR is loaded into the transmit shift register. Reset has no effect on the T8 bit.

M — Character Length Bit

This read/write bit determines whether SCI characters are eight or nine bits long. The ninth bit can be used as an extra stop bit, as a receiver wakeup signal, or as a mark or space parity bit. Reset has no effect on the M bit.

- 1 = 9-bit SCI characters
- 0 = 8-bit SCI characters

Serial Peripheral Interface (SPI)

- CPHA = 1 — A slave SPI can cause a write collision error by writing to the SPDR while receiving a transmission, that is, between the first active SCK edge and the end of the eighth SCK cycle. The error does not affect the transmission from the master SPI, but the byte that caused the error is lost.

11.7.3 Overrun Error

Failing to read the byte in the SPDR before a subsequent byte enters the shift register causes an overrun condition. In an overrun condition, all incoming data is lost until software clears SPIF. The overrun condition has no flag.

11.8 SPI Interrupts

The SPIF bit in the SPSR indicates a byte has shifted into or out of the SPDR. The SPIF bit is a source of SPI interrupt requests. The SPI interrupt enable bit (SPIE) in the SPCR is the local mask for SPIF interrupts.

The MODF bit in the SPSR indicates a mode error and is a source of SPI interrupt requests. The MODF bit is set when a logic 0 occurs on the PD5/ \overline{SS} pin while the MSTR bit is set. The SPI interrupt enable bit (SPIE) in the SPCR is the local mask for MODF interrupts.

11.9 SPI I/O Registers

These input/output (I/O) registers control and monitor SPI operation:

- SPI data register (SPDR)
- SPI control register (SPCR)
- SPI status register (SPSR)

12.4.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from -128 to $+127$ from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register.

13.7 5.0-Volt DC Electrical Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Output voltage, $I_{Load} \leq 10.0 \mu A$	V_{OL} V_{OH}	— $V_{DD} - 0.1$	— —	0.1 —	V
Output high voltage $I_{Load} = -0.8 \text{ mA}$, PA7–PA0, PB7–PB0, PC6–PC0, TCMP (see Figure 13-2) $I_{Load} = -1.6 \text{ mA}$, PD4–PD1 (see Figure 13-3) $I_{Load} = -5.0 \text{ mA}$, PC7	V_{OH}	$V_{DD} - 0.8$	— — —	— — —	V
Output low voltage (see Figure 13-4) $I_{Load} = 1.6 \text{ mA}$ PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1 $I_{Load} = 20 \text{ mA}$, PC7	V_{OL}	— —	— —	0.4 0.4	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, \overline{IRQ} , \overline{RESET} , OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, \overline{IRQ} , \overline{RESET} , OSC1	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
EPROM programming voltage	V_{PP}	14.5	14.75	15.0	V
EPROM/OTPROM programming current	I_{PP}	—	5	10	mA
User mode current	I_{PP}	—	—	± 10	mA
Data-retention mode (0°C to 70°C)	V_{RM}	2.0	—	—	V
Supply current ⁽³⁾ Run ⁽⁴⁾ Wait ⁽⁵⁾ Stop ⁽⁶⁾ 25°C –40°C to +85°C	I_{DD}	— — — —	5.0 1.95 5.0 5.0	7.0 3.0 50 50	mA mA μA μA
I/O ports hi-z leakage current PA7–PA0, PB7–PB0, PC7–PC0, PD4–PD1, PD7, \overline{RESET}	I_{IL}	—	—	± 10	μA
Input current, \overline{IRQ} , TCAP, OSC1, PD0, PD5	I_{In}	—	—	± 1	μA
Capacitance Ports (as input or output) \overline{RESET} , \overline{IRQ} , TCAP, PD0–PD5, PD7	C_{Out} C_{In}	— —	— —	12 8	pF

1. $V_{DD} = 5 \text{ V} \pm 10\%$; $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted

2. Typical values reflect average measurements at midpoint of voltage range at 25°C.

3. I_{DD} measured with port B pullup devices disabled.

4. Run (operating) I_{DD} measured using external square wave clock source ($f_{OSC} = 4.2 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2. OSC2 capacitance linearly affects run I_{DD} .

5. Wait I_{DD} measured using external square wave clock source ($f_{OSC} = 4.2 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2. $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects wait I_{DD} .

6. Stop I_{DD} measured with OSC1 = V_{DD} . All ports configured as inputs. $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$.

14.4 40-Pin Ceramic Dual In-Line Package (Cerdip)

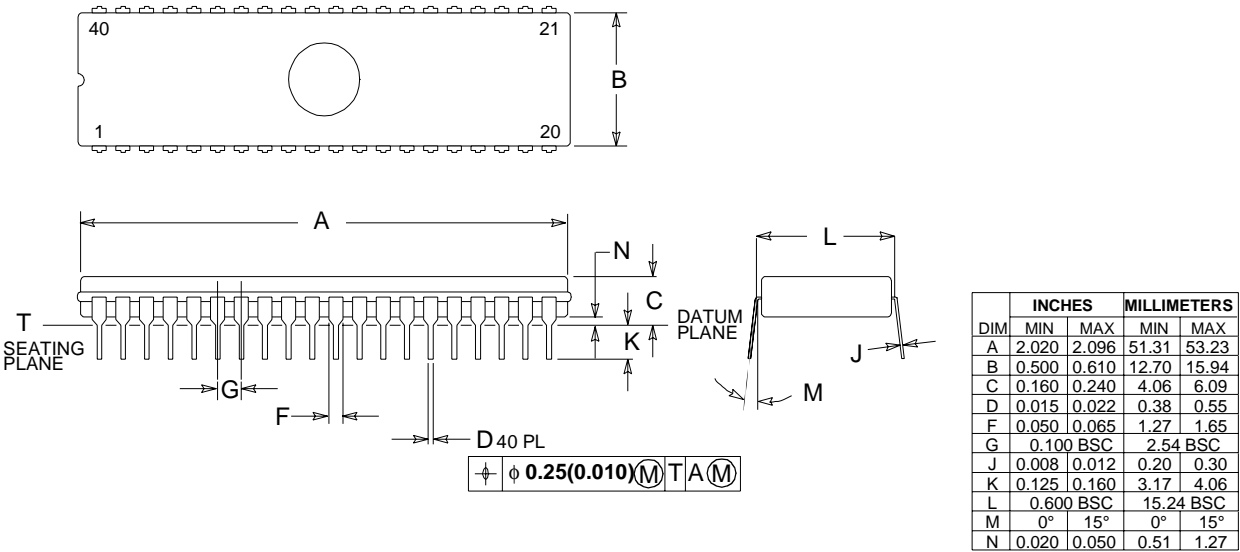
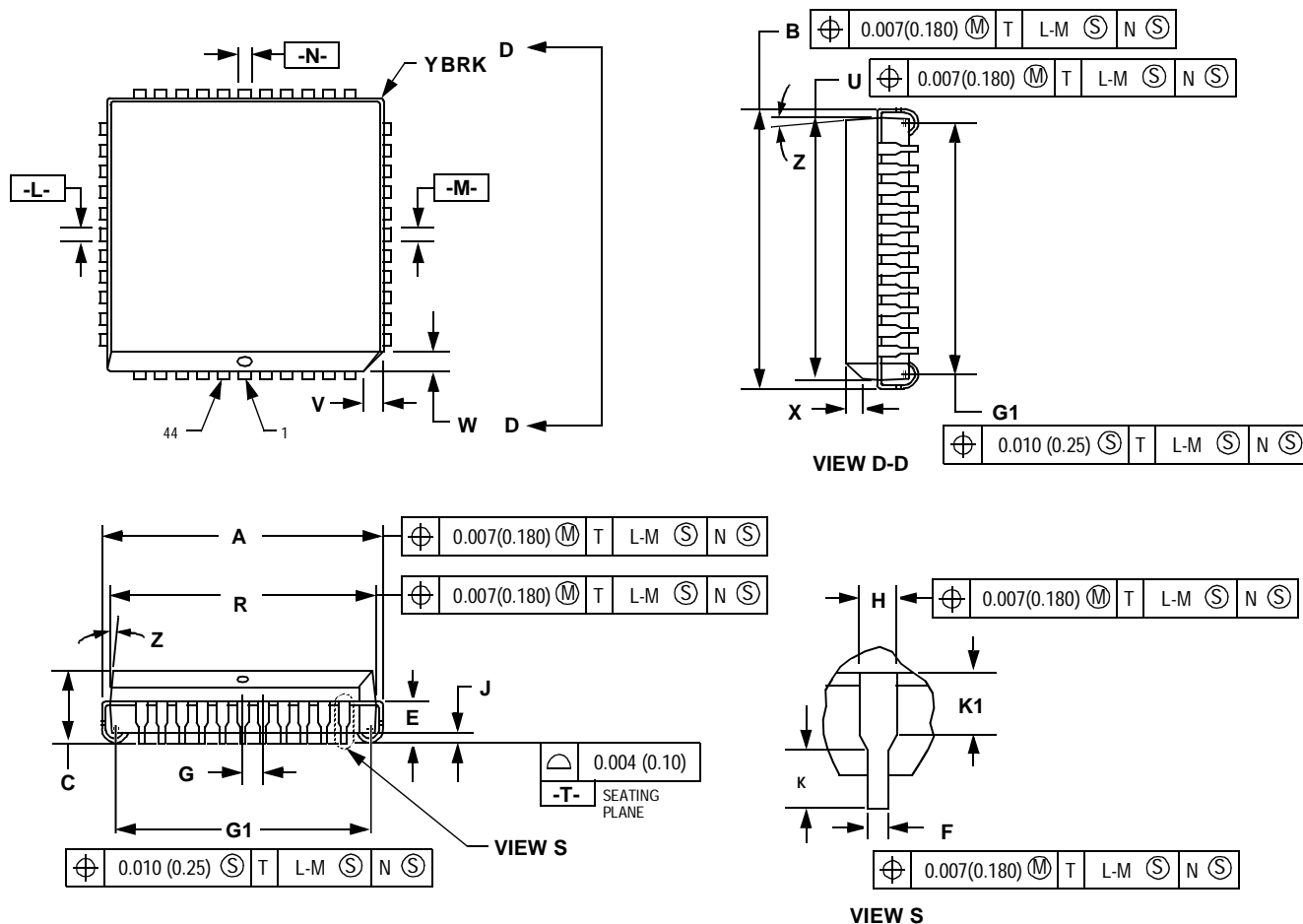


Figure 14-2. MC68HC705C8AS Package Dimensions (Case #734A)

Mechanical Specifications

14.5 44-Lead Plastic-Leaded Chip Carrier (PLCC)



NOTES:

1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOLDERS EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSION R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF THE MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940198). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

Figure 14-3. MC68HC705C8AFN Package Dimensions (Case #777)

MC68HSC705C8A

Diagram Number ⁽¹⁾	Characteristic ⁽²⁾	Symbol	Min	Max	Unit
11	Data hold time (outputs) Master (after capture edge) Slave (after enable edge)	$t_{HO(M)}$ $t_{HO(S)}$	0.25 0	— —	$t_{CYC(M)}$ ns
12	Rise time ⁽⁷⁾ SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, SS)	t_{RM} t_{RS}	— —	100 2.0	ns μs
13	Fall time ⁽⁸⁾ SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, SS)	t_{FM} t_{FS}	— —	100 2.0	ns μs

1. Diagram numbers refer to dimensions in [Figure 13-8. SPI Master Timing](#) and [Figure 13-9. SPI Slave Timing](#).
2. $V_{DD} = 3.3 \text{ V} \pm 10\%$; $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted
3. Signal production depends on software.
4. Time to data active from high-impedance state
5. Hold time to high-impedance state
6. With 200 pF on all SPI pins
7. 20% of V_{DD} to 70% of V_{DD} ; $C_L = 200 \text{ pF}$
8. 70% of V_{DD} to 20% of V_{DD} ; $C_L = 200 \text{ pF}$





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