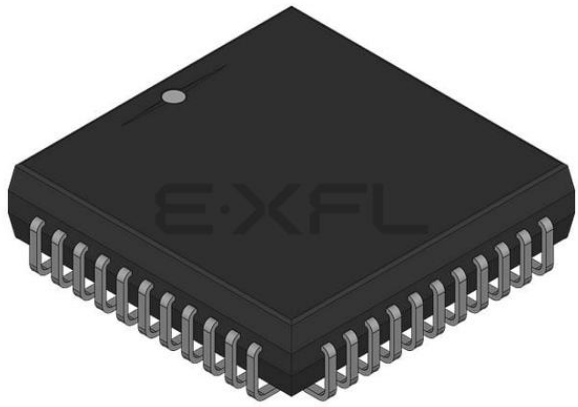

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc705c8afne

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 78.	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 81.	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Reset:	Unaffected by reset							
$0002	Port C Data Register (PORTC) See page 85.	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Unaffected by reset							
$0003	Port D Fixed Input Register (PORTD) See page 88.	Read:	PD7		SS	SCK	MOSI	MISO	TDO	RDI
		Write:								
		Reset:	Unaffected by reset							
$0004	Port A Data Direction Register (DDRA) See page 79.	Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Reset:	0	0	0	0	0	0	0	0
$0005	Port B Data Direction Register (DDRB) See page 82.	Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Reset:	0	0	0	0	0	0	0	0
$0006	Port C Data Direction (DDRC) See page 86.	Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Reset:	0	0	0	0	0	0	0	0
$0007	Unimplemented									
$0008	Unimplemented									
$0009	Unimplemented									

= Unimplemented U = Unaffected

Figure 2-2. I/O Register Summary (Sheet 1 of 4)

5.3.1 Power-On Reset (POR)

A positive transition on the V_{DD} pin generates a power-on reset (POR). The POR is strictly for the power-up condition and cannot be used to detect drops in power supply voltage.

A 4064 t_{CYC} (internal clock cycle) delay after the oscillator becomes active allows the clock generator to stabilize. If the $\overline{\text{RESET}}$ pin is at logic 0 at the end of 4064 t_{CYC}, the MCU remains in the reset condition until the signal on the $\overline{\text{RESET}}$ pin goes to logic 1.

5.3.2 External Reset

The minimum time required for the MCU to recognize a reset is 1 1/2 t_{CYC}. However, to guarantee that the MCU recognizes an external reset as an external reset and not as a COP or clock monitor reset, the $\overline{\text{RESET}}$ pin must be low for eight t_{CYC}. After six t_{CYC}, the input on the $\overline{\text{RESET}}$ pin is sampled. If the pin is still low, an external reset has occurred. If the input is high, then the MCU assumes that the reset was initiated internally by either the COP watchdog timer or by the clock monitor. This method of differentiating between external and internal reset conditions assumes that the $\overline{\text{RESET}}$ pin will rise to a logic 1 less than two t_{CYC} after its release and that an externally generated reset should stay active for at least eight t_{CYC}.

5.3.3 Programmable and Non-Programmable COP Watchdog Resets

A timeout of a COP watchdog generates a COP reset. A COP watchdog, once enabled, is part of a software error detection system and must be cleared periodically to start a new timeout period.

The MC68HC705C8A has two different COP watchdogs for compatibility with devices such as the MC68HC705C8 and the MC68HC05C4A:

1. Programmable COP watchdog reset
2. Non-programmable COP watchdog

One COP has four programmable timeout periods and the other has a fixed non-programmable timeout period.

When a port B pin is programmed as an output, reading the port bit reads the value of the data latch and not the voltage on the pin itself. When a port B pin is programmed as an input, reading the port bit reads the voltage level on the pin. The data latch can always be written, regardless of the state of its DDRB bit.

Table 7-2. Port B Pin Functions

DDRB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PORTB	
		Read/Write	Read	Write
0	Input, Hi-Z(1)	DDRB7–DDRB0	Pin	PB7–PB0(2)
1	Output	DDRB7–DDRB0	PB7–PB0	PB7–PB0

1. Hi-Z = high impedance
2. Writing affects data register but does not affect input.

NOTE: *To avoid excessive current draw, tie all unused input pins to V_{DD} or V_{SS}, or for I/O pins change to outputs by writing to DDRB in user code as early as possible.*

ICIE — Input Capture Interrupt Enable Bit

This read/write bit enables interrupts caused by an active signal on the TCAP pin. Reset clears the ICIE bit.

1 = Input capture interrupts enabled
0 = Input capture interrupts disabled

OCIE — Output Compare Interrupt Enable Bit

This read/write bit enables interrupts caused by an active signal on the TCMP pin. Reset clears the OCIE bit.

1 = Output compare interrupts enabled
0 = Output compare interrupts disabled

TOIE — Timer Overflow Interrupt Enable Bit

This read/write bit enables interrupts caused by a timer overflow. Reset clears the TOIE bit.

1 = Timer overflow interrupts enabled
0 = Timer overflow interrupts disabled

IEDG — Input Edge Bit

The state of this read/write bit determines whether a positive or negative transition on the TCAP pin triggers a transfer of the contents of the timer register to the input capture registers. Reset has no effect on the IEDG bit.

1 = Positive edge (low-to-high transition) triggers input capture
0 = Negative edge (high-to-low transition) triggers input capture

OLVL — Output Level Bit

The state of this read/write bit determines whether a logic 1 or a logic 0 appears on the TCMP pin when a successful output compare occurs. Reset clears the OLVL bit.

1 = TCMP goes high on output compare
0 = TCMP goes low on output compare

Bits 4–2 — Not used; these bits always read 0

10.5.2 Receiver

Figure 10-4 shows the structure of the SCI receiver. Refer to **Figure 10-3** for a summary of the SCI receiver I/O registers.

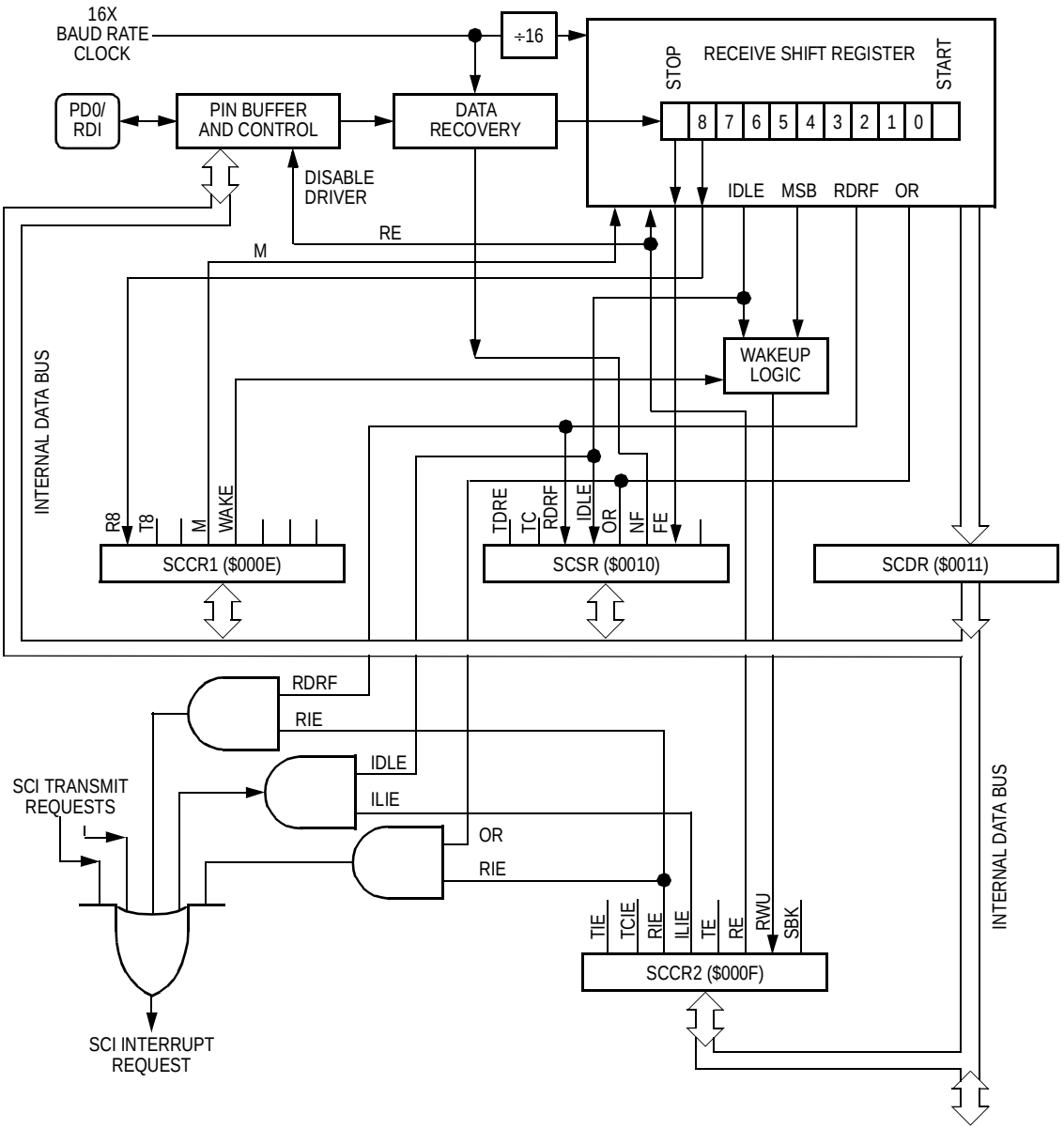

Figure 10-4. SCI Receiver

- Character Length — The receiver can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCCR1) determines character length. When receiving 9-bit data, bit R8 in SCCR1 is the ninth bit (bit 8).
- Character Reception — During reception, the receive shift register shifts characters in from the PD0/RDI pin. The SCI data register (SCDR) is the read-only buffer between the internal data bus and the receive shift register.

  After a complete character shifts into the receive shift register, the data portion of the character is transferred to the SCDR, setting the receive data register full (RDRF) flag. The RDRF flag can be used to generate an interrupt.
- Receiver Wakeup — So that the MCU can ignore transmissions intended only for other receivers in multiple-receiver systems, the MCU can be put into a standby state. Setting the receiver wakeup enable (RWU) bit in SCI control register 2 (SCCR2) puts the MCU into a standby state during which receiver interrupts are disabled.

  Either of two conditions on the PD0/RDI pin can bring the MCU out of the standby state:

  – Idle input line condition — If the PD0/RDI pin is at logic 1 long enough for 10 or 11 logic 1s to shift into the receive shift register, receiver interrupts are again enabled.

  – Address mark — If a logic 1 occurs in the most significant bit position of a received character, receiver interrupts are again enabled.

  The state of the WAKE bit in SCCR1 determines which of the two conditions wakes up the MCU.
- Receiver Noise Immunity — The data recovery logic samples each bit 16 times to identify and verify the start bit and to detect noise. Any conflict between noise detection samples sets the noise flag (NF) in the SCSR. The NF bit is set at the same time that the RDRF bit is set.

TCIE — Transmission Complete Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the TC bit becomes set. Reset clears the TCIE bit.

1 = TC interrupt requests enabled
0 = TC interrupt requests disabled

RIE — Receive Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the RDRF bit or the OR bit becomes set. Reset clears the RIE bit.

1 = RDRF interrupt requests enabled
0 = RDRF interrupt requests disabled

ILIE — Idle Line Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the IDLE bit becomes set. Reset clears the ILIE bit.

1 = IDLE interrupt requests enabled
0 = IDLE interrupt requests disabled

TE — Transmit Enable Bit

Setting this read/write bit begins the transmission by sending a preamble of 10 or 11 logic 1s from the transmit shift register to the PD1/TDO pin. Reset clears the TE bit.

1 = Transmission enabled
0 = Transmission disabled

RE — Receive Enable Bit

Setting this read/write bit enables the receiver. Clearing the RE bit disables the receiver and receiver interrupts but does not affect the receiver interrupt flags. Reset clears the RE bit.

1 = Receiver enabled
0 = Receiver disabled

RWU — Receiver Wakeup Enable Bit

This read/write bit puts the receiver in a standby state. Typically, data transmitted to the receiver clears the RWU bit and returns the receiver to normal operation. The WAKE bit in SCCR1 determines whether an

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	SPI Control Register (SPCR) See page 149.	Read:	SPIE	SPE		MSTR	CPOL	CPHA	SPR1	SPR0
		Write:								
		Reset:	0	0		0	U	U	U	U
$000B	SPI Status Register (SPSR) See page 151.	Read:	SPIF	WCOL		MODF				
		Write:								
		Reset:	0	0		0				
$000C	SPI Data Register (SPDR) See page 149.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	BIt 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented U = Unaffected

Figure 11-2. SPI I/O Register Summary

11.4 Operation

The master/slave SPI allows full-duplex, synchronous, serial communication between the microcontroller unit (MCU) and peripheral devices, including other MCUs. As the 8-bit shift register of a master SPI transmits each byte to another device, a byte from the receiving device enters the master SPI shift register. A clock signal from the master SPI synchronizes data transmission.

Only a master SPI can initiate transmissions. Software begins the transmission from a master SPI by writing to the SPI data register (SPDR). The SPDR does not buffer data being transmitted from the SPI. Data written to the SPDR goes directly into the shift register and begins the transmission immediately under the control of the serial clock. The transmission ends after eight cycles of the serial clock when the SPI flag (SPIF) becomes set. At the same time that SPIF becomes set, the data shifted into the master SPI from the receiving device transfers to the SPDR. The SPDR buffers data being received by the SPI. Before the master SPI sends the next byte, software must clear the SPIF bit by reading the SPSR and then accessing the SPDR.

11.9.3 SPI Status Register

The SPSR shown in **Figure 11-9** contains flags to signal these conditions:

- SPI transmission complete
- Write collision
- Mode fault

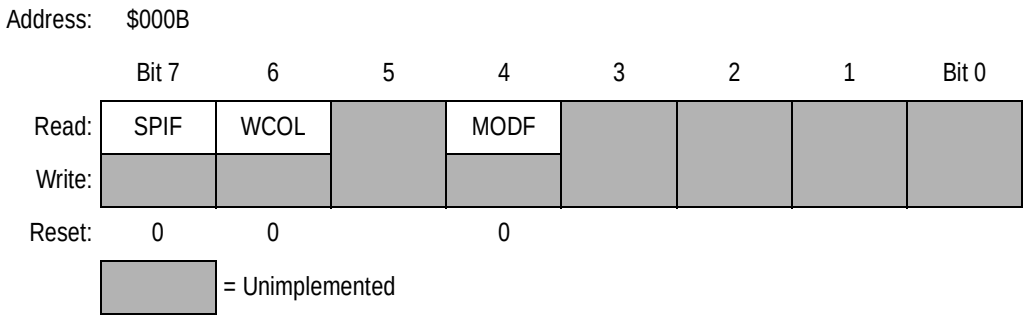

Figure 11-9. SPI Status Register (SPSR)

SPIF — SPI Flag

This clearable, read-only bit is set each time a byte shifts out of or into the shift register. SPIF generates an interrupt request if the SPIE bit in the SPCR is also set. Clear SPIF by reading the SPSR with SPIF set and then reading or writing the SPDR. Reset clears the SPIF bit.

1 = Transmission complete
0 = Transmission not complete

WCOL — Write Collision Bit

This clearable, read-only flag is set when software writes to the SPDR while a transmission is in progress. Clear the WCOL bit by reading the SPSR with WCOL set and then reading or writing the SPDR. Reset clears WCOL.

1 = Invalid write to SPDR
0 = No invalid write to SPDR

MODF — Mode Fault Bit

This clearable, read-only bit is set when a logic 0 occurs on the PD5/$\overline{SS}$ pin while the MSTR bit is set. MODF generates an interrupt request if the SPIE bit is also set. Clear the MODF bit by reading the SPSR with MODF set and then writing to the SPCR. Reset clears MODF.

1 = PD5/$\overline{SS}$ pulled low while MSTR bit set
0 = PD5/$\overline{SS}$ not pulled low while MSTR bit set

12.4.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 12-5. Control Instructions

Instruction	Mnemonic
Clear carry bit	CLC
Clear interrupt mask	CLI
No operation	NOP
Reset stack pointer	RSP
Return from interrupt	RTI
Return from subroutine	RTS
Set carry bit	SEC
Set interrupt mask	SEI
Stop oscillator and enable $\overline{\text{IRQ}}$ pin	STOP
Software interrupt	SWI
Transfer accumulator to index register	TAX
Transfer index register to accumulator	TXA
Stop CPU clock and enable interrupts	WAIT

13.3 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table here. Keep V_{In} and V_{Out} within the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{In}	V_{SS} –0.3 to V_{DD} +0.3	V
Programming voltage	V_{PP}	V_{DD} –0.3 to 16.0	
Bootstrap mode ($\overline{IRQ}$ pin only)	V_{In}	V_{SS} – 0.3 to 2 x V_{DD} + 0.3	V
Current drain per pin excluding V_{DD} and V_{SS}	I	25	mA
Storage temperature range	T_{STG}	–65 to +150	°C

1. Voltages referenced to V_{SS}

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***13.7 5.0-Volt DC Electrical Characteristics*** *and* ***13.8 3.3-Volt DC Electrical Characteristics*** *for guaranteed operating conditions.*

Diagram Number(1)	Characteristic(2)	Symbol	Min	Max	Unit
11	Data hold time (outputs) Master (after capture edge) Slave (after enable edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
12	Rise time(7) SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 50 2.0	 ns µs
13	Fall time(8) SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 50 2.0	 ns µs

1. Diagram numbers refer to dimensions in **Figure 13-8. SPI Master Timing** and **Figure 13-9. SPI Slave Timing**.
2. V_{DD} = 5 V ± 10%; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
3. Signal production depends on software.
4. Time to data active from high-impedance state
5. Hold time to high-impedance state
6. With 200 pF on all SPI pins.
7. 20% of V_{DD} to 70% of V_{DD}; C_L = 200 pF
8. 70% of V_{DD} to 20% of V_{DD}; C_L = 200 pF

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