Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	42-SDIP (0.600", 15.24mm)
Supplier Device Package	42-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705c8acbe

List of Sections

List of Sections

Section 6. Low-Power Modes

Section 7. Parallel Input/Output (I/O)

Section 15. Ordering Information

Appendix A. MC68HSC705C8A

Index

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001C	EPROM Programming Register (PROG) See page 109.	Read:	0	0	0	0	0	LAT	0	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001D	Programmable COP Reset Register (COPRST) See page 64.	Read:								
		Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	U	U	U	U	U	U	U	U
$001E	Programmable COP Control Register (COPCR) See page 64.	Read:	0	0	0	COPF	CME	PCOPE	CM1	CM0
		Write:								
		Reset:	0	0	0	U	0	0	0	0
$001F	Unimplemented									
$1FDF	Option Register (Option) See page 116.	Read:	RAM0	RAM1	0	0	SEC*		IRQ	0
		Write:								
		Reset:	0	0	0	0	*	U	1	0
$1FF0	Mask Option Register 1 (MOR1) See page 117.	Read:	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0/ COPC
		Write:								
		Reset:	Unaffected by reset							
$1FF1	Mask Option Register 2 (MOR2) See page 118.	Read:								NCOPE
		Write:								
		Reset:	Unaffected by reset							

*Implemented as an EPROM cell

= Unimplemented U = Unaffected

Figure 2-2. I/O Register Summary (Sheet 4 of 4)

4.3.3 Port B Interrupts

When these three conditions are true, a port B pin (PBx) acts as an external interrupt pin:

- The corresponding port B pullup bit (PBPUx) in mask option register 1 (MOR1) is programmed to a logic 1.
- The corresponding port B data direction bit (DDRBx) in data direction register B (DDRB) is a logic 0.
- The clear interrupt mask (CLI) instruction has cleared the I bit in the CCR.

MOR1 is an erasable, programmable read-only memory (EPROM) register that enables the port B pullup device. Data from MOR1 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin. See **9.5.2 Mask Option Register 1**.

Port B external interrupt pins can be falling-edge sensitive only or both falling-edge and low-level sensitive, depending on the state of the IRQ bit in the option register at location $1FDF.

When the IRQ bit is a logic 1, a falling edge or a low level on a port B external interrupt pin latches an external interrupt request. As long as any port B external interrupt pin is low, an external interrupt request is present, and the CPU continues to execute the interrupt service routine.

When the IRQ bit is a logic 0, a falling-edge only on a port B external interrupt pin latches an external interrupt request. A subsequent port B external interrupt request can be latched only after the voltage level of the previous port B external interrupt signal returns to a logic 1 and then falls again to a logic 0.

Figure 4-3 shows the port B input/output (I/O) logic.

4.3.4 Capture/Compare Timer Interrupts

Setting the I bit in the CCR disables all interrupts except for SWI.

4.3.5 SCI Interrupts

The serial communications interface (SCI) can generate these interrupts:

- Transmit data register empty interrupt
- Transmission complete interrupt
- Receive data register full interrupt
- Receiver overrun interrupt
- Receiver input idle interrupt

Setting the I bit in the CCR disables all SCI interrupts.

- **SCI Transmit Data Register Empty Interrupt** — The transmit data register empty bit (TDRE) indicates that the SCI data register is ready to receive a byte for transmission. TDRE becomes set when data in the SCI data register transfers to the transmit shift register. TDRE generates an interrupt request if the transmit interrupt enable bit (TIE) is set also.
- **SCI Transmission Complete Interrupt** — The transmission complete bit (TC) indicates the completion of an SCI transmission. TC becomes set when the TDRE bit becomes set and no data, preamble, or break character is being transmitted. TC generates an interrupt request if the transmission complete interrupt enable bit (TCIE) is set also.
- **SCI Receive Data Register Full Interrupt** — The receive data register full bit (RDRF) indicates that a byte is ready to be read in the SCI data register. RDRF becomes set when the data in the receive shift register transfers to the SCI data register. RDRF generates an interrupt request if the receive interrupt enable bit (RIE) is set also.

7.5.2 Data Direction Register C

The contents of data direction register C (DDRC) shown in **Figure 7-8** determine whether each port C pin is an input or an output. Writing a logic 1 to a DDRC bit enables the output buffer for the associated port C pin; a logic 0 disables the output buffer. A reset clears all DDRC bits, configuring all port C pins as inputs.

Address: $0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
Reset:	0	0	0	0	0	0	0	0

Figure 7-8. Data Direction Register C (DDRC)

DDRC7–DDRC0 — Port C Data Direction Bits

These read/write bits control port C data direction. Reset clears bits DDRC7–DDRC0.

1 = Corresponding port C pin configured as output
0 = Corresponding port C pin configured as input

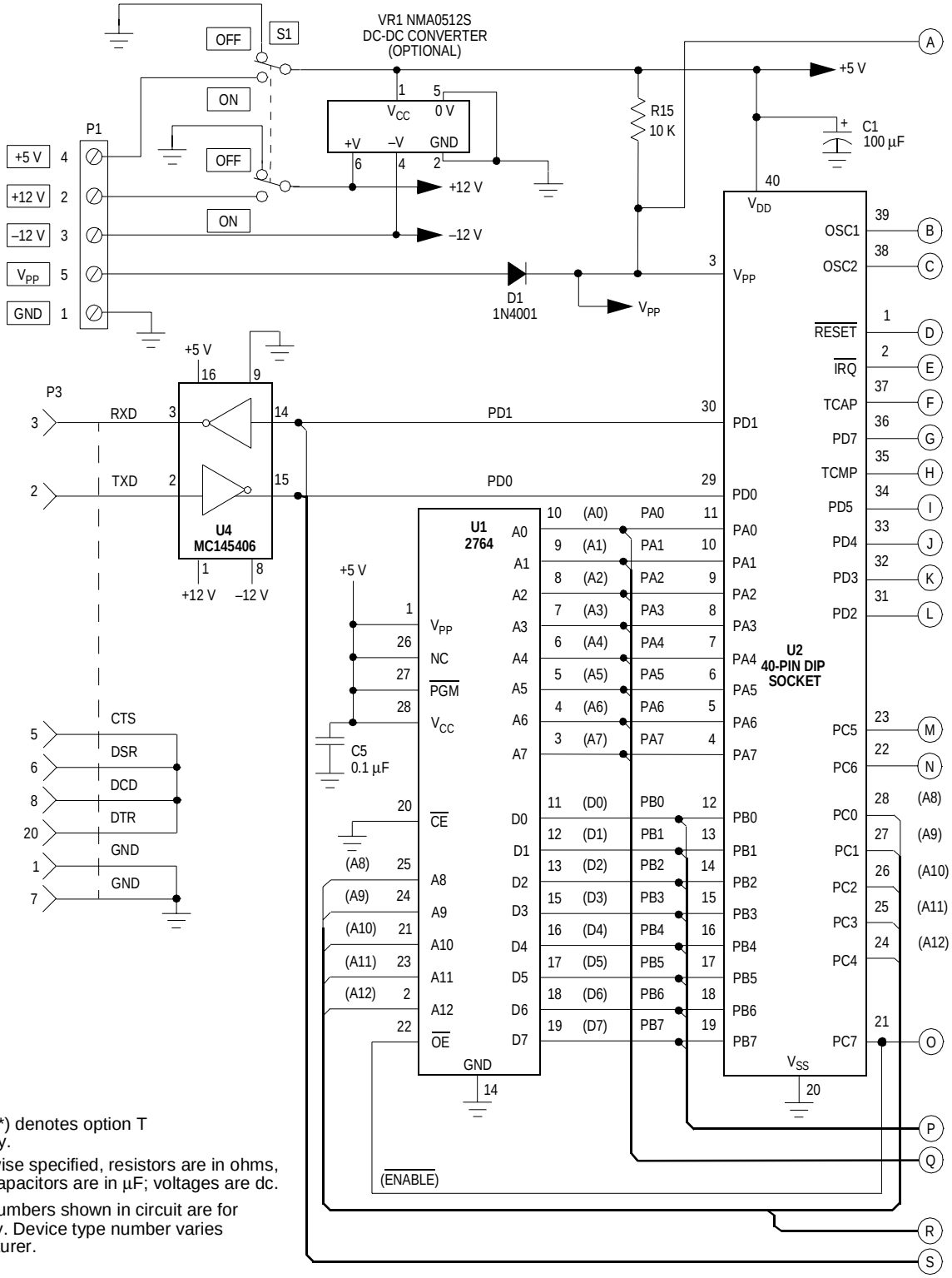
NOTE: *Avoid glitches on port C pins by writing to the port C data register before changing DDRC bits from logic 0 to logic 1.*

Section 9. EPROM/OTPROM (PROM)

9.1 Contents

9.2 Introduction

This section describes erasable, programmable read-only memory/one-time programmable read-only memory (EPROM/OTPROM (PROM)) programming.



Notes:

1. The asterisk (*) denotes option T command only.
2. Unless otherwise specified, resistors are in ohms, ±5% 1/4 W; capacitors are in µF; voltages are dc.
3. Device type numbers shown in circuit are for reference only. Device type number varies with manufacturer.

Figure 9-2. PROM Programming Circuit

To program the PROM MCU, the MCU is installed in the PCB, along with an EPROM device programmed with user code; the MCU is then subjected to a series of routines. The routines necessary to program, verify, and secure the PROM MCU are:

- Program and verify PROM
- Verify PROM contents only
- Secure PROM and verify
- Secure PROM and dump through the serial communications interface (SCI)

Other board routines available to the user are:

- Load program into random-access memory (RAM) and execute
- Execute program in RAM
- Dump PROM contents (binary upload)

The user first configures the MCU for the bootstrap mode of operations by installing a fabricated jumper across pins 1 and 2 of the board's mode select header, J1. Next, the board's mode switches (S3, S4, S5, and S6) are set to determine the routine to be executed after the next reset, as shown in **Table 9-2**.

Table 9-2. PROM Programming Routines

Routine	S3	S4	S5	S6
Program and verify PROM	Off	Off	Off	Off
Verify PROM contents only	Off	Off	On	Off
Secure PROM contents and verify	On	Off	On	Off
Secure PROM contents and dump	On	On	On	Off
Load program into RAM and execute	Off	On	Off	Off
Execute program in RAM	Off	Off	Off	On
Dump PROM contents	Off	On	On	Off

- Framing Errors — If the data recovery logic does not detect a logic 1 where the stop bit should be in an incoming character, it sets the framing error (FE) bit in the SCSR. The FE bit is set at the same time that the RDRF bit is set.
- Receiver Interrupts — These sources can generate SCI receiver interrupt requests:
  - Receive Data Register Full (RDRF) — The RDRF bit in the SCSR indicates that the receive shift register has transferred a character to the SCDR.
  - Receiver Overrun (OR) — The OR bit in the SCSR indicates that the receive shift register shifted in a new character before the previous character was read from the SCDR.
  - Idle Input (IDLE) — The IDLE bit in the SCSR indicates that 10 or 11 consecutive logic 1s shifted in from the PD0/RDI pin.

10.6 SCI I/O Registers

These I/O registers control and monitor SCI operation:

- SCI data register (SCDR)
- SCI control register 1 (SCCR1)
- SCI control register 2 (SCCR2)
- SCI status register (SCSR)

10.6.1 SCI Data Register

The SCI data register (SCDR) shown in **Figure 10-5** is the buffer for characters received and for characters transmitted.

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Unaffected by reset							

Figure 10-5. SCI Data Register (SCDR)

OR — Receiver Overrun Bit

This clearable, read-only bit is set if the SCDR is not read before the receive shift register receives the next word. OR generates an interrupt request if the RIE bit in SCCR2 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading the SCSR with OR set and then reading the SCDR. Reset clears the OR bit.

1 = Receiver shift register full and RDRF = 1
0 = No receiver overrun

NF — Receiver Noise Flag Bit

This clearable, read-only bit is set when noise is detected in data received in the SCI data register. Clear the NF bit by reading the SCSR and then reading the SCDR. Reset clears the NF bit.

1 = Noise detected in SCDR
0 = No noise detected in SCDR

FE — Receiver Framing Error Bit

This clearable, read-only flag is set when a logic 0 is located where a stop bit should be in the character shifted into the receive shift register. If the received word causes both a framing error and an overrun error, the OR bit is set and the FE bit is not set. Clear the FE bit by reading the SCSR and then reading the SCDR. Reset clears the FE bit.

1 = Framing error
0 = No framing error

– CPHA = 1 — A slave SPI can cause a write collision error by writing to the SPDR while receiving a transmission, that is, between the first active SCK edge and the end of the eighth SCK cycle. The error does not affect the transmission from the master SPI, but the byte that caused the error is lost.

11.7.3 Overrun Error

Failing to read the byte in the SPDR before a subsequent byte enters the shift register causes an overrun condition. In an overrun condition, all incoming data is lost until software clears SPIF. The overrun condition has no flag.

11.8 SPI Interrupts

The SPIF bit in the SPSR indicates a byte has shifted into or out of the SPDR. The SPIF bit is a source of SPI interrupt requests. The SPI interrupt enable bit (SPIE) in the SPCR is the local mask for SPIF interrupts.

The MODF bit in the SPSR indicates a mode error and is a source of SPI interrupt requests. The MODF bit is set when a logic 0 occurs on the PD5/$\overline{SS}$ pin while the MSTR bit is set. The SPI interrupt enable bit (SPIE) in the SPCR is the local mask for MODF interrupts.

11.9 SPI I/O Registers

These input/output (I/O) registers control and monitor SPI operation:

- SPI data register (SPDR)
- SPI control register (SPCR)
- SPI status register (SPSR)

SPI — SPI Enable Bit

This read/write bit enables the SPI. Reset clears the SPE bit.

1 = SPI enabled
0 = SPI disabled

MSTR — Master Bit

This read/write bit selects master mode operation or slave mode operation. Reset clears the MSTR bit.

1 = Master mode
0 = Slave mode

CPOL — Clock Polarity Bit

This read/write bit determines the logic state of the PD4/SCK pin between transmissions. To transmit data between SPIs, the SPIs must have identical CPOL bits. Reset has no effect on the CPOL bit.

1 = PD4/SCK pin at logic 1 between transmissions
0 = PD4/SCK pin at logic 0 between transmissions

CPHA — Clock Phase Bit

This read/write bit controls the timing relationship between the serial clock and SPI data. To transmit data between SPIs, the SPIs must have identical CPHA bits. When CPHA = 0, the PD5/$\overline{SS}$ pin of the slave SPI must be set to logic 1 between bytes. Reset has no effect on the CPHA bit.

1 = Edge following first active edge on PD4/SCK latches data
0 = First active edge on PD4/SCK latches data

SPR1 and SPR0 — SPI Clock Rate Bits

These read/write bits select the master mode serial clock rate, as shown in **Table 11-1**. The SPR1 and SPR0 bits of a slave SPI have no effect on the serial clock. Reset has no effect on SPR1 and SPR0.

Table 11-1. SPI Clock Rate Selection

SPR[1:0]	SPI Clock Rate
00	Internal Clock ÷ 2
01	Internal Clock ÷ 4
10	Internal Clock ÷ 16
11	Internal Clock ÷ 32

12.3.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

12.3.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

12.3.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address.

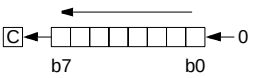
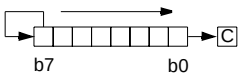
12.3.4 Extended

Extended instructions use three bytes and can access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Motorola assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

12.5 Instruction Set Summary

Table 12-6. Instruction Set Summary (Sheet 1 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3

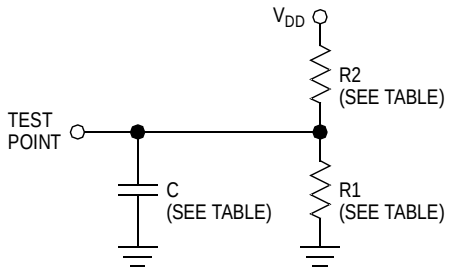
13.4 Operating Temperature Range

Rating(1)	Symbol	Value	Unit
Operating temperature range(2) MC68HC705C8ACB MC68HC705C8ACFB MC68HC705C8ACFS MC68HC705C8ACP MC68HC705C8ACFN MC68HC705C8ACFS	T_A	T_L to T_H – 40 to + 85	°C

1. Voltages referenced to V_{SS}
2. C = Extended temperature range (– 40°C to + 85°C)
   P = Plastic dual in-line package (PDIP)
   B = Plastic shrink dual in-line package (SDIP)
   S = Ceramic dual in-line package (cerdip)
   FN = Plastic-leaded chip carrier (PLCC)
   FB = Quad flat pack (QFP)
   FS = Ceramic-leaded chip carrier (CLCC)

13.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance Plastic dual in-line package (DIP) Ceramic dual in-line package (cerdip) Plastic leaded chip carrier (PLCC) Quad flat pack (QFP) Plastic shrink DIP (SDIP)	θ_{JA}	 60 50 70 95 60	°C/W



V_{DD} = 4.5 V

Pins	R1	R2	C
PA7–PA0 PB7–PB0 PC7–PC0 PD4–PD1	3.26 kΩ	2.38 kΩ	50 pF

V_{DD} = 3.0 V

Pins	R1	R2	C
PA7–PA0 PB7–PB0 PC7–PC0 PD4–PD1	10.91 kΩ	6.32 kΩ	50 pF
PD7, PD5, PD0	6 kΩ	6 kΩ	200 pF

Figure 13-1. Equivalent Test Load

13.9 5.0-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option	f_{OSC}	— dc	4.2 4.2	MHz
Internal operating frequency Crystal ($f_{OSC} \div 2$) External clock ($f_{OSC} \div 2$)	f_{OP}	— dc	2.1 2.1	MHz
Cycle time (see **Figure 13-7**)	t_{CYC}	480	—	ns
Crystal oscillator startup time (see **Figure 13-7**)	t_{OXOV}	—	100	ms
Stop recovery startup time (crystal oscillator) (see **Figure 13-6**)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ pulse width (see **Figure 13-7**)	t_{RL}	8	—	t_{CYC}
Timer Resolution[2] Input capture pulse width (see **Figure 13-5**) Input capture pulse period (see **Figure 13-5**)	t_{RESL} t_{TH}, t_{TL} t_{TLTL}	4.0 125 [3]	— — —	t_{CYC} ns t_{CYC}
Interrupt pulse width low (edge-triggered) (see **Figure 4-2. External Interrupt Timing**)	t_{ILIH}	125	—	ns
Interrupt pulse period (see **Figure 4-2. External Interrupt Timing**)	t_{ILIL}	[4]	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc; $T_A = T_L$ to T_H
2. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
3. The minimum period, t_{TLTL}, should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
4. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.