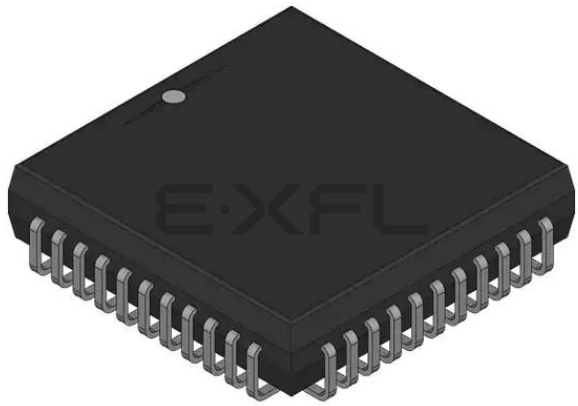

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc705c8acfner

1.2 Introduction

The MC68HC705C8A, an enhanced version of the MC68HC705C8, is a member of the low-cost, high-performance M68HC05 Family of 8-bit microcontroller units (MCU). The MC68HSC705C8A, introduced in **Appendix A. MC68HSC705C8A**, is an enhanced, high-speed version of the MC68HC705C8A. The M68HC05 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the M68HC05 central processor unit (CPU) and are available with a variety of subsystems, memory sizes and types, and package types.

1.3 Features

Features of the MC68HC705C8A include:

- M68HC05 central processor unit (CPU)
- On-chip oscillator with crystal/ceramic resonator
- Memory-mapped input/output (I/O)
- Selectable memory configurations
- Selectable programmable and/or non-programmable computer operating properly (COP) watchdog timers
- Selectable port B external interrupt capability
- Clock monitor
- High current drive on pin C7 (PC7)
- 24 bidirectional I/O lines and 7 input-only lines
- Serial communications interface (SCI) system
- Serial peripheral interface (SPI) system
- Bootstrap capability
- Power-saving stop, wait, and data-retention modes
- Single 3.0-volt to 5.5-volt supply (2-volt data-retention mode)
- Fully static operation

1.7.3.2 Ceramic Resonator

To reduce cost, use a ceramic resonator instead of a crystal. Use the circuit shown in **Figure 1-9** for a 2-pin ceramic resonator or the circuit shown in **Figure 1-10** for a 3-pin ceramic resonator, and follow the resonator manufacturer's recommendations.

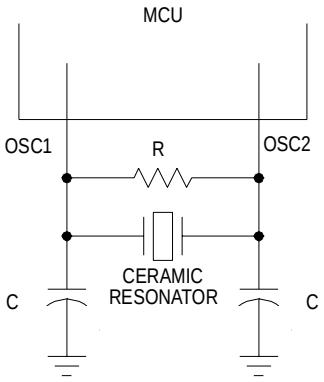


Figure 1-9. 2-Pin Ceramic Resonator Connections

The external component values required for maximum stability and reliable starting depend upon the resonator parameters. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. To minimize output distortion, mount the resonator and capacitors as close as possible to the pins.

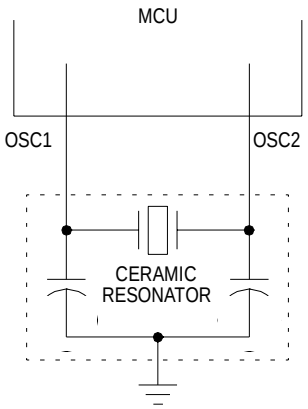


Figure 1-10. 3-Pin Ceramic Resonator Connections

NOTE: *The bus frequency (f_{OP}) is one-half the external or crystal frequency (f_{OSC}), while the processor clock cycle (t_{CYC}) is two times the f_{OSC} period.*

General Description

4.3.2 External Interrupt ($\overline{IRQ}$)

An interrupt signal on the $\overline{IRQ}$ pin latches an external interrupt request. After completing the current instruction, the CPU tests these bits:

- IRQ latch
- I bit in the CCR

Setting the I bit in the CCR disables external interrupts.

If the IRQ latch is set and the I bit is clear, the CPU then begins the interrupt sequence. The CPU clears the IRQ latch while it fetches the interrupt vector, so that another external interrupt request can be latched during the interrupt service routine. As soon as the I bit is cleared during the return-from-interrupt (RTI) instruction, the CPU can recognize the new interrupt request. **Figure 4-1** shows the logic for external interrupts.

Figure 4-1 shows an external interrupt functional diagram. **Figure 4-2** shows an external interrupt timing diagram for the interrupt line. The timing diagram illustrates two treatments of the interrupt line to the processor.

1. Two single pulses on the interrupt line are spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service.

   Once a pulse occurs, the next pulse normally should not occur until an RTI occurs. This time (t_{ILIL}) is obtained by adding 19 instruction cycles to the total number of cycles needed to complete the service routine (not including the RTI instruction).

2. Many interrupt lines are “wire-ORed” to the $\overline{IRQ}$ line. If the interrupt line remains low after servicing an interrupt, then the CPU continues to recognize an interrupt.

NOTE: *The internal interrupt latch is cleared in the first part of the interrupt service routine. Therefore, a new external interrupt pulse could be latched and serviced as soon as the I bit is cleared.*

If the $\overline{IRQ}$ pin is not in use, connect it to the V_{DD} pin.

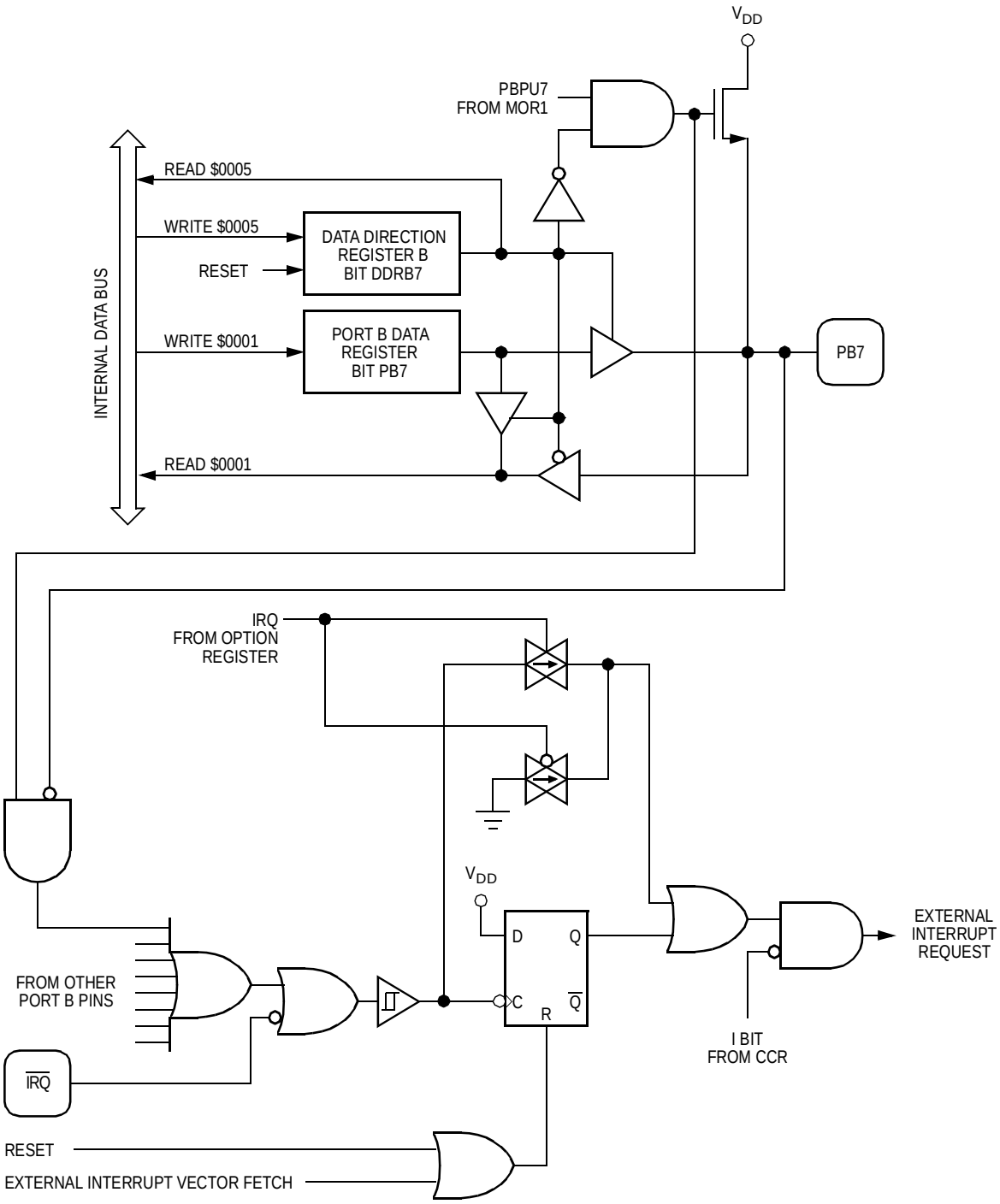


Figure 4-3. Port B I/O Logic

Section 6. Low-Power Modes

6.1 Contents

6.2 Introduction

This section describes the three low-power modes:

- Stop mode
- Wait mode
- Data-retention mode

6.3 Stop Mode

The STOP instruction places the microcontroller unit (MCU) in its lowest power consumption mode. In stop mode, the internal oscillator is turned off, halting all internal processing including timer, serial communications interface (SCI), and master mode serial peripheral interface (SPI) operation. See **Figure 6-1**.

6.3.4 Non-Programmable COP Watchdog in Stop Mode

The STOP instruction has these effects on the non-programmable COP watchdog:

- Turns off the oscillator and the COP watchdog counter
- Clears the COP watchdog counter

If the $\overline{\text{RESET}}$ pin brings the MCU out of stop mode, the COP watchdog begins counting immediately. The reset function clears the COP counter again after the 4064-t_{CYC} clock stabilization delay.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of stop mode, the COP watchdog begins counting immediately. The IRQ function does not clear the COP counter again after the 4064-t_{CYC} clock stabilization delay. See **Figure 6-3**.

NOTE: *If the clock monitor is enabled (CME = 1), the STOP instruction causes it to time out and reset the MCU.*

6.4 Wait Mode

The WAIT instruction places the MCU in an intermediate power consumption mode. All central processor unit (CPU) activity is suspended, but the oscillator, capture/compare timer, SCI, and SPI remain active. Any interrupt or reset brings the MCU out of wait mode. See **Figure 6-1**.

The WAIT instruction has these effects on the CPU:

- Clears the I bit in the condition code register, enabling interrupts
- Stops the CPU clock, but allows the internal clock to drive the capture/compare timer, SCI, and SPI

The WAIT instruction does not affect any other registers or I/O lines. The capture/compare timer, SCI, and SPI can be enabled to allow a periodic exit from wait mode.

7.5 Port C

Port C is an 8-bit, general-purpose, bidirectional I/O port. PC7 has a high current sink and source capability.

7.5.1 Port C Data Register

The port C data register (PORTC) shown in **Figure 7-7** contains a data latch for each of the eight port C pins. When a port C pin is programmed to be an output, the state of its data register bit determines the state of the output pin. When a port C pin is programmed to be an input, reading the port C data register returns the logic state of the pin.

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Reset:	Unaffected by reset							

Figure 7-7. Port C Data Register (PORTC)

PC7–PC0 — Port C Data Bits

These read/write bits are software programmable. Data direction of each bit is under the control of the corresponding bit in data direction register C. PC7 has a high current sink and source capability. Reset has no effect on port C data.

No LED is illuminated during this routine. Further, the end of the routine does not mean that the SEC bit was verified. To ensure that security is properly enabled, attempt to perform another verify routine. If the green LED does not light, the PROM has been secured properly.

9.4.6 Load Program into RAM and Execute

In the load program in RAM and execute routine, user programs are loaded via the SCI port and then executed. Data is loaded sequentially starting at address $0050. After the last byte is loaded, control is transferred to the RAM program starting at $0051. The first byte loaded is the count of the total number of bytes in the program plus the count byte. The program starts at location $0051 in RAM. During initialization, the SCI is configured for eight data bits and one stop bit. The baud rate is 4800 with a 2-MHz crystal or 9600 with a 4-MHz crystal.

To load a program into RAM and execute it, take these steps:

1. Set switch 1 in the ON position (restores V_{DD}).
2. Connect V_{PP} to V_{DD}.
3. Set switches S3, S5, and S6 in the OFF position.
4. Set switch S4 in the ON position.
5. Set switch 2 in the OUT position (routine is activated).

The downloaded program starts executing as soon as the last byte is received by the SCI.

Execution of the routine can be held off by setting the byte count in the count byte (the first byte loaded) to a value greater than the number of bytes to be loaded. After loading the last byte, the firmware waits for more data. Program execution does not begin. At this point, placing switch 2 in the RESET position resets the MCU with the RAM data intact. Any other routine can be entered, including the one to execute the program in RAM, simply by setting switches S3–S6 as necessary to select the desired routine, then setting switch 2 in the OUT position.

9.4.7 Execute Program in RAM

This routine allows the MCU to transfer control to a program previously loaded in RAM. This program is executed once bootstrap mode is entered, if switch S6 is in the ON position and switch 2 is in the OUT position, without any firmware initialization. The program must start at location $0051 to be compatible with the load program in RAM routine.

To run the execute program in RAM routine, take these steps:

1. Set switch 1 in the ON position (restores V_{DD}).
2. Connect V_{PP} to V_{DD}.
3. Set switch S6 in the OFF position.
4. Switches S3, S4, and S5 can be in either position.
5. Set switch 2 in the OUT position (routine is activated).

NOTE: *The non-programmable watchdog COP is disabled in bootloader mode, even if the NCOPE bit is programmed.*

9.4.8 Dump PROM Contents

In the dump PROM contents routine, the PROM contents are dumped sequentially to the SCI output, provided the PROM has not been secured. The first location sent is $0020 and the last location sent is $1FFF. Unused locations are skipped so that no gaps exist in the data stream. The external memory address lines indicate the current location being sent. Data is sent with eight data bits and one stop bit at 4800 baud with a 2-MHz crystal or 9600 baud with a 4-MHz crystal.

To run the dump PROM contents routine, take these steps:

1. Set switch 1 in the ON position (restores V_{DD}).
2. Connect V_{PP} to V_{DD}.
3. Set switches S3 and S6 in the OFF position.
4. Set switches S4 and S5 in the ON position.
5. Set switch 2 in the OUT position (routine is activated).
6. Once PROM dumping is complete, set switch 2 in the RESET position.

10.5.2 Receiver

Figure 10-4 shows the structure of the SCI receiver. Refer to **Figure 10-3** for a summary of the SCI receiver I/O registers.

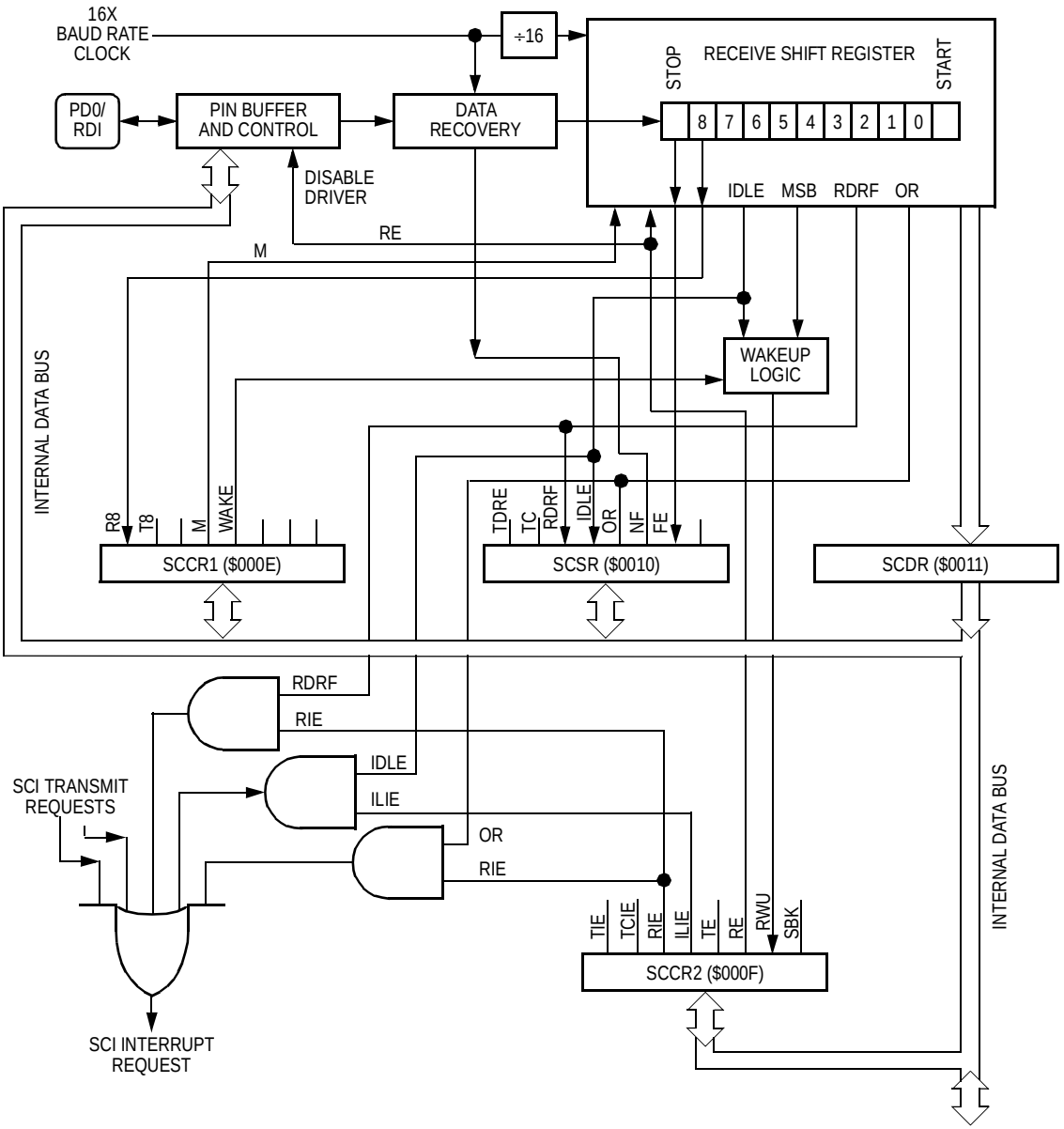


Figure 10-4. SCI Receiver

OR — Receiver Overrun Bit

This clearable, read-only bit is set if the SCDR is not read before the receive shift register receives the next word. OR generates an interrupt request if the RIE bit in SCCR2 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading the SCSR with OR set and then reading the SCDR. Reset clears the OR bit.

1 = Receiver shift register full and RDRF = 1
0 = No receiver overrun

NF — Receiver Noise Flag Bit

This clearable, read-only bit is set when noise is detected in data received in the SCI data register. Clear the NF bit by reading the SCSR and then reading the SCDR. Reset clears the NF bit.

1 = Noise detected in SCDR
0 = No noise detected in SCDR

FE — Receiver Framing Error Bit

This clearable, read-only flag is set when a logic 0 is located where a stop bit should be in the character shifted into the receive shift register. If the received word causes both a framing error and an overrun error, the OR bit is set and the FE bit is not set. Clear the FE bit by reading the SCSR and then reading the SCDR. Reset clears the FE bit.

1 = Framing error
0 = No framing error

SCR2–SCR0 — SCI Baud Rate Select Bits

These read/write bits select the SCI baud rate, as shown in Table 10-2. Reset has no effect on the SCR2–SCR0 bits.

Table 10-2. Baud Rate Selection

SCR[2:1:0]	SCI Baud Rate (Baud)
000	Prescaled clock ÷ 1
001	Prescaled clock ÷ 2
010	Prescaled clock ÷ 4
011	Prescaled clock ÷ 8
100	Prescaled clock ÷ 16
101	Prescaled clock ÷ 32
110	Prescaled clock ÷ 64
111	Prescaled clock ÷ 128

Table 10-3 shows all possible SCI baud rates derived from crystal frequencies of 2 MHz, 4 MHz, and 4.194304 MHz.

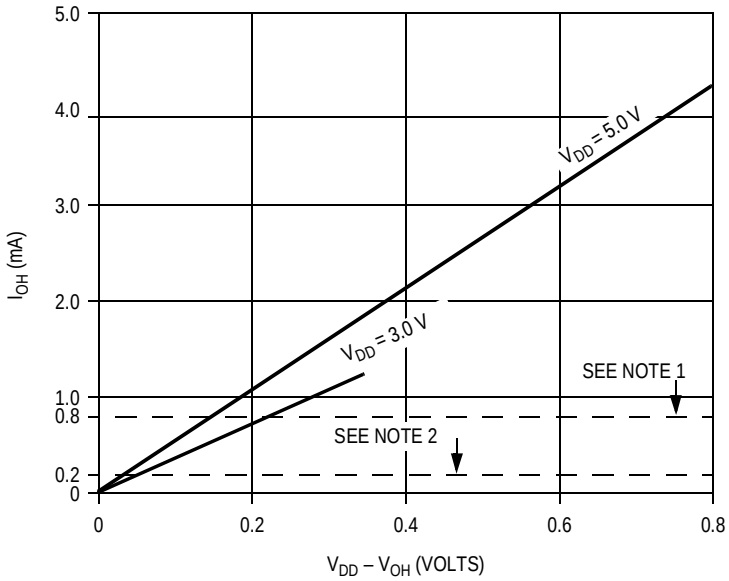
Table 12-6. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2

13.8 3.3-Volt DC Electrical Characteristics

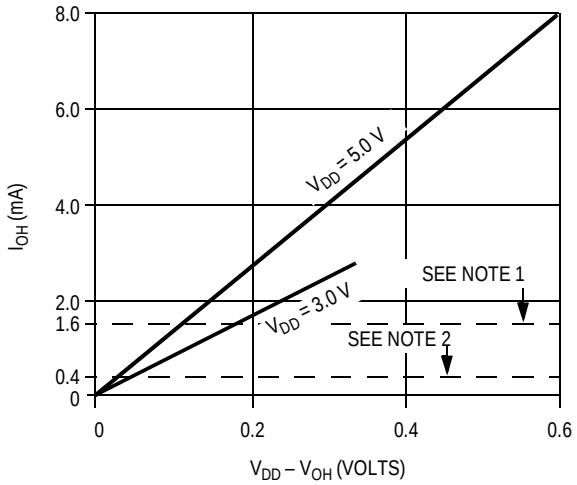
Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage, $I_{Load} \leq 10.0\ \mu A$	V_{OL} V_{OH}	— $V_{DD} - 0.1$	— —	0.1 —	V
Output high voltage I_{Load} = –0.2 mA PA7–PA0, PB7–PB0, PC6–PC0, TCMP (see **Figure 13-2**) I_{Load} = –0.4 mA PD4–PD1 (see **Figure 13-3**) I_{Load} = –1.5 mA PC7	V_{OH}	$V_{DD} - 0.3$	— — —	— — —	V
Output low voltage (see **Figure 13-4**) I_{Load} = 0.4 mA PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1 I_{Load} = 6.0 mA PC7	V_{OL}	— —	— —	0.3 0.3	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSCI	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
Data-retention mode (0°C to 70°C)	V_{RM}	2.0	—	—	V
Supply current[3] Run[4] Wait[5] Stop[6]	I_{DD}	— — —	1.53 0.711 2.0	3.0 1.0 20	mA mA µA
I/O ports hi-z leakage current PA7–PA0, PB7–PB0, PC7–PC0, PD4–PD1, PD7, $\overline{RESET}$	I_{IL}	—	—	± 10	µA
Input current $\overline{IRQ}$, TCAP, OSC1, PD5, PD0	I_{In}	—	—	± 1	µA

1. V_{DD} = 3.3 V ± 10%; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only.
3. I_{DD} measured with port B pullup devices disabled.
4. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. OSC2 capacitance linearly affects run I_{DD}.
5. Wait I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects wait I_{DD}.
6. Stop I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V; $V_{IH} = V_{DD} - 0.2$ V.



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 800 mV @ I_{OH} = –0.8 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 300 mV @ I_{OH} = –0.2 mA.

(a) V_{OH} versus I_{OH} for Ports A, B, PC6–PC0, and TCMP

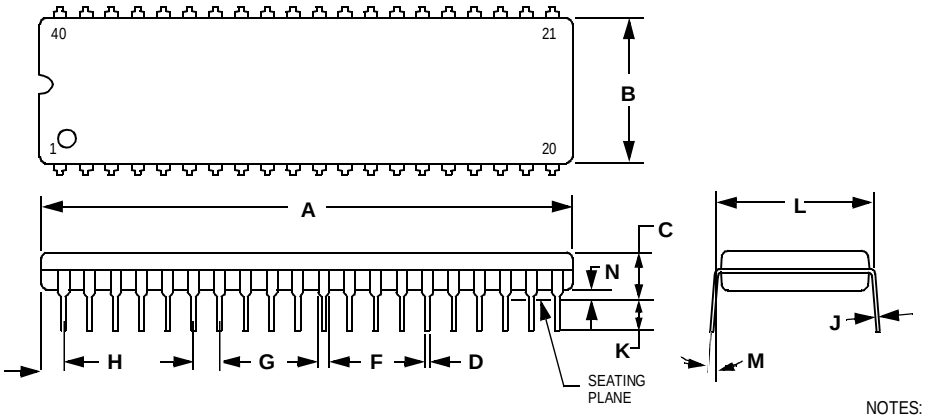


Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 800 mV @ I_{OH} = –1.6 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 300 mV @ I_{OH} = –0.4 mA.

(b) V_{OH} versus I_{OH} for PD4–PD1

Figure 13-2. Typical Voltage Compared to Current

14.3 40-Pin Plastic Dual In-Line Package (PDIP)

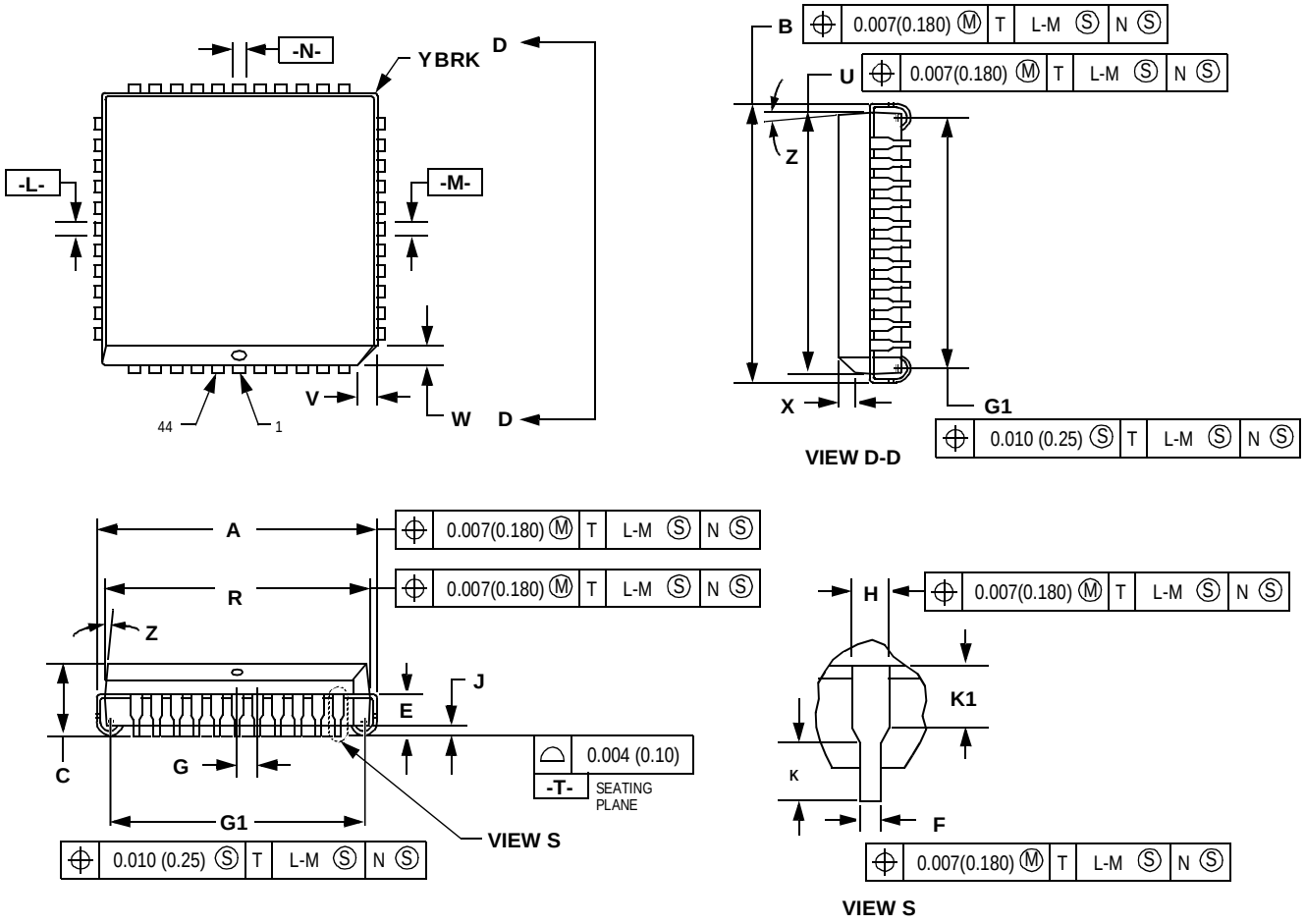


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	1°	0°	1°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITION TOLERANCE OF LEADS (D), SHALL BEWITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITIONS, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

Figure 14-1. MC68HC705C8AP Package Dimensions (Case #711)

14.5 44-Lead Plastic-Leaded Chip Carrier (PLCC)



NOTES:
1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOLDERS EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSION R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF THE MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMINSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTUSION(S) SHALL NOT CAUSE THE H DIMINSION TO BE GREATER THAN 0.037 (0.940198). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMINISION TO SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

Figure 14-3. MC68HC705C8AFN Package Dimensions (Case #777)

Mechanical Specifications

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