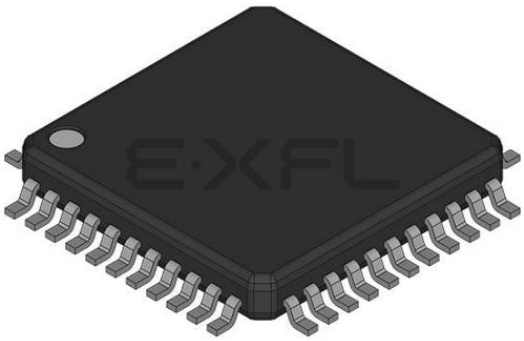

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | HC05 |
| Core Size | 8-Bit |
| Speed | 2.1MHz |
| Connectivity | SCI, SPI |
| Peripherals | POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 304 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc705c8acpbe |

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## Appendix A. MC68HSC705C8A

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### 3.3.3 Stack Pointer

The stack pointer (SP) shown in **Figure 3-4** is a 13-bit register that contains the address of the next free location on the stack. During a reset or after the reset stack pointer (RSP) instruction, the stack pointer initializes to $00FF. The address in the stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

The seven most significant bits of the stack pointer are fixed permanently at 0000011, so the stack pointer produces addresses from $00C0 to $00FF. If subroutines and interrupts use more than 64 stack locations, the stack pointer wraps around to address $00FF and begins writing over the previously stored data. A subroutine uses two stack locations. An interrupt uses five locations.

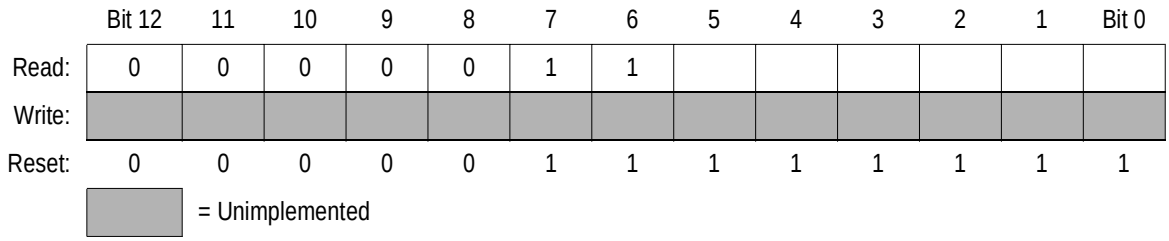


**Figure 3-4. Stack Pointer (SP)**

### 3.3.4 Program Counter

The program counter (PC) shown in **Figure 3-5** is a 13-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the address in the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

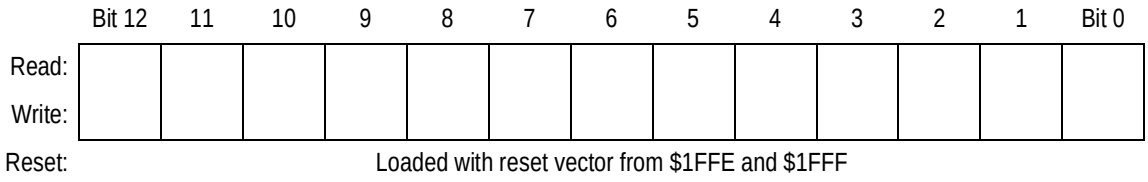


**Figure 3-5. Program Counter (PC)**

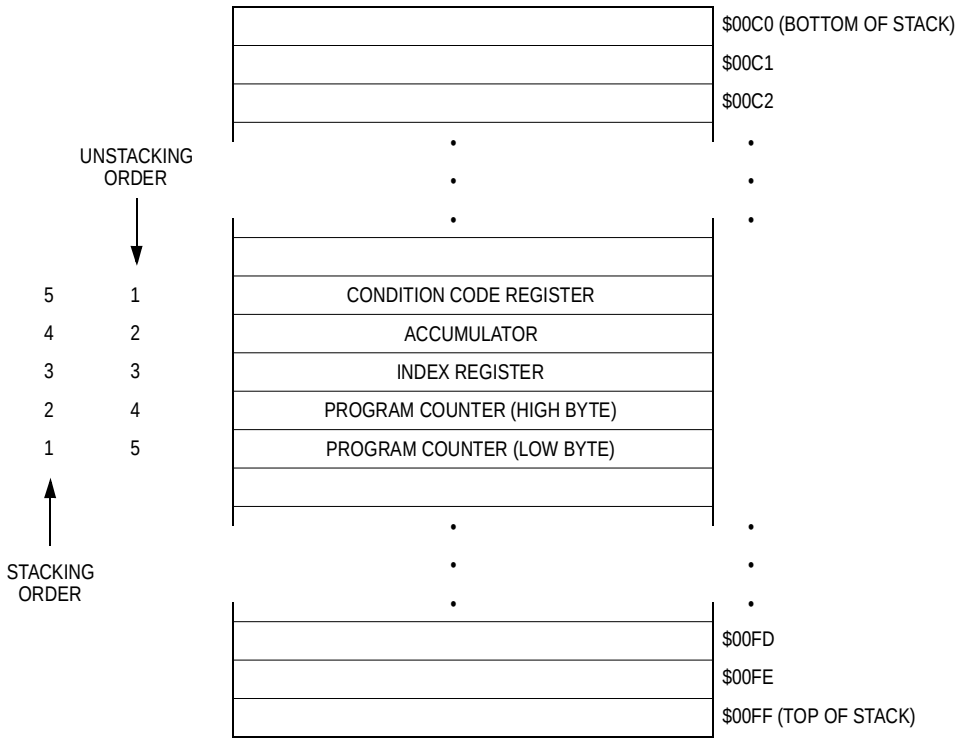


**Figure 4-4. Interrupt Stacking Order**

***NOTE:*** *If more than one interrupt request is pending, the CPU fetches the vector of the higher priority interrupt first. A higher priority interrupt does not interrupt a lower priority interrupt service routine unless the lower priority interrupt service routine clears the I bit. See **Table 4-1** for a priority listing.*

**Figure 4-5** shows the sequence of events caused by an interrupt.

**Table 5-1. Programmable COP Timeout Period Selection**

| CM1:CM0 | COP Timeout Rate | Programmable COP Timeout Period | | | |
|---|---|---|---|---|---|
| | | $f_{OSC}$ = 4.0 MHz<br>$f_{OP}$ = 2.0 MHz | $f_{OSC}$ = 3.5795 MHz<br>$f_{OP}$ = 1.7897 MHz | $f_{OSC}$ = 2.0 MHz<br>$f_{OP}$ = 1.0 MHz | $f_{OSC}$ = 1.0 MHz<br>$f_{OP}$ = 0.5 MHz |
| 00 | $f_{OP} \div 2^{15}$ | 16.38 ms | 18.31 ms | 32.77 ms | 65.54 ms |
| 01 | $f_{OP} \div 2^{17}$ | 65.54 ms | 73.24 ms | 131.07 ms | 262.14 ms |
| 10 | $f_{OP} \div 2^{19}$ | 262.14 ms | 292.95 ms | 524.29 ms | 1.048 s |
| 11 | $f_{OP} \div 2^{21}$ | 1.048 s | 1.172 s | 2.097 s | 4.194 s |

#### *5.3.3.2 Non-Programmable COP Watchdog*

A timeout of the 18-stage ripple counter in the non-programmable COP watchdog generates a reset. The timeout period is 65.536 ms when $f_{OSC}$ = 4 MHz. The timeout period for the non-programmable COP timer is a direct function of the crystal frequency. The equation is:

$$\text{Timeout period} = \frac{262{,}144}{f_{OSC}}$$

Two memory locations control operation of the non-programmable COP watchdog:

1. Non-programmable COP enable bit (NCOPE) in mask option register 2 (MOR2)

   Programming the NCOPE bit in MOR2 to a logic 1 enables the non-programmable COP watchdog. See **9.5.3 Mask Option Register 2**.

***NOTE:*** *Writing a logic 1 to the programmable COP enable bit (PCOPE) in the COP control register enables the programmable COP watchdog. Setting the PCOPE bit while the NCOPE bit is programmed to logic 1 enables both COP watchdogs to operate at the same time.*

## 7.3 Port A

Port A is an 8-bit, general-purpose, bidirectional input/output (I/O) port.

### 7.3.1 Port A Data Register

The port A data register (PORTA) shown in **Figure 7-1** contains a data latch for each of the eight port A pins. When a port A pin is programmed to be an output, the state of its data register bit determines the state of the output pin. When a port A pin is programmed to be an input, reading the port A data register returns the logic state of the pin.

Address: $0000

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read:<br>Write: | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Reset: | Unaffected by reset | | | | | | | |

**Figure 7-1. Port A Data Register (PORTA)**

PA7–PA0 — Port A Data Bits

These read/write bits are software programmable. Data direction of each bit is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

## 7.6 Port D

Port D is a 7-bit, special-purpose, input-only port that has no data register. Reading address $0003 returns the logic states of the port D pins.

Port D shares pins PD5–PD2 with the serial peripheral interface module (SPI). When the SPI is enabled, PD5–PD2 read as logic 0s. When the SPI is disabled, reading address $0003 returns the logic states of the PD5–PD2 pins.

Port D shares pins PD1 and PD0 with the SCI module. When the SCI is enabled, PD1 and PD0 read as logic 0s. When the SCI is disabled, reading address $0003 returns the logic states of the PD1 and PD0 pins.

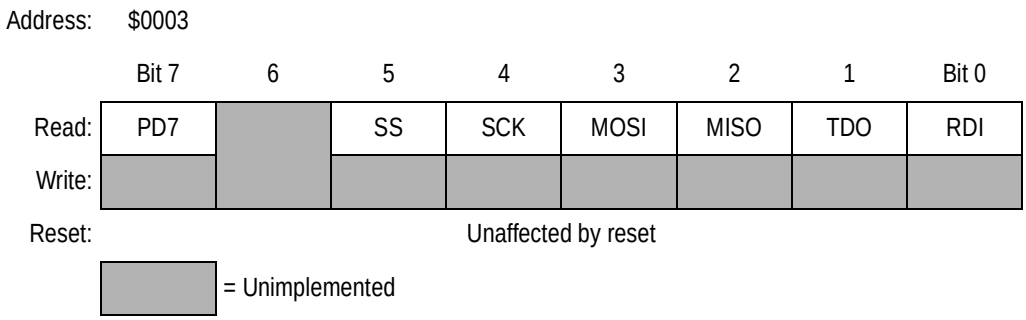


**Figure 7-10. Port D Fixed Input Register (PORTD)**

Because of the 16-bit timer architecture, the I/O registers for the input capture and output compare functions are pairs of 8-bit registers.

Because the counter is 16 bits long and preceded by a fixed divide-by-four prescaler, the counter rolls over every 262,144 internal clock cycles. Timer resolution with a 4-MHz crystal is 2 µs.

### 8.3.1 Input Capture

The input capture function can record the time at which an external event occurs. When the input capture circuitry detects an active edge on the input capture pin (TCAP), it latches the contents of the timer registers into the input capture registers. The polarity of the active edge is programmable.

Latching values into the input capture registers at successive edges of the same polarity measures the period of the input signal on the TCAP pin. Latching the counter values at successive edges of opposite polarity measures the pulse width of the signal. **Figure 8-3** shows the logic of the input capture function.

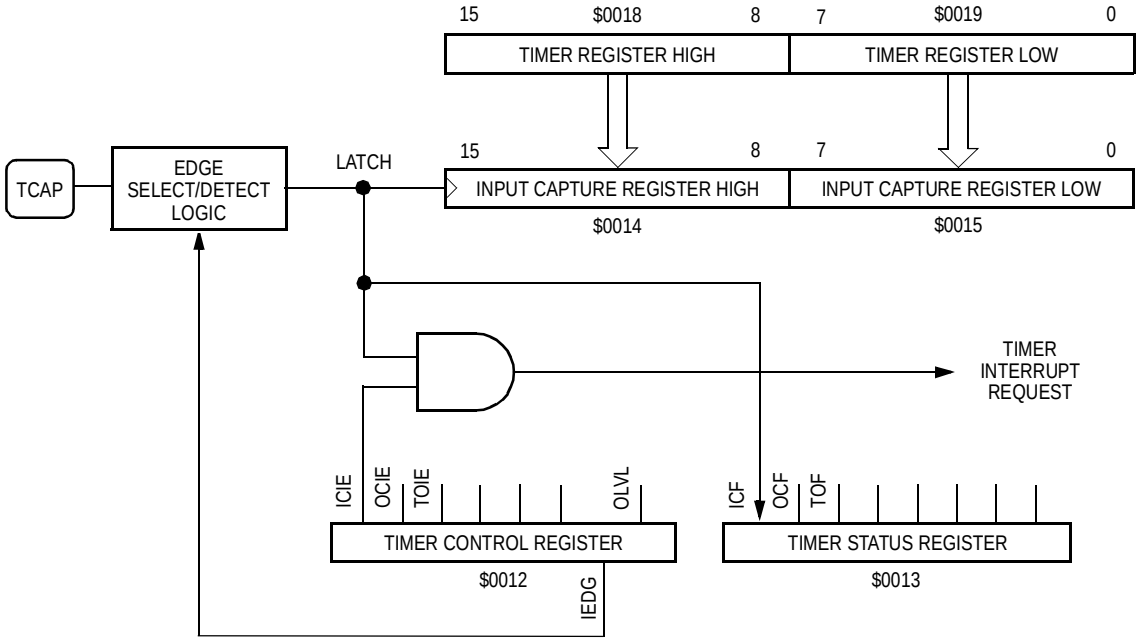


**Figure 8-3. Input Capture Operation**

### 8.3.2 Output Compare

The output compare function can generate an output signal when the 16-bit counter reaches a selected value. Software writes the selected value into the output compare registers. On every fourth internal clock cycle the output compare circuitry compares the value of the counter to the value written in the output compare registers. When a match occurs, the timer transfers the programmable output level bit (OLVL) from the timer control register to the output compare pin (TCMP).

Software can use the output compare register to measure time periods, to generate timing delays, or to generate a pulse of specific duration or a pulse train of specific frequency and duty cycle on the TCMP pin. **Figure 8-4** shows the logic of the output compare function.

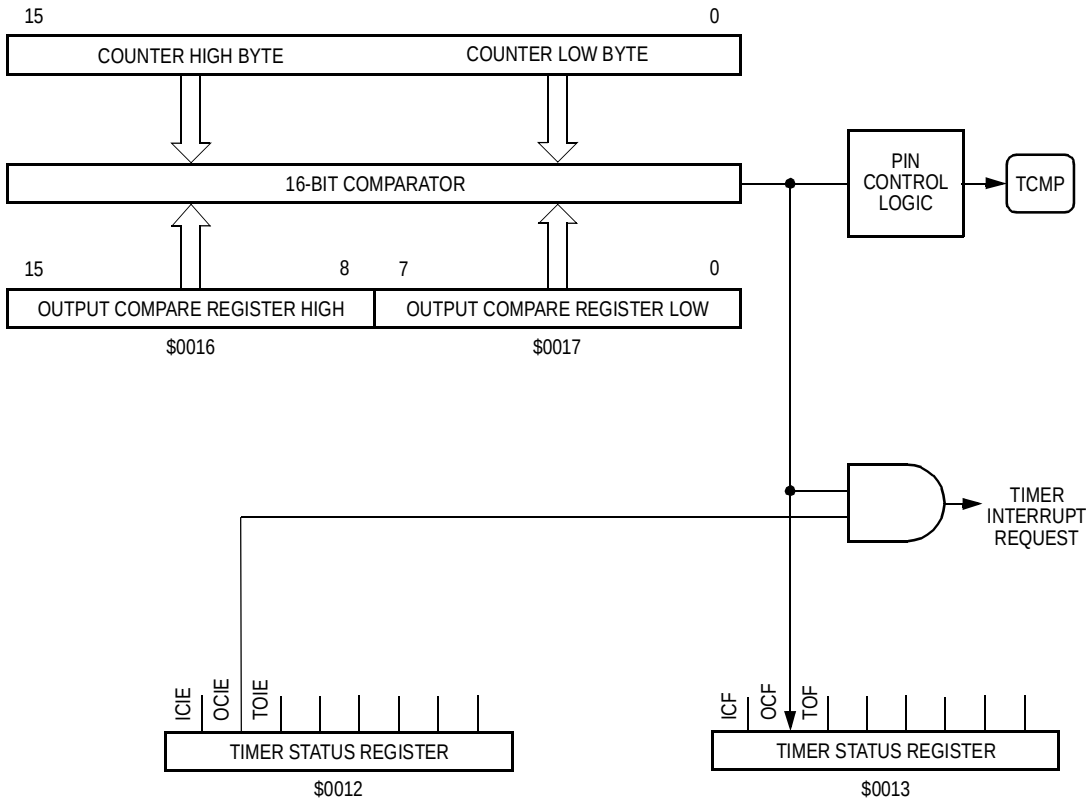


**Figure 8-4. Output Compare Operation**

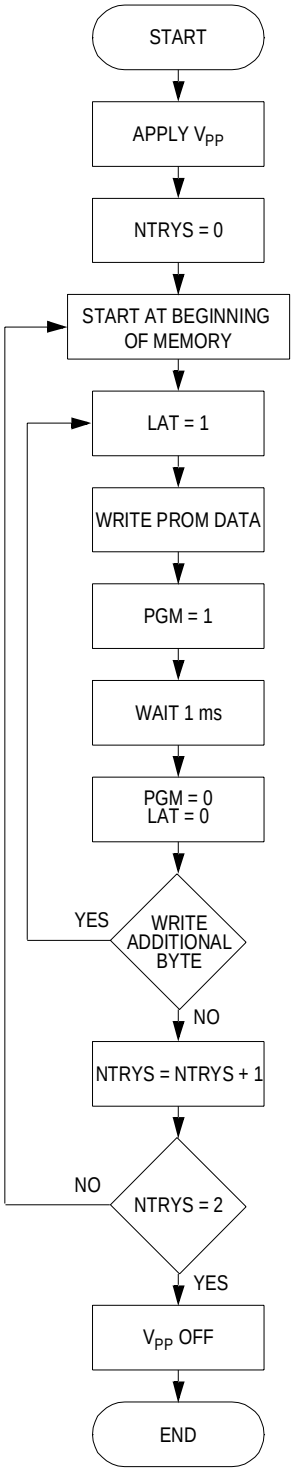


**Figure 9-1. EPROM/OTPROM Programming Flowchart**

### 9.4.2 Verify PROM Contents

The verify PROM contents routine is normally run automatically after the PROM is programmed. Direct entry to this routine causes the PROM contents of the MCU to be compared to the contents of the external memory locations of the EPROM at the same addresses.

To invoke the verify PROM contents routine of the MCU, take these steps:

1. Set switch 1 in the ON position (restores $V_{DD}$).
2. Connect $V_{PP}$ to $V_{DD}$.
3. Set switches S3, S4, and S6 in the OFF position.
4. Set S5 in the ON position.
5. Set switch 2 in the OUT position (routine is activated).

   The red LED is not illuminated during this routine, since no programming takes place. If verification fails, the routine halts with the failing address in the external memory bus. When the green LED is illuminated, verification is completed successfully and the routine is finished.
6. Set switch 2 in the RESET position.

At this point, if another routine is to be performed on the MCU being programmed, the user can set switches S3, S4, S5, and S6 to the positions necessary to select the next routine and move switch S2 to the OUT position to start the routine. If no other routine is to be performed, remove $V_{DD}$ from the board and remove the MCU from the programming socket.

### 9.4.3 Secure PROM

The secure PROM routines are used after the PROM is successfully programmed and verified. Only the SEC bit of the option register ($1FDF) is programmed, but $V_{PP}$ is necessary. Once this bit is programmed, PROM is secure and can be neither verified nor dumped.

## 9.5 Control Registers

This subsection describes the three registers that control memory configuration, PROM security, and IRQ edge or level sensitivity; port B pullups; and non-programmable COP enable/disable.

### 9.5.1 Option Register

The option register shown in **Figure 9-4** is used to select the IRQ sensitivity, enable the PROM security, and select the memory configuration.

Address: $1FDF

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | RAM0 | RAM1 | 0 | 0 | SEC* | | IRQ | 0 |
| Reset: | 0 | 0 | 0 | 0 | * | U | 1 | 0 |

*Implemented as an EPROM cell

= Unimplemented U = Unaffected

**Figure 9-4. Option Register (Option)**

RAM0 — Random-Access Memory Control Bit 0

1 = Maps 32 bytes of RAM into page zero starting at address $0030. Addresses from $0020 to $002F are reserved. This bit can be read or written at any time, allowing memory configuration to be changed during program execution.

0 = Provides 48 bytes of PROM at location $0020–$005F.

RAM1 — Random-Access Memory Control Bit 1

1 = Maps 96 bytes of RAM into page one starting at address $0100. This bit can be read or written at any time, allowing memory configuration to be changed during program execution.

0 = Provides 96 bytes of PROM at location $0100.

SCR2–SCR0 — SCI Baud Rate Select Bits

These read/write bits select the SCI baud rate, as shown in Table 10-2. Reset has no effect on the SCR2–SCR0 bits.

**Table 10-2. Baud Rate Selection**

| SCR[2:1:0] | SCI Baud Rate (Baud) |
|---|---|
| 000 | Prescaled clock ÷ 1 |
| 001 | Prescaled clock ÷ 2 |
| 010 | Prescaled clock ÷ 4 |
| 011 | Prescaled clock ÷ 8 |
| 100 | Prescaled clock ÷ 16 |
| 101 | Prescaled clock ÷ 32 |
| 110 | Prescaled clock ÷ 64 |
| 111 | Prescaled clock ÷ 128 |

Table 10-3 shows all possible SCI baud rates derived from crystal frequencies of 2 MHz, 4 MHz, and 4.194304 MHz.

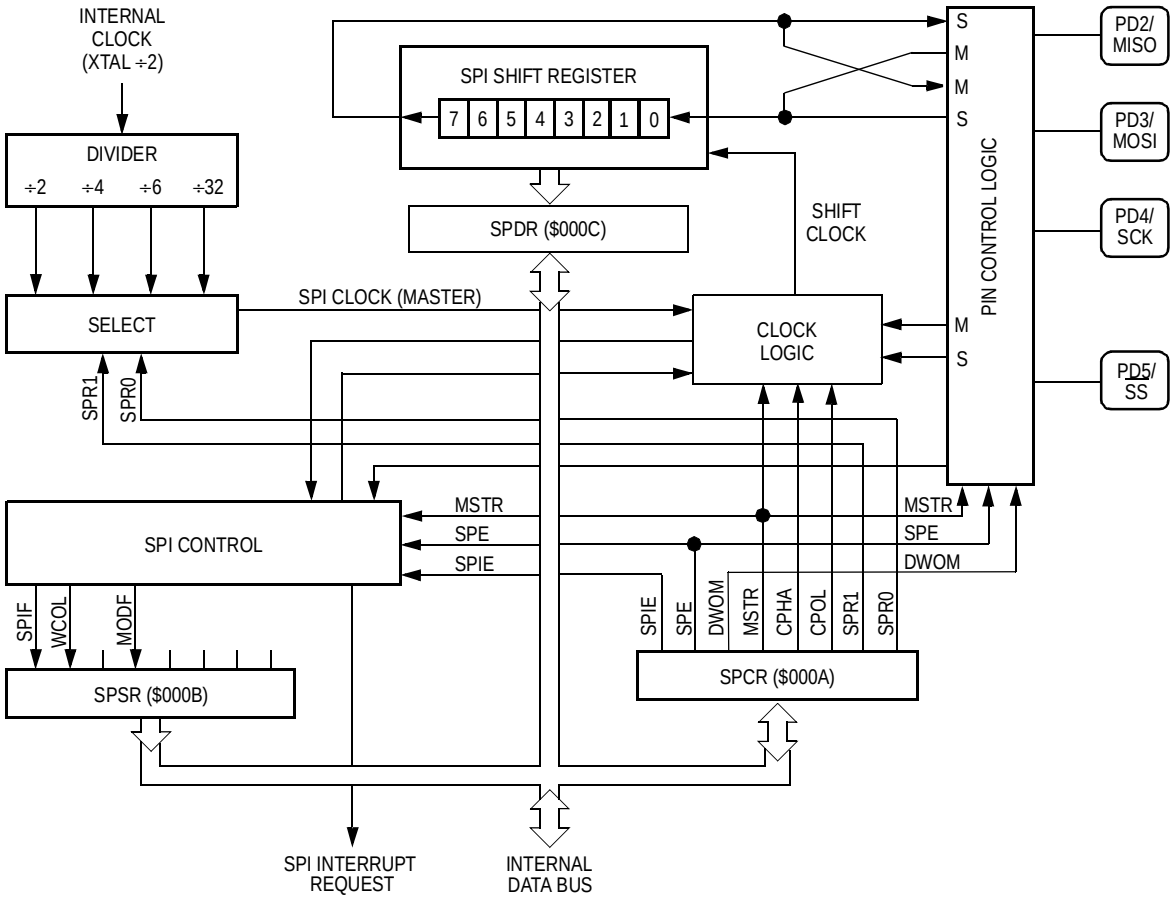


**Figure 11-1. SPI Block Diagram**

### 11.4.2 Pin Functions in Slave Mode

Clearing the MSTR bit in the SPCR configures the SPI for operation in slave mode. The slave-mode functions of the SPI pins are:

- PD4/SCK (serial clock) — In slave mode, the PD4/SCK pin is the input for the synchronizing clock signal from the master SPI.
- PD3/MOSI (master output, slave input) — In slave mode, the PD3/MOSI pin is the serial input.
- PD2/MISO (master input, slave output) — In slave mode, the PD2/MISO pin is the serial output.
- PD5/$\overline{SS}$ (slave select) — In slave mode, the PD5/$\overline{SS}$ pin enables the SPI for data and serial clock reception from a master SPI.

When CPHA = 0, the shift clock is the OR of $\overline{SS}$ with SCK. In this clock phase mode, SS must go high between successive characters in an SPI message. When CPHA = 1, $\overline{SS}$ may be left low for several SPI characters. In cases with only one SPI slave MCU, the slave MCU $\overline{SS}$ line can be tied to $V_{SS}$ as long as CPHA = 1 clock modes are used.

The WCOL flag bit can be improperly set when attempting the first transmission after a reset if these conditions are present: MSTR = 0, CPOL = 0, CPHA = 1, $\overline{SS}$ pin = 0, and SCK pin = 1. The reset states of the CPOL and CPHA bits are 0 and 1, respectively. Under normal operating conditions (CPOL = 0, CPHA = 1), the SCK input will be low.

The incorrect setting of the WCOL bit can be prevented in two ways:

1. Send a dummy transmission after reset, clear the WCOL flag, and then proceed with the real transmission.
2. Use the MSTR bit in the SPCR (SPI control register). This is accomplished by setting the MSTR bit at the same time the CPOL and CPHA bits are programmed to the desired logic levels. Then, the data register can be written to if desired. After this, the MSTR bit should be set to a logic 0, the SPE (SPI enable bit) should be set to a logic 1, and the CPOL, CPHA, SPR1, and SPR0 bits set to the desired logic levels. If this procedure is followed after a reset and before the first access to the SPDR, the WCOL flag will not be set.

## 13.7 5.0-Volt DC Electrical Characteristics

| Characteristic[1] | Symbol | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| Output voltage, $I_{Load} \leq 10.0\ \mu A$ | $V_{OL}$<br>$V_{OH}$ | —<br>$V_{DD} - 0.1$ | —<br>— | 0.1<br>— | V |
| Output high voltage<br>$I_{Load}$ = –0.8 mA, PA7–PA0, PB7–PB0, PC6–PC0, TCMP (see **Figure 13-2**)<br>$I_{Load}$ = –1.6 mA, PD4–PD1 (see **Figure 13-3**)<br>$I_{Load}$ = –5.0 mA, PC7 | $V_{OH}$ | $V_{DD} - 0.8$ | —<br>—<br>— | —<br>—<br>— | V |
| Output low voltage (see **Figure 13-4**)<br>$I_{Load}$ = 1.6 mA<br>PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1<br>$I_{Load}$ = 20 mA, PC7 | $V_{OL}$ | —<br>— | —<br>— | 0.4<br>0.4 | V |
| Input high voltage<br>PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1 | $V_{IH}$ | $0.7 \times V_{DD}$ | — | $V_{DD}$ | V |
| Input low voltage<br>PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1 | $V_{IL}$ | $V_{SS}$ | — | $0.2 \times V_{DD}$ | V |
| EPROM programming voltage | $V_{PP}$ | 14.5 | 14.75 | 15.0 | V |
| EPROM/OTPROM programming current | $I_{PP}$ | — | 5 | 10 | mA |
| User mode current | $I_{PP}$ | — | — | ± 10 | mA |
| Data-retention mode (0°C to 70°C) | $V_{RM}$ | 2.0 | — | — | V |
| Supply current [3]<br>Run[4]<br>Wait[5]<br>Stop[6]<br>25°C<br>–40°C to +85°C | $I_{DD}$ | <br>—<br>—<br><br>—<br>— | <br>5.0<br>1.95<br><br>5.0<br>5.0 | <br>7.0<br>3.0<br><br>50<br>50 | <br>mA<br>mA<br><br>µµA<br>µµA |
| I/O ports hi-z leakage current<br>PA7–PA0, PB7–PB0, PC7–PC0, PD4–PD1, PD7, $\overline{RESET}$ | $I_{IL}$ | — | — | ± 10 | µA |
| Input current, $\overline{IRQ}$, TCAP, OSC1, PD0, PD5 | $I_{In}$ | — | — | ± 1 | µA |
| Capacitance<br>Ports (as input or output)<br>$\overline{RESET}$, $\overline{IRQ}$, TCAP, PD0–PD5, PD7 | $C_{Out}$<br>$C_{In}$ | —<br>— | —<br>— | 12<br>8 | pF |

1. $V_{DD}$ = 5 V ± 10%; $V_{SS}$ = 0 Vdc, $T_A = T_L$ to $T_H$, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range at 25°C.
3. $I_{DD}$ measured with port B pullup devices disabled.
4. Run (operating) $I_{DD}$ measured using external square wave clock source ($f_{OSC}$ = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L$ = 20 pF on OSC2. OSC2 capacitance linearly affects run $I_{DD}$.
5. Wait $I_{DD}$ measured using external square wave clock source ($f_{OSC}$ = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L$ = 20 pF on OSC2. $V_{IL}$ = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects wait $I_{DD}$.
6. Stop $I_{DD}$ measured with OSC1 = $V_{DD}$. All ports configured as inputs. $V_{IL}$ = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V.

# Section 15. Ordering Information

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## 15.2 Introduction

This section contains ordering information for the available package types.

## 15.3 MCU Order Numbers

**Table 15-1** lists the MC order numbers.

**Table 15-1. MC68HC705C8A Order Numbers**

| Package Type | Temperature Range | Order Number |
|---|---|---|
| 40-pin plastic dual in-line package (PDIP) | –40°C to +85°C | MC68HC705C8AC(1)P(2) |
| 44-lead plastic-leaded chip carrier (PLCC) | –40°C to +85°C | MC68HC705C8ACFN(3) |
| 44-lead ceramic-leaded chip carrier (CLCC) | –40°C to +85°C | MC68HC705C8ACFS(4) |
| 40-pin windowed ceramic DIP (Cerdip) | –40°C to +85°C | MC68HC705C8ACS(5) |
| 44-pin quad flat pack (QFP) | –40°C to +85°C | MC68HC705C8ACFB(6) |
| 42-pin shrink dual in-line package (SDIP) | –40°C to +85°C | MC68HC705C8ACB(7) |

1. C = Extended temperature range (–40°C to +85°C)
2. P = Plastic dual in-line package (PDIP)
3. FN = Plastic-leaded chip carrier (PLCC)
4. FS = Ceramic-leaded chip carrier (CLCC)
5. S = Windowed ceramic dual in-line package (Cerdip)
6. FB = Quad flat pack (QFP)
7. B = Shrink dual in-line package (SDIP)

## A.9 Ordering Information

Table A-2 provides ordering information for the MC68HSC705C8A.

**Table A-2. MC68HSC705C8A Order Numbers**

| Package Type | Temperature Range | Order Number |
|---|---|---|
| 40-pin plastic dual in-line package (PDIP) | –40°C to +85°C | MC68HSC705C8AC(1)P(2) |
| 44-lead plastic-leaded chip carrier (PLCC) | –40°C to +85°C | MC68HSC705C8ACFN(3) |
| 44-lead ceramic-leaded chip carrier (CLCC) | –40°C to +85°C | MC68HSC705C8ACFS(4) |
| 40-pin ceramic DIP (cerdip) | –40°C to +85°C | MC68HSC705C8ACS(5) |
| 44-pin quad flat pack (QFP) | –40°C to +85°C | MC68HSC705C8ACFB(6) |
| 42-pin shrink dual in-line package (SDIP) | –40°C to +85°C | MC68HSC705C8ACB(7) |

1. C = Extended temperature range (–40°C to +85°C)
2. P = Plastic dual in-line package (PDIP)
3. FN = Plastic-leaded chip carrier (PLCC)
4. FS = Ceramic-leaded chip carrier (CLCC)
5. S = Windowed ceramic dual in-line package (cerdip)
6. FB = Quad flat pack (QFP)
7. B = Shrink dual in-line package (SDIP)

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