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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchsc705c8acfbe

1.7 Pin Functions

This subsection describes the MC68HC705C8A signals. Reference is made, where applicable, to other sections that contain more detail about the function being performed.

1.7.1 V_{DD} and V_{SS}

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins, placing high short-duration current demands on the power supply. To prevent noise problems, take special care to provide good power supply bypassing at the MCU. Place bypass capacitors as close to the MCU as possible, as shown in Figure 1-7.

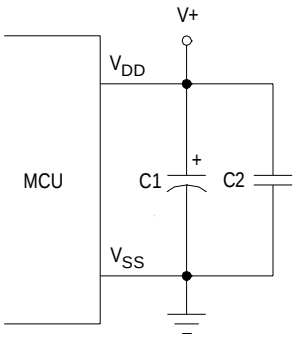


Figure 1-7. Bypassing Layout Recommendation

1.7.2 V_{PP}

This pin provides the programming voltage to the EPROM array. For normal operation, V_{PP} shuld be tied to V_{DD}.

NOTE: *Connecting the V_{PP} pin (programming voltage) to V_{SS} (ground) could result in damage to the MCU.*

subroutine call to save the CPU state. The stack pointer decrements during pushes and increments during pulls.

Figure 2-1 is a memory map of the MCU. Addresses $0000–$001F, shown in **Figure 2-2**, contain most of the control, status, and data registers. Additional I/O registers have these addresses:

- $1FDF, option register
- $1FF0, mask option register 1 (MOR1)
- $1FF1, mask option register 2 (MOR2)

2.4 Input/Output (I/O)

The first 32 addresses of memory space, from $0000 to $001F, are the I/O section. These are the addresses of the I/O control registers, status registers, and data registers. See **Figure 2-2** for more information.

2.5 RAM

One of four selectable memory configurations is selected by the state of the RAM1 and RAM0 bits in the option register located at $1FDF. Reset or power-on reset (POR) clears these bits, automatically selecting the first memory configuration as shown in **Table 2-1**. See **9.5.1 Option Register**.

Table 2-1. Memory Configurations

RAM0	RAM1	RAM Bytes	PROM Bytes
0	0	176	7744
1	0	208	7696
0	1	272	7648
1	1	304	7600

NOTE: *Be careful when using nested subroutines or multiple interrupt levels. The CPU can overwrite data in the stack RAM during a subroutine or during the interrupt stacking operation.*

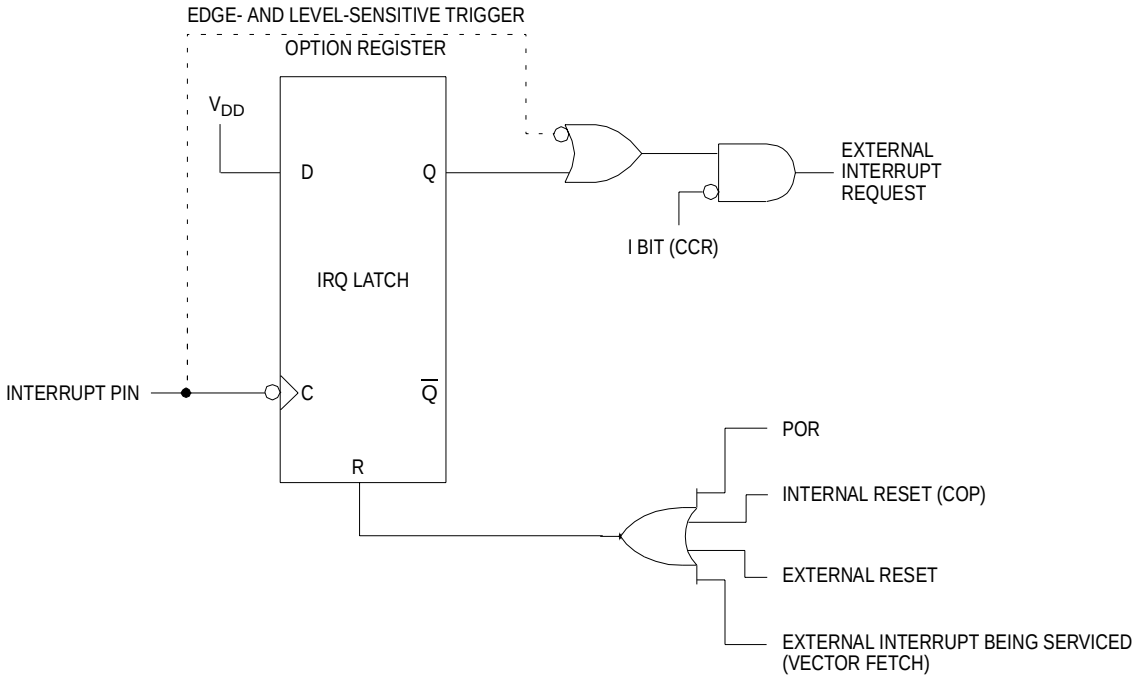
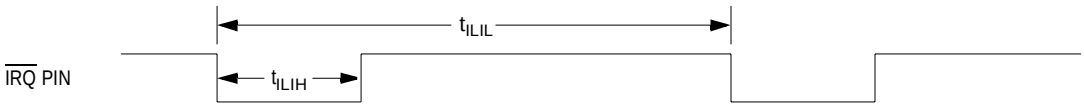
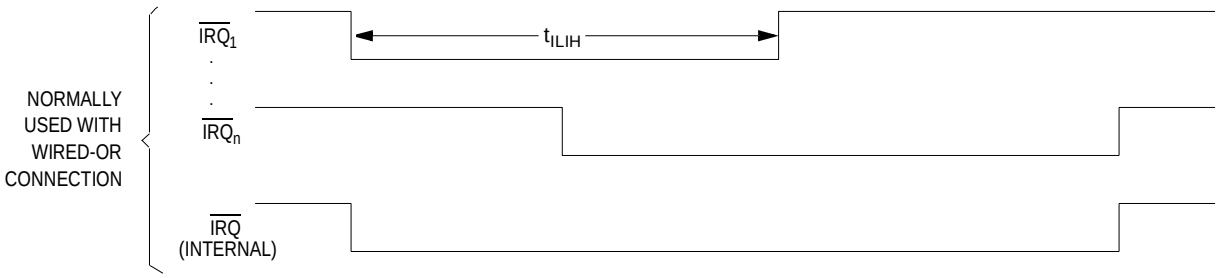


Figure 4-1. External Interrupt Internal Function Diagram



a. Edge-Sensitive Trigger Condition. The minimum pulse width (t_{ILIH}) is either 125 ns (f_{OP} = 2.1 MHz) or 250 ns (f_{OP} = 1 MHz). The period t_{ILIL} should not be less than the number of t_{CYC} cycles it takes to execute the interrupt service routine plus 19 t_{CYC} cycles.



b. Level-Sensitive Trigger Condition. If the interrupt line remains low after servicing an interrupt, then the CPU continues to recognize an interrupt.

Figure 4-2. External Interrupt Timing

4.3.4 Capture/Compare Timer Interrupts

Setting the I bit in the CCR disables all interrupts except for SWI.

4.3.5 SCI Interrupts

The serial communications interface (SCI) can generate these interrupts:

- Transmit data register empty interrupt
- Transmission complete interrupt
- Receive data register full interrupt
- Receiver overrun interrupt
- Receiver input idle interrupt

Setting the I bit in the CCR disables all SCI interrupts.

- **SCI Transmit Data Register Empty Interrupt** — The transmit data register empty bit (TDRE) indicates that the SCI data register is ready to receive a byte for transmission. TDRE becomes set when data in the SCI data register transfers to the transmit shift register. TDRE generates an interrupt request if the transmit interrupt enable bit (TIE) is set also.
- **SCI Transmission Complete Interrupt** — The transmission complete bit (TC) indicates the completion of an SCI transmission. TC becomes set when the TDRE bit becomes set and no data, preamble, or break character is being transmitted. TC generates an interrupt request if the transmission complete interrupt enable bit (TCIE) is set also.
- **SCI Receive Data Register Full Interrupt** — The receive data register full bit (RDRF) indicates that a byte is ready to be read in the SCI data register. RDRF becomes set when the data in the receive shift register transfers to the SCI data register. RDRF generates an interrupt request if the receive interrupt enable bit (RIE) is set also.

5.3.3.1 Programmable COP Watchdog Reset

A timeout of the 18-stage ripple counter in the programmable COP watchdog generates a reset. **Figure 5-1** is a diagram of the programmable COP watchdog. Two registers control and monitor operation of the programmable COP watchdog:

- COP reset register (COPRST), $001D
- COP control register (COPCR), $001E

To clear the programmable COP watchdog and begin a new timeout period, write these values to the COP reset register (COPRST). See **Figure 5-2**.

1. $55
2. $AA

The $55 write must precede the $AA write. Instructions may be executed between the write operations provided that the COP watchdog does not time out before the second write.

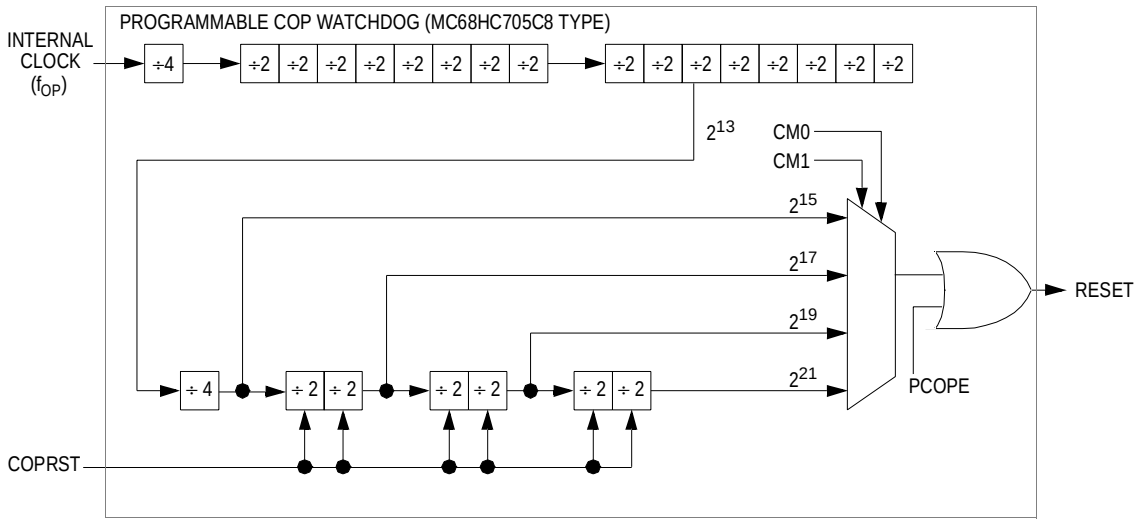


Figure 5-1. Programmable COP Watchdog Diagram

2. COP clear bit (COPC) at address $1FF0

   To clear the non-programmable COP watchdog and start a new COP timeout period, write a logic 0 to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. See **9.5.2 Mask Option Register 1**.

NOTE: *The non-programmable watchdog COP is disabled in bootloader mode, even if the NCOPE bit is programmed.*

Figure 5-4 is a diagram of the non-programmable COP.

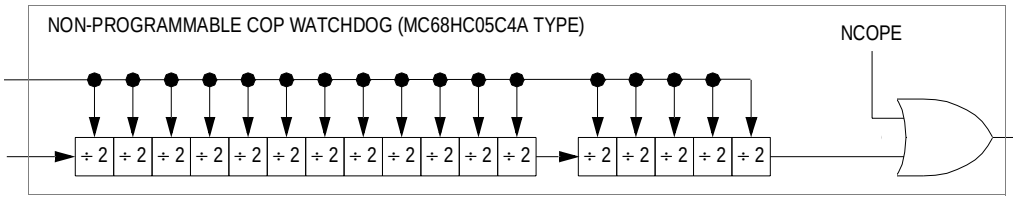


Figure 5-4. Non-Programmable COP Watchdog Diagram

5.3.4 Clock Monitor Reset

When the CME bit in the COP control register is set, the clock monitor detects the absence of the internal bus clock for a certain period of time. The timeout period depends on processing parameters and varies from 5 µs to 100 µs, which implies that systems using a bus clock rate of 200 kHz or less should not use the clock monitor function.

If a slow or absent clock is detected, the clock monitor causes a system reset. The reset is issued to the external system for four bus cycles using the bidirectional $\overline{\text{RESET}}$ pin.

Special consideration is required when using the STOP instruction with the clock monitor. Since STOP causes the system clocks to halt, the clock monitor issues a system reset when STOP is executed.

The clock monitor is a useful backup to the COP watchdog system. Because the watchdog timer requires a clock to function, it cannot indicate a system clock failure. The clock monitor would detect such a condition and force the MCU to a reset state. Clocks are not required for the MCU to reach a reset condition. They are, however, required to bring the MCU through the reset sequence and back to run condition.

Section 7. Parallel Input/Output (I/O)

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7.5.3 Port C Logic 87

7.6 Port D 88

7.2 Introduction

This section describes the programming of ports A, B, C, and D.

7.6 Port D

Port D is a 7-bit, special-purpose, input-only port that has no data register. Reading address $0003 returns the logic states of the port D pins.

Port D shares pins PD5–PD2 with the serial peripheral interface module (SPI). When the SPI is enabled, PD5–PD2 read as logic 0s. When the SPI is disabled, reading address $0003 returns the logic states of the PD5–PD2 pins.

Port D shares pins PD1 and PD0 with the SCI module. When the SCI is enabled, PD1 and PD0 read as logic 0s. When the SCI is disabled, reading address $0003 returns the logic states of the PD1 and PD0 pins.

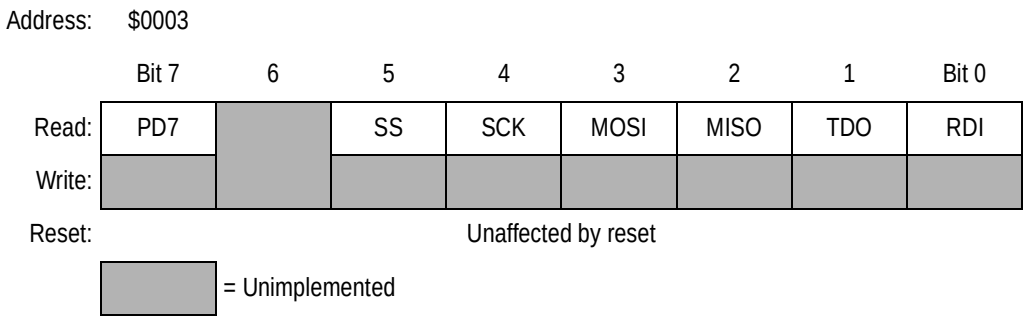

Figure 7-10. Port D Fixed Input Register (PORTD)

Section 8. Capture/Compare Timer

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8.2 Introduction

This section describes the operation of the 16-bit capture/compare timer. **Figure 8-1** shows the structure of the timer module. **Figure 8-2** is a summary of the timer input/output (I/O) registers.

8.3 Timer Operation

The core of the capture/compare timer is a 16-bit free-running counter. The counter is the timing reference for the input capture and output compare functions. The input capture and output compare functions can latch the times at which external events occur, measure input waveforms, and generate output waveforms and timing delays. Software can read the value in the counter at any time without affecting the counter sequence.

8.4 Timer I/O Registers

These registers control and monitor the timer operation:

- Timer control register (TCR)
- Timer status register (TSR)
- Timer registers (TRH and TRL)
- Alternate timer registers (ATRH and ATRL)
- Input capture registers (ICRH and ICRL)
- Output compare registers (OCRH and OCRL)

8.4.1 Timer Control Register

The timer control register (TCR) as shown in **Figure 8-5** performs these functions:

- Enables input capture interrupts
- Enables output compare interrupts
- Enables timer overflow interrupts
- Controls the active edge polarity of the TCAP signal
- Controls the active level of the TCMP output

Address: $0012

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
Reset:	0	0	0	0	0	0	U	0

U = Unaffected

Figure 8-5. Timer Control Register (TCR)

EPROM/OTPROM (PROM)

Example:

```
LDA #$1C   ; MSTR = 1, CPOL = 1, CPHA = 1,
           ; SPR1 = SPR0 = 0
STA SPCR   ; SPI control register
LDA #$4C   ; MSTR = 0, SPE = 1, CPOL = 1, CPHA = 1,
           ; SPR1 = SPR0 = 0
STA SPCR   ; SPI control register
```

11.5 Multiple-SPI Systems

In a multiple-SPI system, all PD4/SCK pins are connected together, all PD3/MOSI pins are connected together, and all PD2/MISO pins are connected together.

Before a transmission, one SPI is configured as master and the rest are configured as slaves. **Figure 11-4** is a block diagram showing a single master SPI and three slave SPIs.

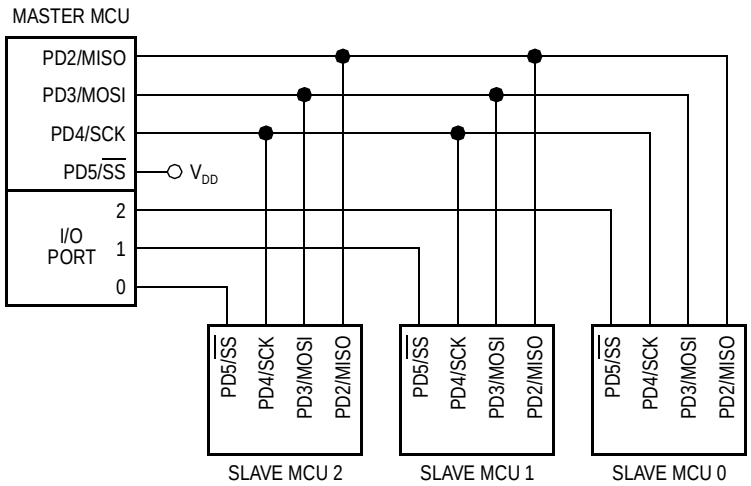

Figure 11-4. One Master and Three Slaves Block Diagram

Figure 11-5 is another block diagram with two master/slave SPIs and three slave SPIs.

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12.5 Instruction Set Summary 164

12.6 Opcode Map 169

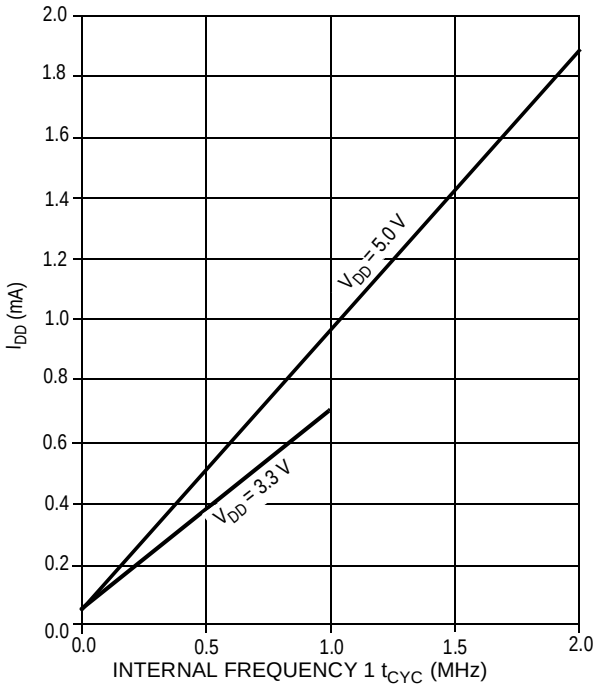
Table 12-6. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2

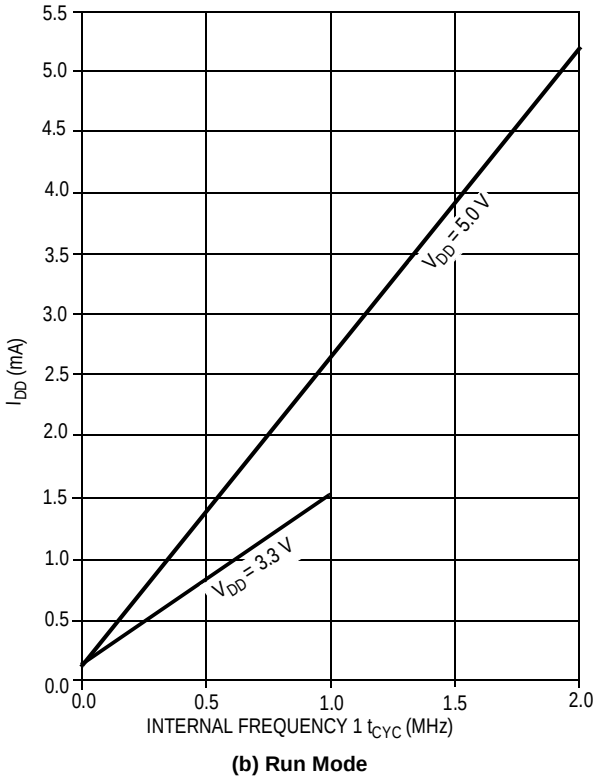
13.7 5.0-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage, $I_{Load} \leq 10.0\ \mu A$	V_{OL} V_{OH}	— $V_{DD} - 0.1$	— —	0.1 —	V
Output high voltage I_{Load} = –0.8 mA, PA7–PA0, PB7–PB0, PC6–PC0, TCMP (see **Figure 13-2**) I_{Load} = –1.6 mA, PD4–PD1 (see **Figure 13-3**) I_{Load} = –5.0 mA, PC7	V_{OH}	$V_{DD} - 0.8$	— — —	— — —	V
Output low voltage (see **Figure 13-4**) I_{Load} = 1.6 mA PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1 I_{Load} = 20 mA, PC7	V_{OL}	— —	— —	0.4 0.4	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD5–PD0, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
EPROM programming voltage	V_{PP}	14.5	14.75	15.0	V
EPROM/OTPROM programming current	I_{PP}	—	5	10	mA
User mode current	I_{PP}	—	—	± 10	mA
Data-retention mode (0°C to 70°C)	V_{RM}	2.0	—	—	V
Supply current [3] Run[4] Wait[5] Stop[6] 25°C –40°C to +85°C	I_{DD}	 — — — —	 5.0 1.95 5.0 5.0	 7.0 3.0 50 50	 mA mA µµA µµA
I/O ports hi-z leakage current PA7–PA0, PB7–PB0, PC7–PC0, PD4–PD1, PD7, $\overline{RESET}$	I_{IL}	—	—	± 10	µA
Input current, $\overline{IRQ}$, TCAP, OSC1, PD0, PD5	I_{In}	—	—	± 1	µA
Capacitance Ports (as input or output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, PD0–PD5, PD7	C_{Out} C_{In}	— —	— —	12 8	pF

1. V_{DD} = 5 V ± 10%; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range at 25°C.
3. I_{DD} measured with port B pullup devices disabled.
4. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. OSC2 capacitance linearly affects run I_{DD}.
5. Wait I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects wait I_{DD}.
6. Stop I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V, $V_{IH} = V_{DD} - 0.2$ V.



(a) Wait Mode



(b) Run Mode

Figure 13-3. Typical Current versus Internal Frequency for Run and Wait Modes

13.9 5.0-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option	f_{OSC}	— dc	4.2 4.2	MHz
Internal operating frequency Crystal ($f_{OSC} \div 2$) External clock ($f_{OSC} \div 2$)	f_{OP}	— dc	2.1 2.1	MHz
Cycle time (see **Figure 13-7**)	t_{CYC}	480	—	ns
Crystal oscillator startup time (see **Figure 13-7**)	t_{OXOV}	—	100	ms
Stop recovery startup time (crystal oscillator) (see **Figure 13-6**)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ pulse width (see **Figure 13-7**)	t_{RL}	8	—	t_{CYC}
Timer Resolution[2] Input capture pulse width (see **Figure 13-5**) Input capture pulse period (see **Figure 13-5**)	t_{RESL} t_{TH}, t_{TL} t_{TLTL}	4.0 125 [3]	— — —	t_{CYC} ns t_{CYC}
Interrupt pulse width low (edge-triggered) (see **Figure 4-2. External Interrupt Timing**)	t_{ILIH}	125	—	ns
Interrupt pulse period (see **Figure 4-2. External Interrupt Timing**)	t_{ILIL}	[4]	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc; $T_A = T_L$ to T_H
2. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
3. The minimum period, t_{TLTL}, should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
4. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.

Diagram Number(1)	Characteristic(2)	Symbol	Min	Max	Unit
11	Data hold time (outputs) Master (after capture edge) Slave (after enable edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
12	Rise time(7) SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 50 2.0	 ns µs
13	Fall time(8) SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 50 2.0	 ns µs

1. Diagram numbers refer to dimensions in **Figure 13-8. SPI Master Timing** and **Figure 13-9. SPI Slave Timing**.
2. V_{DD} = 5 V ± 10%; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
3. Signal production depends on software.
4. Time to data active from high-impedance state
5. Hold time to high-impedance state
6. With 200 pF on all SPI pins.
7. 20% of V_{DD} to 70% of V_{DD}; C_L = 200 pF
8. 70% of V_{DD} to 20% of V_{DD}; C_L = 200 pF

Diagram Number(1)	Characteristic(2)	Symbol	Min	Max	Unit
11	Data hold time (outputs) Master (after capture edge) Slave (after enable edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
12	Rise time(7) SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 100 2.0	 ns µs
13	Fall time(8) SPI outputs (SCK, MOSI, MISO) SPI inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 100 2.0	 ns µs

1. Diagram numbers refer to dimensions in **Figure 13-8. SPI Master Timing** and **Figure 13-9. SPI Slave Timing**.
2. V_{DD} = 3.3 V ± 10%; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
3. Signal production depends on software.
4. Time to data active from high-impedance state
5. Hold time to high-impedance state
6. With 200 pF on all SPI pins
7. 20% of V_{DD} to 70% of V_{DD}; C_L = 200 pF
8. 70% of V_{DD} to 20% of V_{DD}; C_L = 200 pF