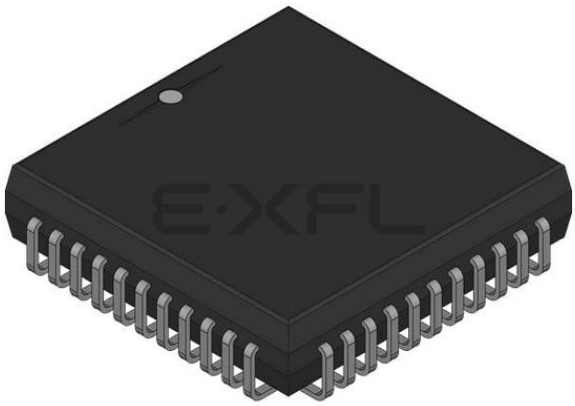


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchsc705c8acfne

List of Sections

Section 12. Instruction Set

Section 13. Electrical Specifications

Section 14. Mechanical Specifications

List of Figures

1.6 Pin Assignments

The MC68HC705C8A is available in six packages:

- 40-pin plastic dual in-line package (PDIP)
- 40-pin ceramic dual in-line package (cerdip)
- 44-lead plastic-leaded chip carrier (PLCC)
- 44-lead ceramic-leaded chip carrier (CLCC)
- 44-pin quad flat pack (QFP)
- 42-pin shrink dual in-line package (SDIP)

The pin assignments for these packages are shown in **Figure 1-3**, **Figure 1-4**, **Figure 1-5**, and **Figure 1-6**.

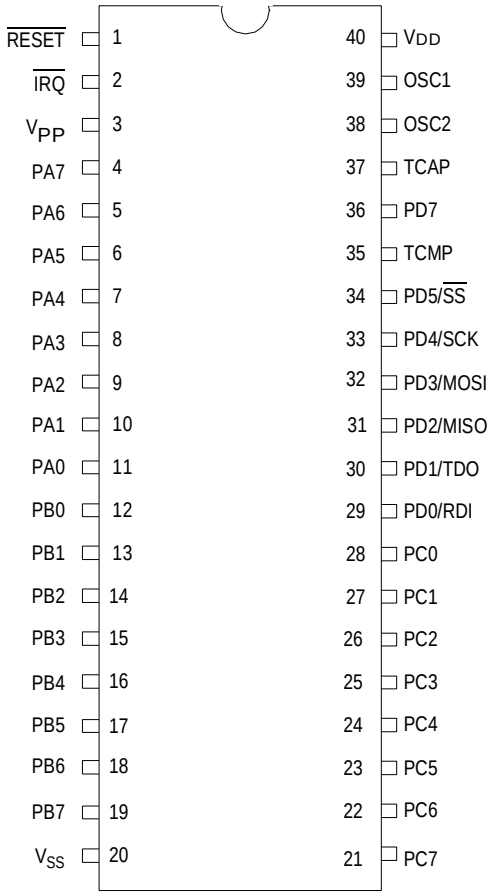


Figure 1-3. 40-Pin PDIP/Cerdip Pin Assignments

1.7.3.3 External Clock Signal

An external clock from another CMOS-compatible device can drive the OSC1 input, with the OSC2 pin unconnected, as **Figure 1-11** shows.

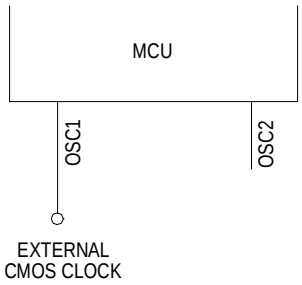


Figure 1-11. External Clock

NOTE: *The bus frequency (f_{OP}) is one-half the external frequency (f_{OSC}) while the processor clock cycle is two times the f_{OSC} period.*

1.7.4 External Reset Pin ($\overline{\text{RESET}}$)

A logic 0 on the bidirectional $\overline{\text{RESET}}$ pin forces the MCU to a known startup state. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. See **Section 5. Resets**.

1.7.5 External Interrupt Request Pin ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is an asynchronous external interrupt pin. The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. See **4.3.2 External Interrupt (IRQ)**.

1.7.6 Input Capture Pin (TCAP)

The TCAP pin is the input capture pin for the on-chip capture/compare timer. The TCAP pin contains an internal Schmitt trigger as part of its input to improve noise immunity. See **Section 8. Capture/Compare Timer**.

2.6 EPROM/OTPROM (PROM)

An MCU with a quartz window has a maximum of 7744 bytes of EPROM. The quartz window allows the EPROM erasure with ultraviolet light. In an MCU without a quartz window, the EPROM cannot be erased and serves a maximum 7744 bytes of OTPROM (see **Table 2-1**). See **Section 9. EPROM/OTPROM (PROM)**.

2.7 Bootloader ROM

The 240 bytes at addresses $1F00–$1FEF are reserved ROM addresses that contain the instructions for the bootloader functions. See **Section 9. EPROM/OTPROM (PROM)**.

3.3 CPU Registers

Figure 3-1 shows the five CPU registers. These are hard-wired registers within the CPU and are not part of the memory map.

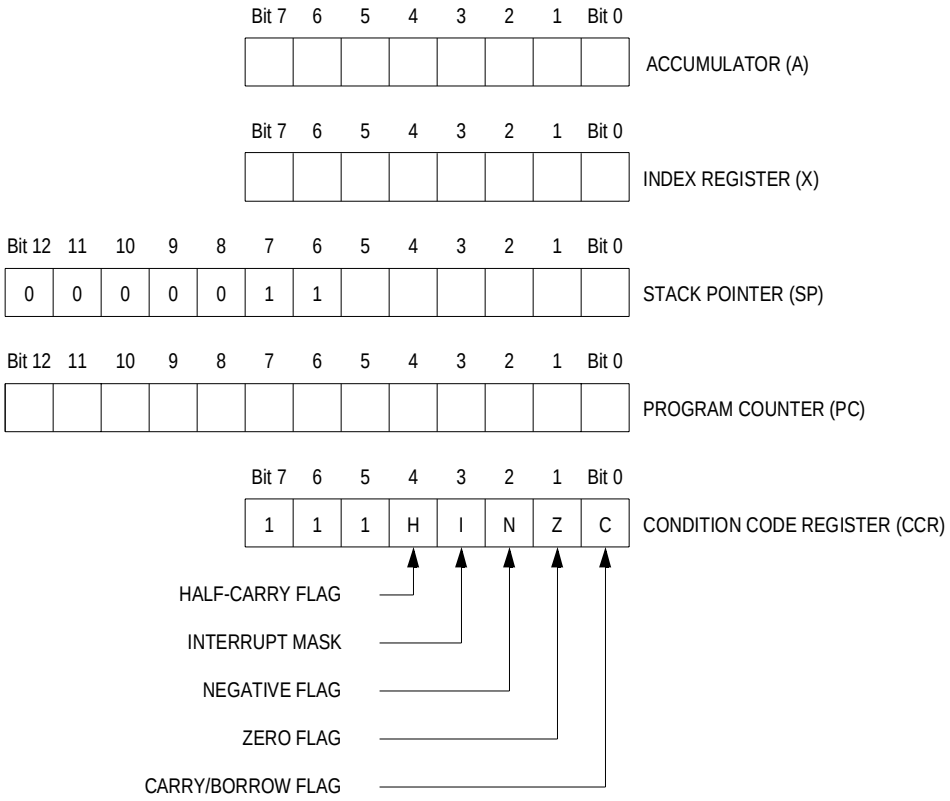


Figure 3-1. Programming Model

3.3.3 Stack Pointer

The stack pointer (SP) shown in **Figure 3-4** is a 13-bit register that contains the address of the next free location on the stack. During a reset or after the reset stack pointer (RSP) instruction, the stack pointer initializes to $00FF. The address in the stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

The seven most significant bits of the stack pointer are fixed permanently at 0000011, so the stack pointer produces addresses from $00C0 to $00FF. If subroutines and interrupts use more than 64 stack locations, the stack pointer wraps around to address $00FF and begins writing over the previously stored data. A subroutine uses two stack locations. An interrupt uses five locations.

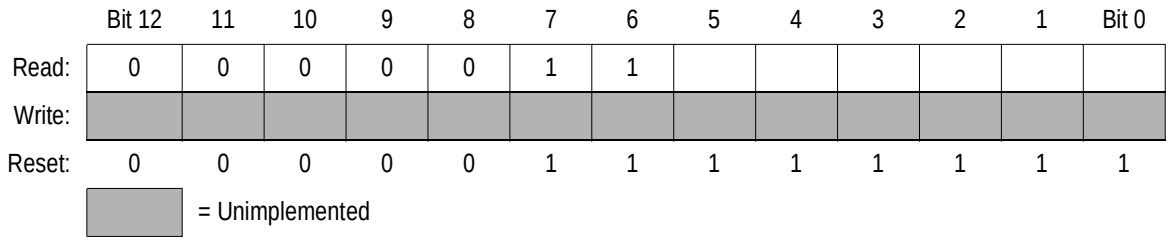


Figure 3-4. Stack Pointer (SP)

3.3.4 Program Counter

The program counter (PC) shown in **Figure 3-5** is a 13-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the address in the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

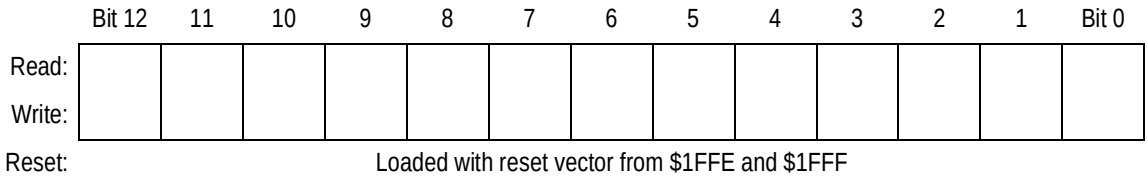


Figure 3-5. Program Counter (PC)

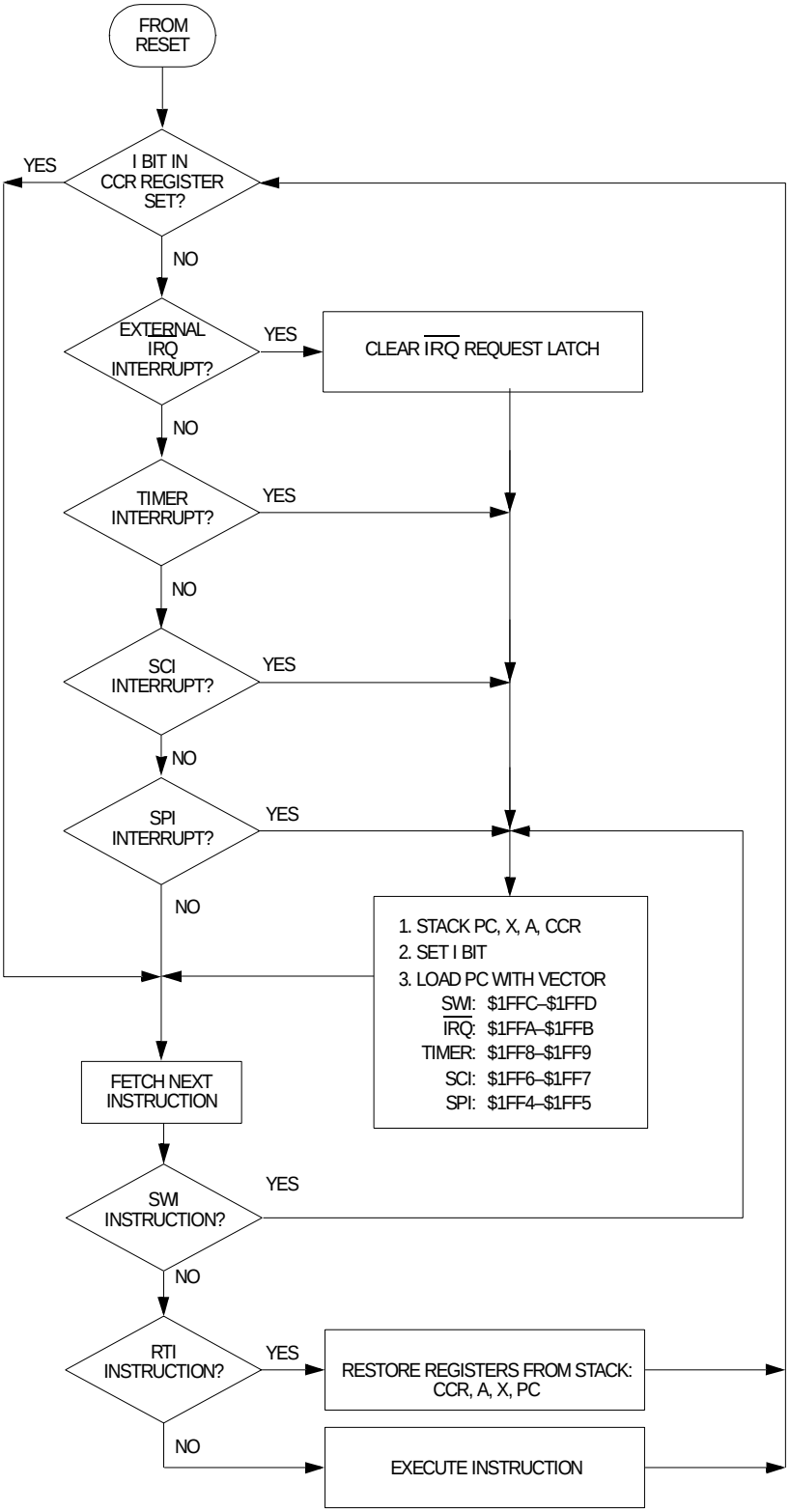


Figure 4-5. Reset and Interrupt Processing Flowchart

2. COP clear bit (COPC) at address $1FF0

   To clear the non-programmable COP watchdog and start a new COP timeout period, write a logic 0 to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. See **9.5.2 Mask Option Register 1**.

NOTE: *The non-programmable watchdog COP is disabled in bootloader mode, even if the NCOPE bit is programmed.*

Figure 5-4 is a diagram of the non-programmable COP.

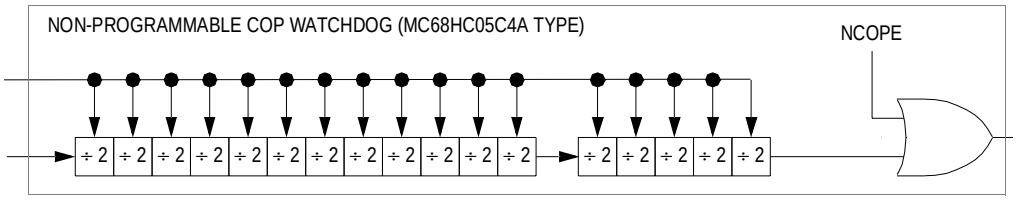


Figure 5-4. Non-Programmable COP Watchdog Diagram

5.3.4 Clock Monitor Reset

When the CME bit in the COP control register is set, the clock monitor detects the absence of the internal bus clock for a certain period of time. The timeout period depends on processing parameters and varies from 5 µs to 100 µs, which implies that systems using a bus clock rate of 200 kHz or less should not use the clock monitor function.

If a slow or absent clock is detected, the clock monitor causes a system reset. The reset is issued to the external system for four bus cycles using the bidirectional $\overline{\text{RESET}}$ pin.

Special consideration is required when using the STOP instruction with the clock monitor. Since STOP causes the system clocks to halt, the clock monitor issues a system reset when STOP is executed.

7.3.3 Port A Logic

Figure 7-3 is a diagram of the port A I/O logic.

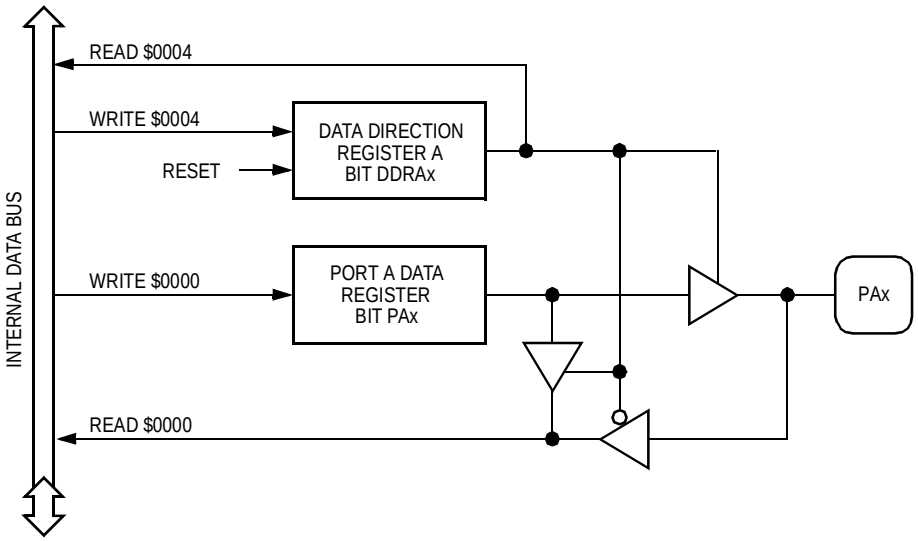


Figure 7-3. Port A I/O Logic

When a port A pin is programmed to be an output, the state of its data register bit determines the state of the output pin. When a port A pin is programmed to be an input, reading the port A data register returns the logic state of the pin.

The data latch can always be written, regardless of the state of its DDRA bit. Table 7-1 summarizes the operation of the port A pins.

Table 7-1. Port A Pin Functions

DDRA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PORTA	
		Read/Write	Read	Write
0	Input, Hi-Z(1)	DDRA7–DDRA0	Pin	PA7–PA0(2)
1	Output	DDRA7–DDRA0	PA7–PA0	PA7–PA0

1. Hi-Z = high impedance
2. Writing affects data register but does not affect input.

NOTE: *To avoid excessive current draw, tie all unused input pins to V_{DD} or V_{SS}, or change I/O pins to outputs by writing to DDRA in user code as early as possible.*

7.5.2 Data Direction Register C

The contents of data direction register C (DDRC) shown in **Figure 7-8** determine whether each port C pin is an input or an output. Writing a logic 1 to a DDRC bit enables the output buffer for the associated port C pin; a logic 0 disables the output buffer. A reset clears all DDRC bits, configuring all port C pins as inputs.

Address: $0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
Reset:	0	0	0	0	0	0	0	0

Figure 7-8. Data Direction Register C (DDRC)

DDRC7–DDRC0 — Port C Data Direction Bits

These read/write bits control port C data direction. Reset clears bits DDRC7–DDRC0.

1 = Corresponding port C pin configured as output
0 = Corresponding port C pin configured as input

NOTE: *Avoid glitches on port C pins by writing to the port C data register before changing DDRC bits from logic 0 to logic 1.*

9.4 PROM Programming Routines

This subsection describes the routines necessary to program, verify, and secure the PROM device, and other routines available to the user.

9.4.1 Program and Verify PROM

The program and verify PROM routine copies the contents of the external EPROM into the MCU PROM with direct correspondence between the addresses. Memory addresses in the MCU that are not implemented in PROM are skipped. Unprogrammed addresses in the EPROM being copied should contain $00 bytes to speed up the programming process.

To run the program and verify the PROM routine on the PROM MCU, take these steps:

1. Set switch 1 in the ON position (restores V_{DD}).
2. Restore the V_{PP} power source.
3. Set switches S3, S4, S5, and S6 in the OFF position (selects proper routine).
4. Set switch 2 in the OUT position (routine is activated).

   The red light-emitting diode (LED) is illuminated, showing that the programming part of the routine is running. The LED goes out when programming is finished. The verification part of the routine now begins. When the green LED is illuminated, verification is successfully completed and the routine is finished.
5. Set switch 2 in the RESET position.

At this point, if no other MCU is to be programmed or secured, remove V_{PP} power from the board. If another routine is to be performed on the MCU being programmed, the user can then set switches S3, S4, S5, and S6 to the positions necessary to select the next routine, and begin the routine by setting switch 2 to the OUT position. If no other routine is to be performed, remove V_{DD} from the board and remove the MCU from the programming socket.

9.6 EPROM Erasing

The erased state of an EPROM or OTPROM byte is $00. EPROM devices can be erased by exposure to a high intensity ultraviolet (UV) light with a wave length of 2537 Å. The recommended erasure dosage (UV intensity on a given surface area x exposure time) is 15 Ws/cm^2. UV lamps should be used without short-wave filters, and the EPROM device should be positioned about one inch from the UV source.

OTPROM devices are shipped in an erased state. Once programmed, they cannot be erased. Electrical erasing procedures cannot be performed on either EPROM or OTPROM devices.

Section 10. Serial Communications Interface (SCI)

10.1 Contents

10.2 Introduction

The serial communications interface (SCI) module allows high-speed asynchronous communication with peripheral devices and other microcontroller units (MCUs).

11.9.3 SPI Status Register

The SPSR shown in **Figure 11-9** contains flags to signal these conditions:

- SPI transmission complete
- Write collision
- Mode fault

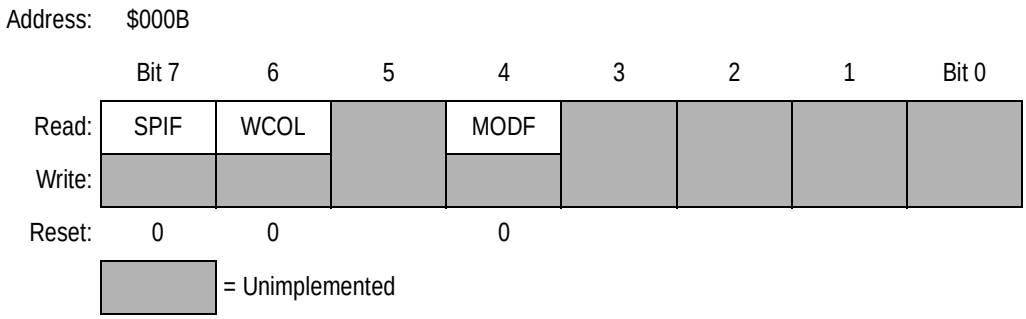


Figure 11-9. SPI Status Register (SPSR)

SPIF — SPI Flag

This clearable, read-only bit is set each time a byte shifts out of or into the shift register. SPIF generates an interrupt request if the SPIE bit in the SPCR is also set. Clear SPIF by reading the SPSR with SPIF set and then reading or writing the SPDR. Reset clears the SPIF bit.

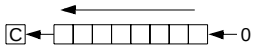
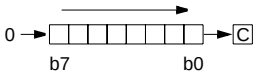
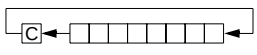
1 = Transmission complete
0 = Transmission not complete

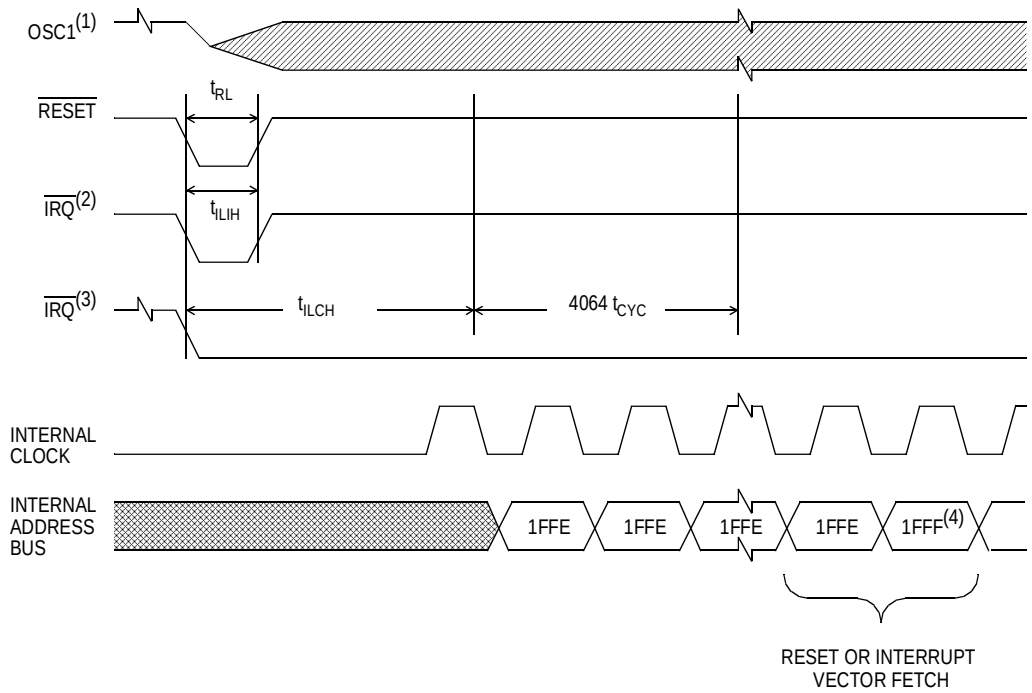
WCOL — Write Collision Bit

This clearable, read-only flag is set when software writes to the SPDR while a transmission is in progress. Clear the WCOL bit by reading the SPSR with WCOL set and then reading or writing the SPDR. Reset clears WCOL.

1 = Invalid write to SPDR
0 = No invalid write to SPDR

Table 12-6. Instruction Set Summary (Sheet 4 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		1 1
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff 	5 3 3 6 5



Notes:
1. Represents the internal gating of the OSC1 pin
2. IRQ pin edge-sensitive option
3. IRQ pin level and edge-sensitive option
4. RESET vector address shown for timing example

Figure 13-6. Stop Recovery Timing Diagram

Index