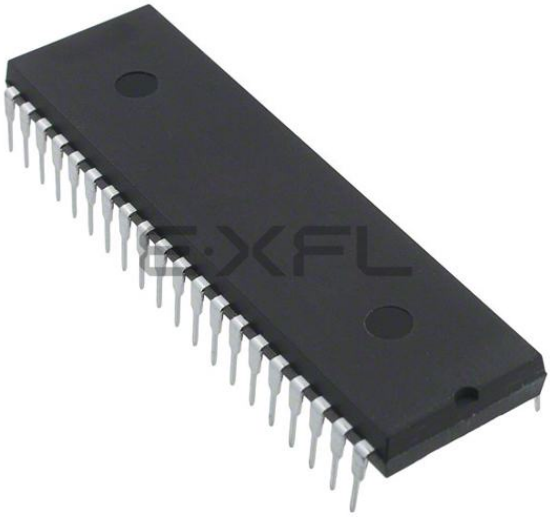

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	304 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchsc705c8acpe

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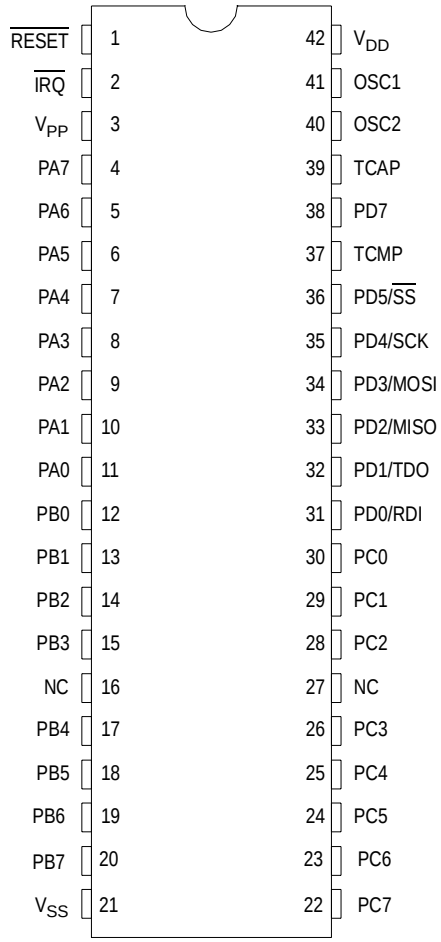

Figure 1-6. 42-Pin SDIP Pin Assignments

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	SPI Control Register (SPCR) See page 149.	Read:	SPIE	SPE		MSTR	CPOL	CPHA	SPR1	SPR0
		Write:								
		Reset:	0	0		0	U	U	U	U
$000B	SPI Status Register (SPSR) See page 151.	Read:	SPIF	WCOL		MODF				
		Write:								
		Reset:	0	0		0				
$000C	SPI Data Register (SPDR) See page 149.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	BIt 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							
$000D	Baud Rate Register (Baud) See page 136.	Read:			SCP1	SCP0		SCR2	SCR1	SCR0
		Write:								
		Reset:	U	U	0	0	U	U	U	U
$000E	SCI Control Register 1 (SCCR1) See page 130.	Read:	R8	T8		M	WAKE			
		Write:								
		Reset:	U	U		U	U			
$000F	SCI Control Register 2 (SCCR2) See page 131.	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0010	SCI Status Register (SCSR) See page 133.	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	
		Write:								
		Reset:	1	1	0	0	0	0	0	U
$0011	SCI Data Register (SCDR) See page 129.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							
$0012	Timer Control Register (TCR) See page 94.	Read:	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
		Write:								
		Reset:	0	0	0	0	0	0	U	0

= Unimplemented U = Unaffected

Figure 2-2. I/O Register Summary (Sheet 2 of 4)

3.3 CPU Registers

Figure 3-1 shows the five CPU registers. These are hard-wired registers within the CPU and are not part of the memory map.

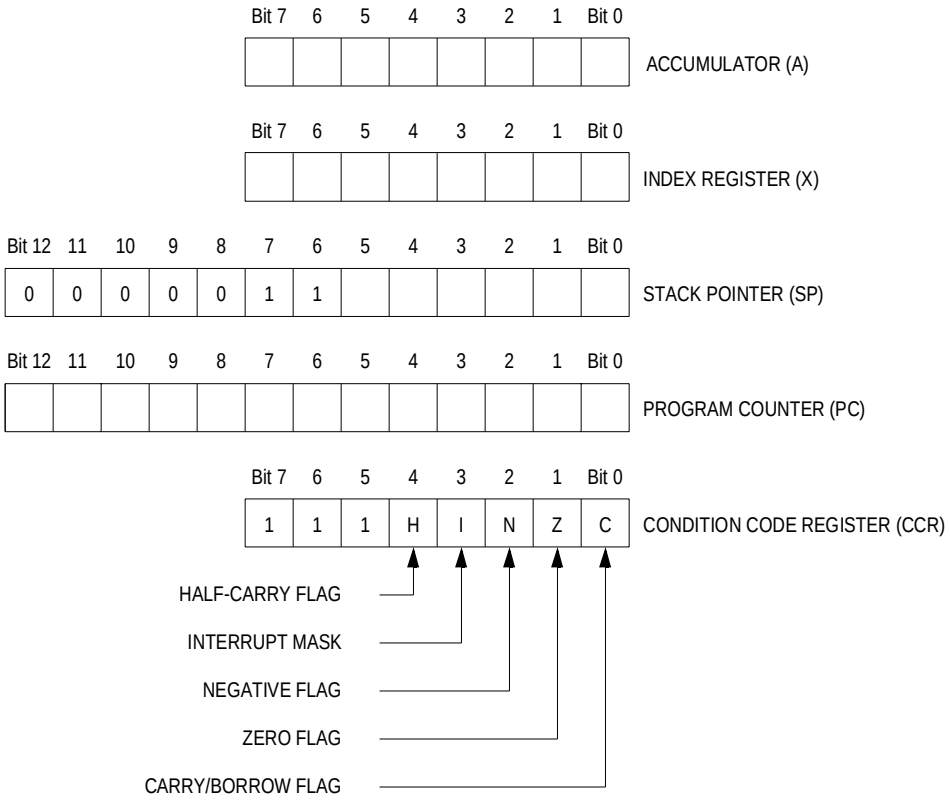

Figure 3-1. Programming Model

- **SCI Receiver Overrun Interrupt** — The overrun bit (OR) indicates that a received byte is lost because software has not read the previously received byte. OR becomes set when a byte shifts into the receive shift register before software reads the word already in the SCI data register. OR generates an interrupt request if the receive interrupt enable bit (RIE) is set also.
- **SCI Receiver Input Idle Interrupt** — The receiver input idle bit (IDLE) indicates that the SCI receiver input is not receiving data. IDLE becomes set when 10 or 11 consecutive logic 1s appear on the receiver input. IDLE generates an interrupt request if the idle line interrupt enable bit (ILIE) is set also.

4.3.6 SPI Interrupts

The serial peripheral interrupt (SPI) can generate these interrupts:

- SPI transmission complete interrupt
- SPI mode fault interrupt

Setting the I bit in the CCR disables all SPI interrupts.

- **SPI Transmission Complete Interrupt** — The SPI flag bit (SPIF) in the SPI status register indicates the completion of an SPI transmission. SPIF becomes set when a byte shifts into or out of the SPI data register. SPIF generates an interrupt request if the SPIE bit is set also.
- **SPI Mode Fault Interrupt** — The mode fault bit (MODF) in the SPI status register indicates an SPI mode error. MODF becomes set when a logic 0 occurs on the PD5/$\overline{SS}$ pin while the master bit (MSTR) in the SPI control register is set. MODF generates an interrupt request if the SPIE bit is set also.

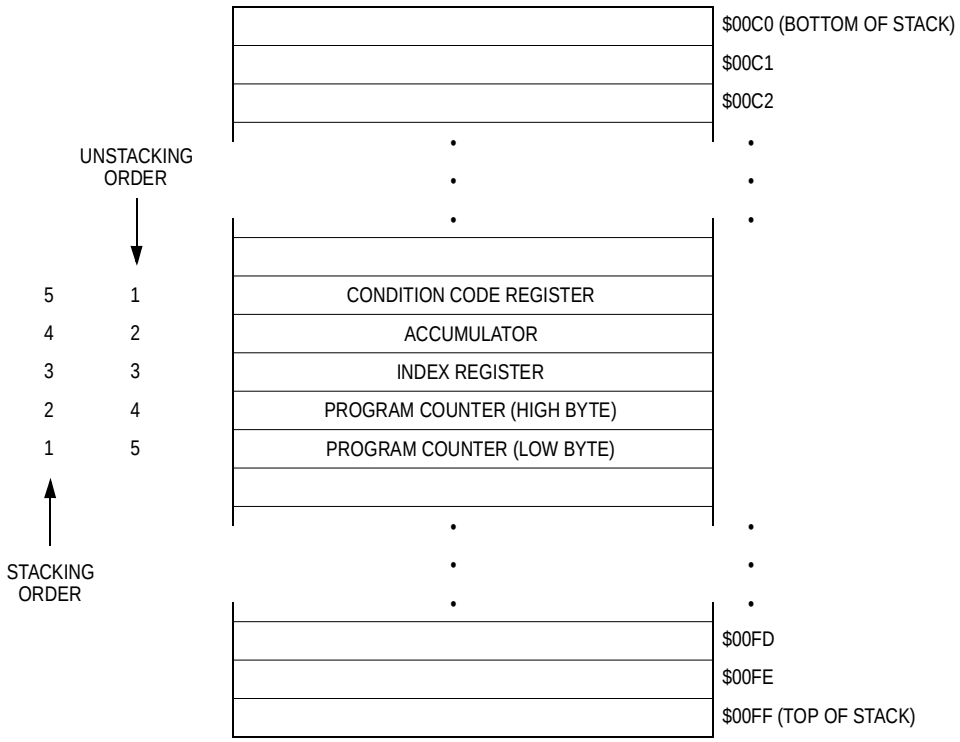

Figure 4-4. Interrupt Stacking Order

NOTE: *If more than one interrupt request is pending, the CPU fetches the vector of the higher priority interrupt first. A higher priority interrupt does not interrupt a lower priority interrupt service routine unless the lower priority interrupt service routine clears the I bit. See **Table 4-1** for a priority listing.*

Figure 4-5 shows the sequence of events caused by an interrupt.

2. COP clear bit (COPC) at address $1FF0

   To clear the non-programmable COP watchdog and start a new COP timeout period, write a logic 0 to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. See **9.5.2 Mask Option Register 1**.

NOTE: *The non-programmable watchdog COP is disabled in bootloader mode, even if the NCOPE bit is programmed.*

Figure 5-4 is a diagram of the non-programmable COP.

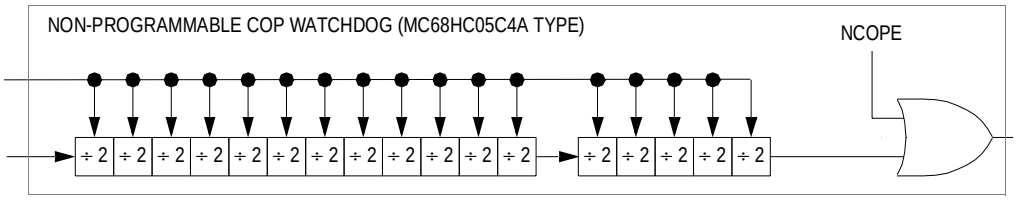

Figure 5-4. Non-Programmable COP Watchdog Diagram

5.3.4 Clock Monitor Reset

When the CME bit in the COP control register is set, the clock monitor detects the absence of the internal bus clock for a certain period of time. The timeout period depends on processing parameters and varies from 5 µs to 100 µs, which implies that systems using a bus clock rate of 200 kHz or less should not use the clock monitor function.

If a slow or absent clock is detected, the clock monitor causes a system reset. The reset is issued to the external system for four bus cycles using the bidirectional $\overline{\text{RESET}}$ pin.

Special consideration is required when using the STOP instruction with the clock monitor. Since STOP causes the system clocks to halt, the clock monitor issues a system reset when STOP is executed.

7.3.2 Data Direction Register A

The contents of data direction register A (DDRA) shown in **Figure 7-2** determine whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the associated port A pin; a logic 0 disables the output buffer. A reset clears all DDRA bits, configuring all port A pins as inputs.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 7-2. Data Direction Register A (DDRA)

DDRA7–DDRA0 — Port A Data Direction Bits

These read/write bits control port A data direction. Reset clears bits DDRA7–DDRA0.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE: *Avoid glitches on port A pins by writing to the port A data register before changing DDRA bits from logic 0 to logic 1.*

7.4 Port B

Port B is an 8-bit, general-purpose, bidirectional I/O port. Port B pins can also be configured to function as external interrupts. The port B pullup devices are enabled in mask option register 1 (MOR1). See **9.5.2 Mask Option Register 1** and **4.3.3 Port B Interrupts**.

7.4.1 Port B Data Register

The port B data register (PORTB) shown in **Figure 7-4** contains a data latch for each of the eight port B pins.

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Reset:	Unaffected by reset							

Figure 7-4. Port B Data Register (PORTB)

PB7–PB0 — Port B Data Bits

These read/write bits are software programmable. Data direction of each bit is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

7.4.3 Port B Logic

Figure 7-6 shows the port B I/O logic.

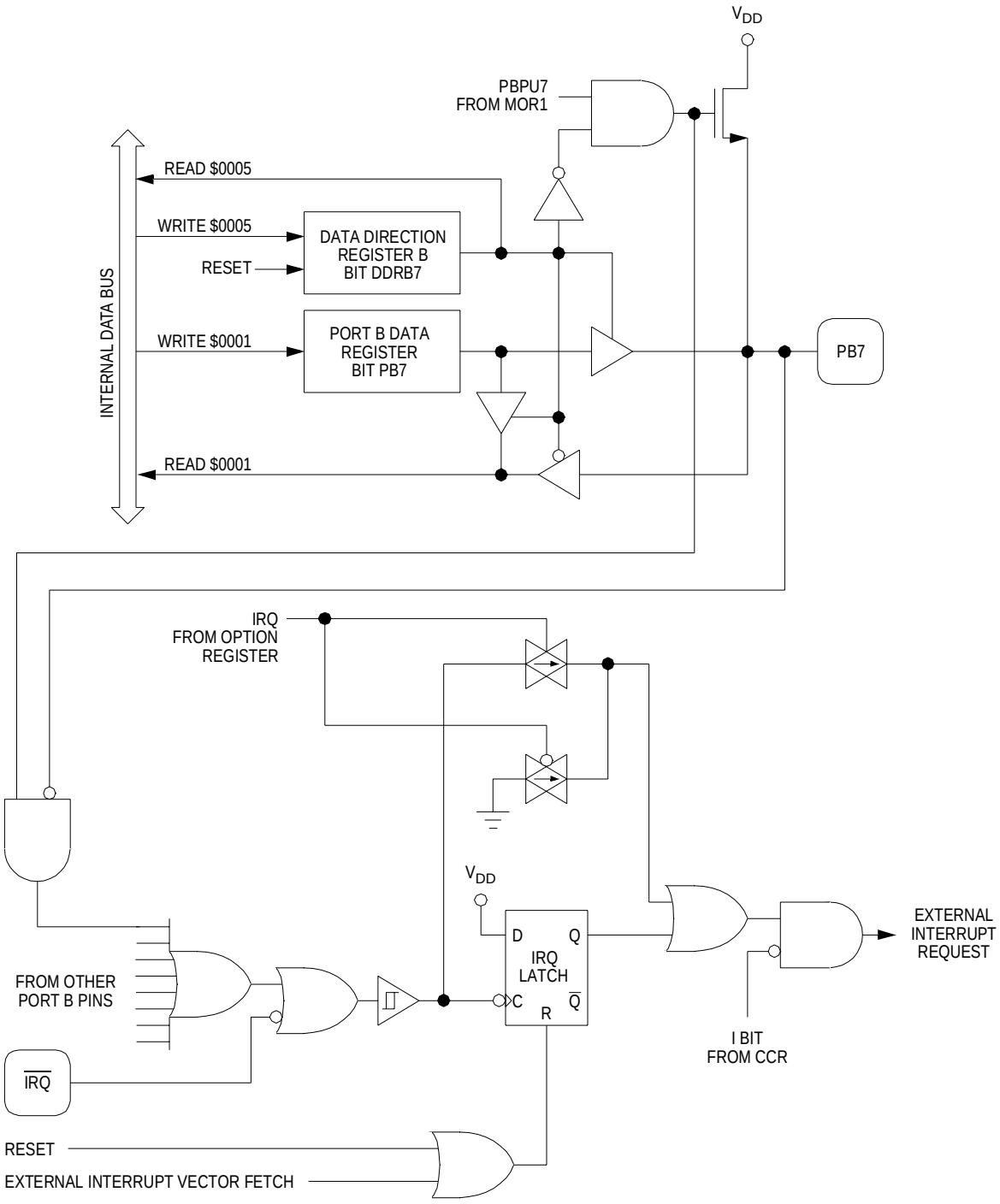

Figure 7-6. Port B I/O Logic

7.5.3 Port C Logic

Figure 7-9 shows port C I/O logic.

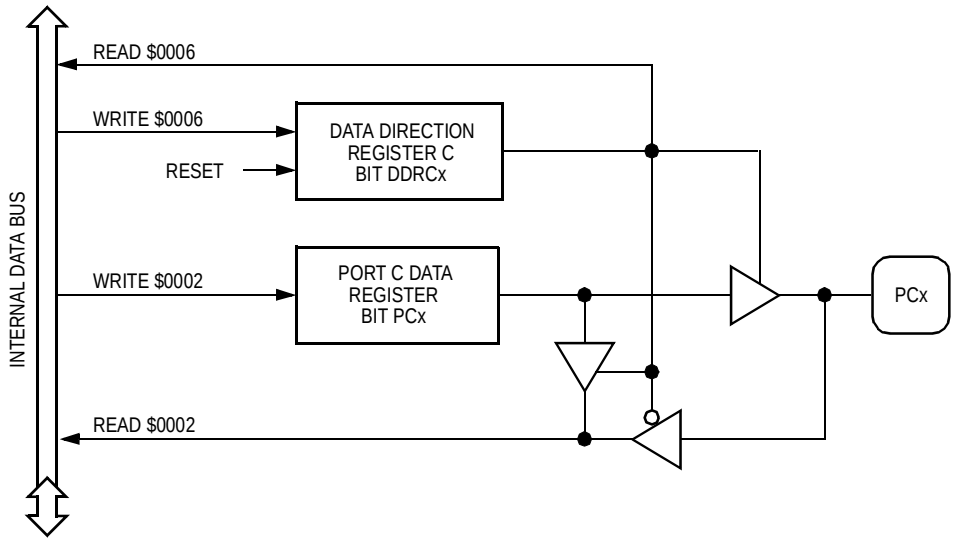

Figure 7-9. Port C I/O Logic

When a port C pin is programmed as an output, reading the port bit reads the value of the data latch and not the voltage on the pin. When a port C pin is programmed as an input, reading the port bit reads the voltage level on the pin. The data latch can always be written, regardless of the state of its DDRC bit. Table 7-3 summarizes the operation of the port C pins.

Table 7-3. Port C Pin Functions

DDRC Bit	I/O Pin Mode	Accesses to DDRC	Accesses to PORTC	
		Read/Write	Read	Write
0	Input, Hi-Z(1)	DDRC7–DDRC0	Pin	PC7–PC0(2)
1	Output	DDRC7–DDRC0	PC7–PC0	PC7–PC0

1. Hi-Z = high impedance
2. Writing affects data register but does not affect input.

NOTE: *To avoid excessive current draw, tie all unused input pins to V_{DD} or V_{SS} or change I/O pins to outputs by writing to DDRC in user code as early as possible.*

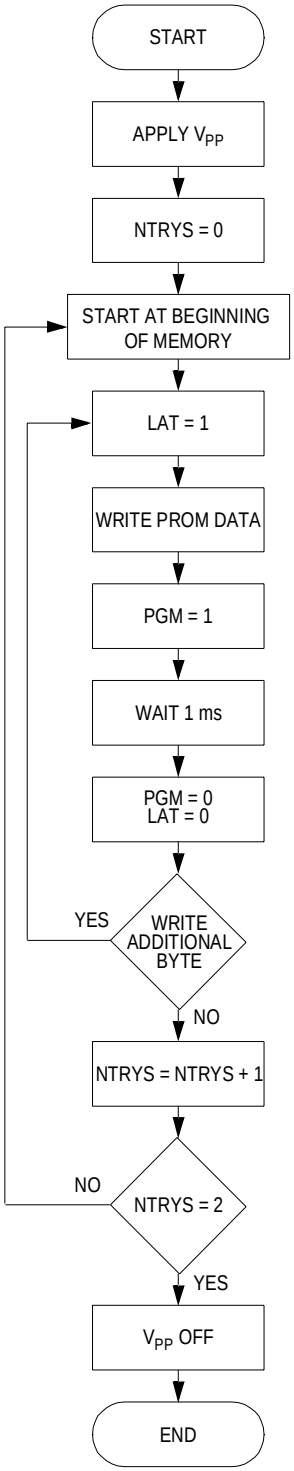

Figure 9-1. EPROM/OTPROM Programming Flowchart

9.3.1 Program Register

The program register (PROG) shown in **Figure 9-3** is used for PROM programming.

Address: $001C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	0	0	0	LAT	0	PGM
Reset:	0	0	0	0	0	0	0	0

Figure 9-3. Program Register (PROG)

LAT — Latch Enable Bit

This bit is both readable and writable.

1 = Enables PROM data and address bus latches for programming on the next byte write cycle

0 = Latch disabled. PROM data and address buses are unlatched for normal CPU operations.

PGM — Program Bit

If LAT is cleared, PGM cannot be set.

1 = Enables V_{PP} power to the PROM for programming

0 = V_{PP} is disabled.

Bits 1 and 3–7 — Not used; always read 0

9.4 PROM Programming Routines

This subsection describes the routines necessary to program, verify, and secure the PROM device, and other routines available to the user.

9.4.1 Program and Verify PROM

The program and verify PROM routine copies the contents of the external EPROM into the MCU PROM with direct correspondence between the addresses. Memory addresses in the MCU that are not implemented in PROM are skipped. Unprogrammed addresses in the EPROM being copied should contain $00 bytes to speed up the programming process.

To run the program and verify the PROM routine on the PROM MCU, take these steps:

1. Set switch 1 in the ON position (restores V_{DD}).
2. Restore the V_{PP} power source.
3. Set switches S3, S4, S5, and S6 in the OFF position (selects proper routine).
4. Set switch 2 in the OUT position (routine is activated).

   The red light-emitting diode (LED) is illuminated, showing that the programming part of the routine is running. The LED goes out when programming is finished. The verification part of the routine now begins. When the green LED is illuminated, verification is successfully completed and the routine is finished.
5. Set switch 2 in the RESET position.

At this point, if no other MCU is to be programmed or secured, remove V_{PP} power from the board. If another routine is to be performed on the MCU being programmed, the user can then set switches S3, S4, S5, and S6 to the positions necessary to select the next routine, and begin the routine by setting switch 2 to the OUT position. If no other routine is to be performed, remove V_{DD} from the board and remove the MCU from the programming socket.

10.6.5 Baud Rate Register

The baud rate register shown in **Figure 10-9** selects the baud rate for both the receiver and the transmitter.

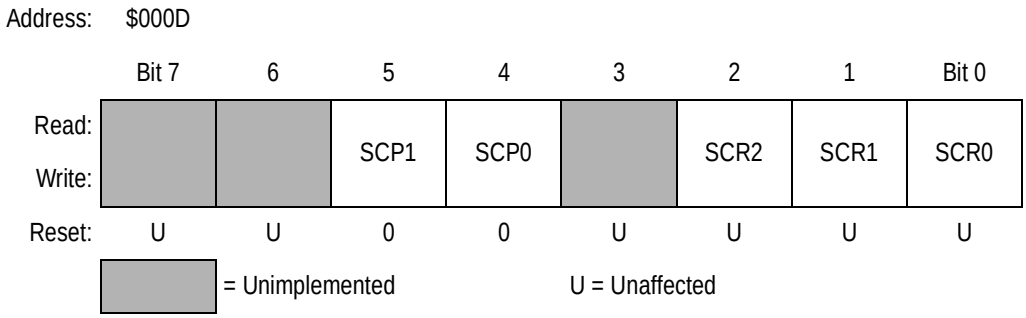

Figure 10-9. Baud Rate Register (Baud)

SCP1 and SCP0 — SCI Prescaler Select Bits

These read/write bits control prescaling of the baud rate generator clock, as shown in **Table 10-1**. Resets clear both SCP1 and SCP0.

Table 10-1. Baud Rate Generator Clock Prescaling

SCP[1:0]	Baud Rate Generator Clock
00	Internal clock ÷ 1
01	Internal clock ÷ 3
10	Internal clock ÷ 4
11	Internal clock ÷ 13

MODF — Mode Fault Bit

This clearable, read-only bit is set when a logic 0 occurs on the PD5/$\overline{SS}$ pin while the MSTR bit is set. MODF generates an interrupt request if the SPIE bit is also set. Clear the MODF bit by reading the SPSR with MODF set and then writing to the SPCR. Reset clears MODF.

1 = PD5/$\overline{SS}$ pulled low while MSTR bit set
0 = PD5/$\overline{SS}$ not pulled low while MSTR bit set

12.3.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

12.3.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

12.3.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address.

12.3.4 Extended

Extended instructions use three bytes and can access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Motorola assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

13.3 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table here. Keep V_{In} and V_{Out} within the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{In}	V_{SS} –0.3 to V_{DD} +0.3	V
Programming voltage	V_{PP}	V_{DD} –0.3 to 16.0	
Bootstrap mode ($\overline{IRQ}$ pin only)	V_{In}	V_{SS} – 0.3 to 2 x V_{DD} + 0.3	V
Current drain per pin excluding V_{DD} and V_{SS}	I	25	mA
Storage temperature range	T_{STG}	–65 to +150	°C

1. Voltages referenced to V_{SS}

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***13.7 5.0-Volt DC Electrical Characteristics*** *and* ***13.8 3.3-Volt DC Electrical Characteristics*** *for guaranteed operating conditions.*

A.7 5.0-Volt High-Speed SPI Timing

Diagram Number[1]	Characteristic[2]	Symbol	Min	Max	Unit
	Operating frequency Master Slave	$f_{OP(S)}$ $f_{OP(S)}$	dc dc	0.5 4.0	f_{OP} MHz
1	Cycle time Master Slave	$t_{CYC(M)}$ $t_{CYC(S)}$	2.0 250	— —	t_{CYC} ns
2	Enable lead time Master Slave	$t_{Lead(M)}$ $t_{Lead(S)}$	Note [3] 125	— —	ns
3	Enable lag time Master Slave	$t_{Lag(M)}$ $t_{Lag(S)}$	Note[2] 375	— —	ns
4	Clock (SCK) high time Master Slave	$t_{W(SCKH)M}$ $t_{W(SCKH)S}$	170 95	— —	ns
5	Clock (SCK) low time Master Slave	$t_{W(SCKL)M}$ $t_{W(SCKL)S}$	170 95	— —	ns
6	Data setup time (inputs) Master Slave	$t_{SU(M)}$ $t_{SU(S)}$	50 50	— —	ns
7	Data hold time (inputs) Master Slave	$t_{H(M)}$ $t_{H(S)}$	50 50	— —	ns
8	Access time[4] Slave	t_A	0	60	ns
9	Disable time[5] Slave	t_{DIS}	—	120	ns
10	Data valid time Master (before capture edge) Slave (after enable edge)[6]	$t_{V(M)}$ $t_{V(S)}$	0.25 —	— 120	$t_{CYC(M)}$ ns

Continued