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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC G4 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.0GHz |
| Co-Processors/DSP | Multimedia; SIMD |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.5V, 1.8V, 2.5V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 483-BCBGA, FCCBGA |
| Supplier Device Package | 483-FCCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7457rx1000nc |

- Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
- Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions

- Four integer units (IUs) that share 32 GPRs for integer operands
  - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions
  - IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions
- Five-stage FPU and a 32-entry FPR file
  - Fully IEEE 754-1985 compliant FPU for both single- and double-precision operations
  - Supports non-IEEE mode for time-critical operations
  - Hardware support for denormalized numbers
  - Thirty-two 64-bit FPRs for single- or double-precision operands
- Four vector units and 32-entry vector register file (VRs)
  - Vector permute unit (VPU)
  - Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**)
  - Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**)
  - Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half-word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - Dedicated adder calculates effective addresses (EAs)
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues FIQ, VIQ, and GIQ can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can be dispatched only from the three lowest IQ entries—IQ0, IQ1, and IQ2
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle

**Table 5. Package Thermal Characteristics [1] (continued)**

| Characteristic | Symbol | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | MPC7447 | MPC7457 | | |
| Coefficient of thermal expansion | | 6.8 | 6.8 | ppm/°C | |

**Notes**:
1. Refer to Section 9.8, "Thermal Management Information," for more details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7457.

**Table 6. DC Electrical Specifications**

At recommended operating conditions. See Table 4.

| Characteristic | Nominal Bus Voltage [1] | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage (all inputs including SYSCLK) | 1.5 | $V_{IH}$ | $GV_{DD} \times 0.65$ | $GV_{DD} + 0.3$ | V | 2 |
| | 1.8 | | $OV_{DD}/GV_{DD} \times 0.65$ | $OV_{DD}/GV_{DD} + 0.3$ | V | |
| | 2.5 | | 1.7 | $OV_{DD}/GV_{DD} + 0.3$ | V | |
| Input low voltage (all inputs including SYSCLK) | 1.5 | $V_{IL}$ | –0.3 | $GV_{DD} \times 0.35$ | V | 2, 6 |
| | 1.8 | | –0.3 | $OV_{DD}/GV_{DD} \times 0.35$ | V | |
| | 2.5 | | –0.3 | 0.7 | V | |
| Input leakage current, $V_{in} = GV_{DD}/OV_{DD}$ | — | $I_{in}$ | — | 30 | µA | 2, 3 |
| High-impedance (off-state) leakage current, $V_{in} = GV_{DD}/OV_{DD}$ | — | $I_{TSI}$ | — | 30 | µA | 2, 3, 4 |
| Output high voltage, $I_{OH} = –5$ mA | 1.5 | $V_{OH}$ | $OV_{DD}/GV_{DD} – 0.45$ | — | V | 6 |
| | 1.8 | | $OV_{DD}/GV_{DD} – 0.45$ | — | V | |
| | 2.5 | | 1.8 | — | V | |
| Output low voltage, $I_{OL} = 5$ mA | 1.5 | $V_{OL}$ | — | 0.45 | V | 6 |
| | 1.8 | | — | 0.45 | V | |
| | 2.5 | | — | 0.6 | V | |

**Table 8. Clock AC Timing Specifications (continued)**

At recommended operating conditions. See Table 4.

| Characteristic | Symbol | Maximum Processor Core Frequency | | | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 867 MHz | | 1000 MHz | | 1200 MHz | | 1267 MHz | | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Internal PLL relock time | | — | 100 | — | 100 | — | 100 | — | 100 | µs | 7 |

**Notes**:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, “PLL Configuration,” for valid PLL_CFG[0:4] settings.
2. Assumes lightly-loaded, single-processor system; see Section 5.2.1, “Clock AC Specifications” for more information.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver’s closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable $V_{DD}$ and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

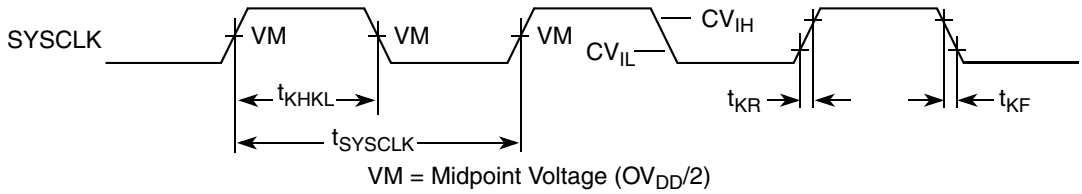



**Figure 3. SYSCLK Input Timing Diagram**

## 5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 as defined in Figure 4 and Figure 5. Timing specifications for the L3 bus are provided in Section 5.2.3, “L3 Clock AC Specifications.”

**Table 10. L3_CLK Output AC Timing Specifications (continued)**

At recommended operating conditions. See Table 4.

| Parameter | Symbol | Device Revision (L3 I/O Voltage) [6] | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode) | | | Rev 1.2 (1.8-, 2.5-V I/O Modes) | | | | |
| | | Min | Typ | Max | Min | Typ | Max | | |
| L3 clock jitter | | — | — | ± 75 | — | — | ± 75 | ps | 5 |

**Notes**:

1. The maximum L3 clock frequency (and minimum L3 clock period) will be system dependent. See Section 5.2.3, "L3 Clock AC Specifications," for an explanation that this maximum frequency is not functionally tested at speed by Freescale. The minimum L3 clock frequency and period are $f_{SYSCLK}$ and $t_{SYSCLK}$, respectively.
2. The nominal duty cycle of the L3 output clocks is 50% measured at midpoint voltage.
3. Maximum possible skew between L3_CLK0 and L3_CLK1. This parameter is critical to the address and control signals which are common to both SRAM chips in the L3.
4. Maximum possible skew between L3_CLK0 and L3_ECHO_CLK1 or between L3_CLK1 and L3_ECHO_CLK3 for PB2 or Late Write SRAM. This parameter is critical to the read data signals because the processor uses the feedback loop to latch data driven from the SRAM, each of which drives data based on L3_CLK0 or L3_CLK1.
5. Guaranteed by design and not tested. The input jitter on SYSCLK affects L3 output clocks and the L3 address, data, and control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L3 timing analysis. The clock-to-clock jitter shown here is uncertainty in the internal clock period caused by supply voltage noise or thermal effects. This is also comprehended in the AC timing specifications and need not be considered in the L3 timing analysis.
6. L3 I/O voltage mode must be configured by L3VSEL as described in Table 3, and voltage supplied at $GV_{DD}$ must match mode selected as specified in Table 4. See Table 22 for revision level information and part marking.

The L3_CLK timing diagram is shown in Figure 7.

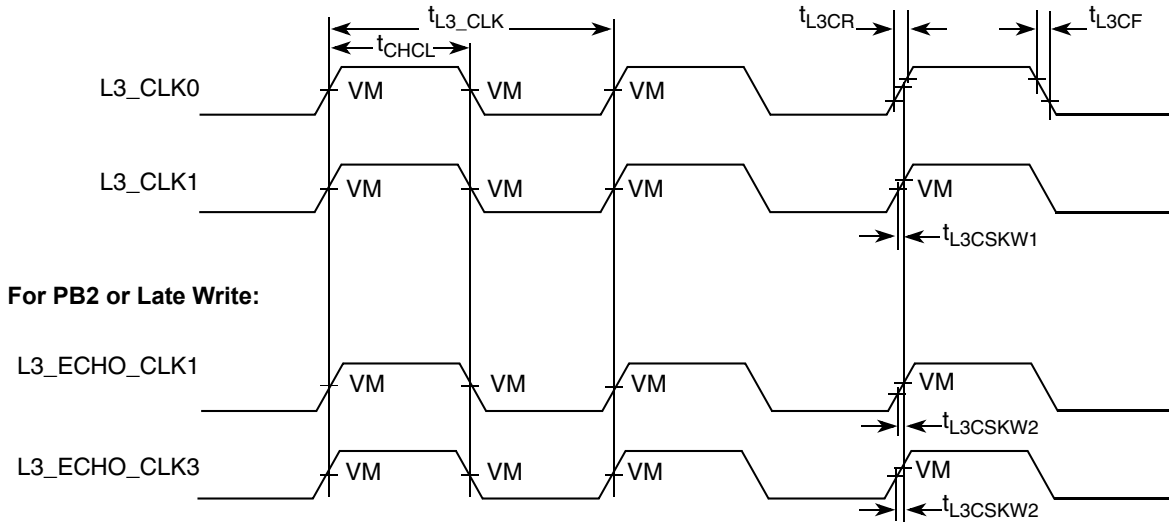
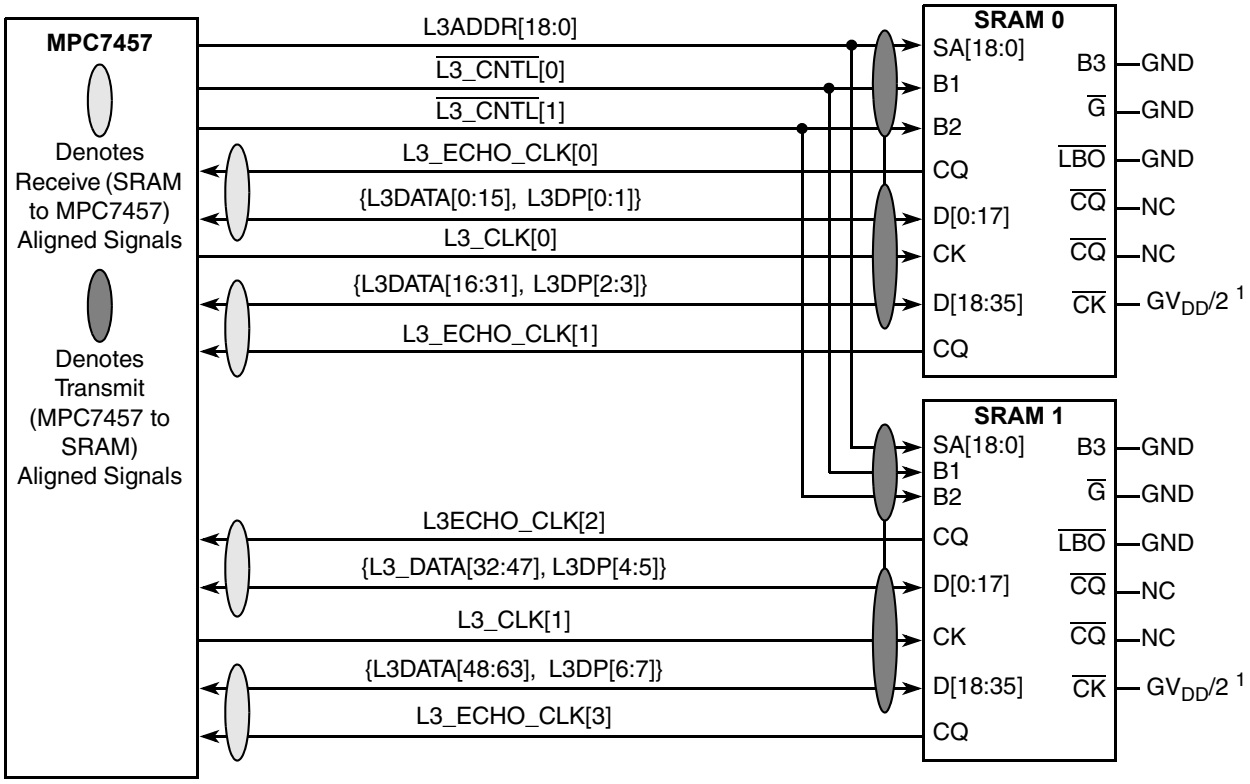



**Figure 7. L3_CLK_OUT Output Timing Diagram**

Figure 9 shows the typical connection diagram for the MPC7457 interfaced to MSUG2 DDR SRAMs.

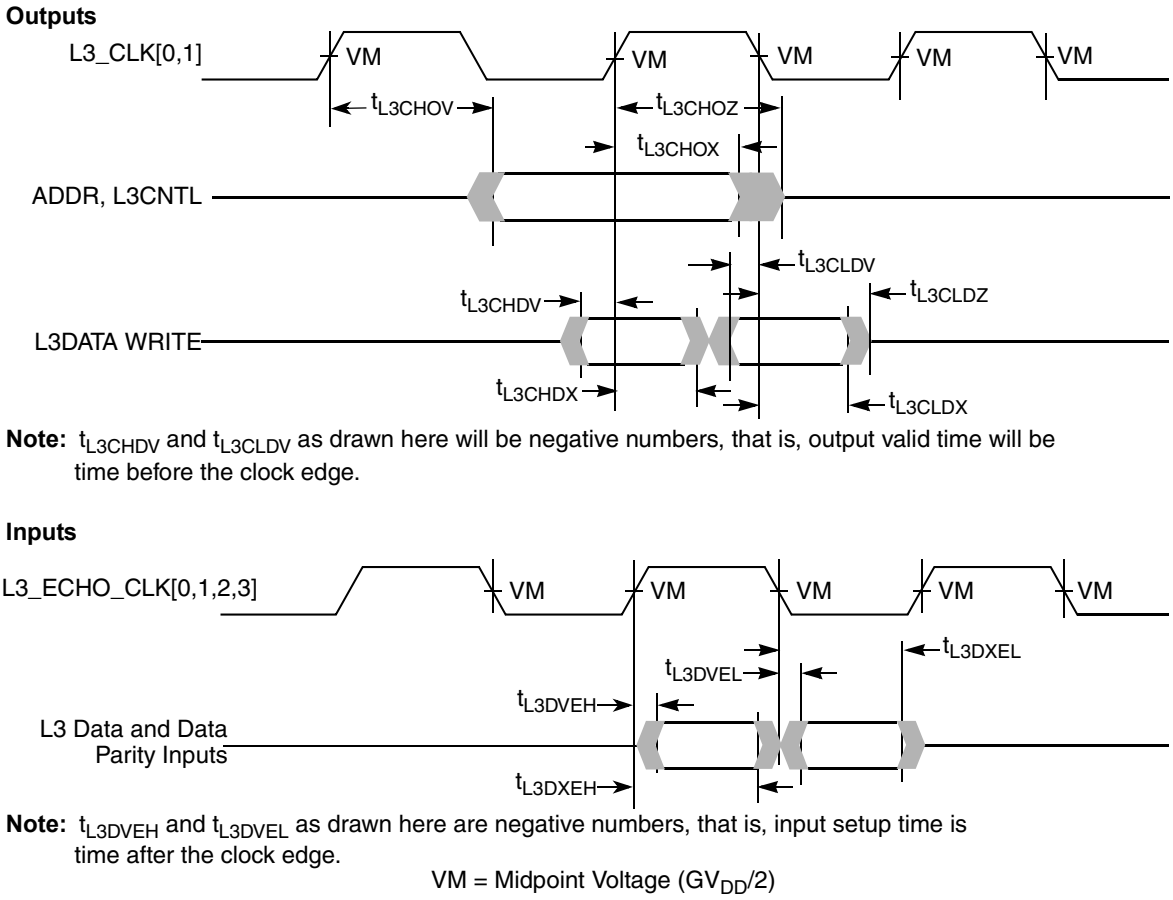



**Note:**

1. Or as recommended by SRAM manufacturer for single-ended clocking.

**Figure 9. Typical Source Synchronous 4-Mbyte L3 Cache DDR Interface**

Figure 10 shows the L3 bus timing diagrams for the MPC7457 interfaced to MSUG2 SRAMs.




**Note:** $t_{L3CHDV}$ and $t_{L3CLDV}$ as drawn here will be negative numbers, that is, output valid time will be time before the clock edge.

**Note:** $t_{L3DVEH}$ and $t_{L3DVEL}$ as drawn here are negative numbers, that is, input setup time is time after the clock edge.

VM = Midpoint Voltage ($GV_{DD}/2$)

**Figure 10. L3 Bus Timing Diagrams for L3 Cache DDR SRAMs**

### 5.2.4.3 L3 Bus AC Specifications for PB2 and Late Write SRAMs

When using PB2 or Late Write SRAMs at the L3 interface, the parts should be connected as shown in Figure 11. These SRAMs are synchronous to the MPC7457; one L3_CLK*n* signal is output to each SRAM to latch address, control, and write data. Read data is launched by the SRAM synchronous to the delayed L3_CLK*n* signal it received. The MPC7457 needs a copy of that delayed clock which launched the SRAM read data to know when the returning data will be valid. Therefore, L3_ECHO_CLK1 and L3_ECHO_CLK3 must be routed halfway to the SRAMs and returned to the MPC7457 inputs L3_ECHO_CLK0 and L3_ECHO_CLK2, respectively. Thus, L3_ECHO_CLK0 and L3_ECHO_CLK2 are phase-aligned with the input clock received at the SRAMs. The MPC7457 will latch the incoming data on the rising edge of L3_ECHO_CLK0 and L3_ECHO_CLK2.

Table 14 provides the L3 bus interface AC timing specifications for the configuration shown in Figure 11, assuming the timing relationships of Figure 12 and the loading of Figure 8.

### Table 14. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs

At recommended operating conditions. See Table 4.

| Parameter | Symbol | All Revisions and L3 I/O Voltage Modes | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| L3_CLK rise and fall time | $t_{L3CR}$, $t_{L3CF}$ | — | 0.75 | ns | 1, 2 |
| Setup times: Data and parity | $t_{L3DVEH}$ | 0.1 | — | ns | 2, 3 |
| Input hold times: Data and parity | $t_{L3DXEH}$ | 0.7 | — | ns | 2, 3 |
| Valid times: Data and parity | $t_{L3CHDV}$ | — | 2.5 | ns | 2, 4, 5 |
| Valid times: All other outputs | $t_{L3CHOV}$ | — | 1.8 | ns | 5 |
| Output hold times: Data and parity | $t_{L3CHDX}$ | 1.4 | — | ns | 2, 4, 5 |
| Output hold times: All other outputs | $t_{L3CHOX}$ | 1.0 | — | ns | 2, 5 |
| L3_CLK to high impedance: Data and parity | $t_{L3CHDZ}$ | — | 3.0 | ns | 2 |
| L3_CLK to high impedance: All other outputs | $t_{L3CHOZ}$ | — | 3.0 | ns | 2 |

**Notes**:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of $GV_{DD}$.
2. Timing behavior and characterization are currently being evaluated.
3. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
4. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLK*n* to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
5. Assumes default value of L3OHCR. See Section 5.2.4.1, “Effects of L3OHCR Settings on L3 Bus AC Specifications,” for more information.

**Table 16. Pinout Listing for the MPC7447, 360 CBGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Select [1] | Notes |
|---|---|---|---|---|---|
| $\overline{\text{TEA}}$ | L1 | Low | Input | BVSEL | |
| TEST[0:3] | A12, B6, B10, E10 | — | Input | BVSEL | 12 |
| TEST[4] | D10 | — | Input | BVSEL | 9 |
| TMS | F1 | High | Input | BVSEL | 6 |
| $\overline{\text{TRST}}$ | A5 | Low | Input | BVSEL | 6, 14 |
| $\overline{\text{TS}}$ | L4 | Low | I/O | BVSEL | 3 |
| TSIZ[0:2] | G6, F7, E7 | High | Output | BVSEL | |
| TT[0:4] | E5, E6, F6, E9, C5 | High | I/O | BVSEL | |
| $\overline{\text{WT}}$ | D3 | Low | Output | BVSEL | |
| $V_{DD}$ | H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12 | — | — | N/A | |

**Notes:**

1. $OV_{DD}$ supplies power to the processor bus, JTAG, and all control signals; and $V_{DD}$ supplies power to the processor core and the PLL (after filtering to become $AV_{DD}$). To program the I/O voltage, connect BVSEL to either GND (selects 1.8 V) or to $\overline{\text{HRESET}}$ (selects 2.5 V). If used, the pull-down resistor should be less than 250 Ω. For actual recommended value of $V_{in}$ or supply voltages see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7447 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to $OV_{DD}$ or negation by $\neg\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7447 is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation.
12. These input signals are for factory use only and must be pulled up to $OV_{DD}$ for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.

**Table 17. Pinout Listing for the MPC7457, 483 CBGA Package**

| Signal Name | Pin Number | Active | I/O | I/F Select [1] | Notes |
|---|---|---|---|---|---|
| A[0:35] | E10, N4, E8, N5, C8, R2, A7, M2, A6, M1, A10, U2, N2, P8, M8, W4, N6, U6, R5, Y4, P1, P4, R6, M7, N7, AA3, U4, W2, W1, W3, V4, AA1, D10, J4, G10, D9 | High | I/O | BVSEL | 2 |
| $\overline{\text{AACK}}$ | U1 | Low | Input | BVSEL | |
| AP[0:4] | L5, L6, J1, H2, G5 | High | I/O | BVSEL | |
| $\overline{\text{ARTRY}}$ | T2 | Low | I/O | BVSEL | 3 |

**Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Select [1] | Notes |
|---|---|---|---|---|---|
| TDI | E4 | High | Input | BVSEL | 7 |
| TDO | H1 | High | Output | BVSEL | |
| $\overline{\text{TEA}}$ | T1 | Low | Input | BVSEL | |
| TEST[0:5] | B10, H6, H10, D8, F9, F8 | — | Input | BVSEL | 13 |
| TEST[6] | A9 | — | Input | BVSEL | 10 |
| TMS | K4 | High | Input | BVSEL | 7 |
| $\overline{\text{TRST}}$ | C1 | Low | Input | BVSEL | 7, 16 |
| $\overline{\text{TS}}$ | P5 | Low | I/O | BVSEL | 3 |
| TSIZ[0:2] | L1,H3,D1 | High | Output | BVSEL | |
| TT[0:4] | F1, F4, K8, A5, E1 | High | I/O | BVSEL | |
| $\overline{\text{WT}}$ | L2 | Low | Output | BVSEL | |
| $V_{DD}$ | J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14 | — | — | N/A | |
| VDD_SENSE[0:1] | G11, J8 | — | — | N/A | 17 |

**Notes:**

1. $OV_{DD}$ supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); $GV_{DD}$ supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals $\overline{\text{L3\_CNTL}}$[0:1]; and $V_{DD}$ supplies power to the processor core and the PLL (after filtering to become $AV_{DD}$). For actual recommended value of $V_{in}$ or supply voltages, see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to $OV_{DD}$ or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. See Table 3 for bus voltage configuration information. If used, pull-down resistors should be less than 250 Ω.
7. Internal pull up on die.
8. Ignored in 60x bus mode.
9. These signals must be pulled down to GND if unused or if the MPC7457 is in 60x bus mode.
10. These input signals for factory use only and must be pulled down to GND for normal machine operation.
11. Power must be supplied to $GV_{DD}$, even when the L3 interface is disabled or unused.
12. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These input signals are for factory use only and must be pulled up to $OV_{DD}$ for normal machine operation.
14. These signals are for factory use only and must be left unconnected for normal machine operation.
15. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
16. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
17. These pins are internally connected to $V_{DD}$. They are intended to allow an external device to detect the core voltage level present at the processor core. If unused, they must be connected directly to $V_{DD}$ or left unconnected.

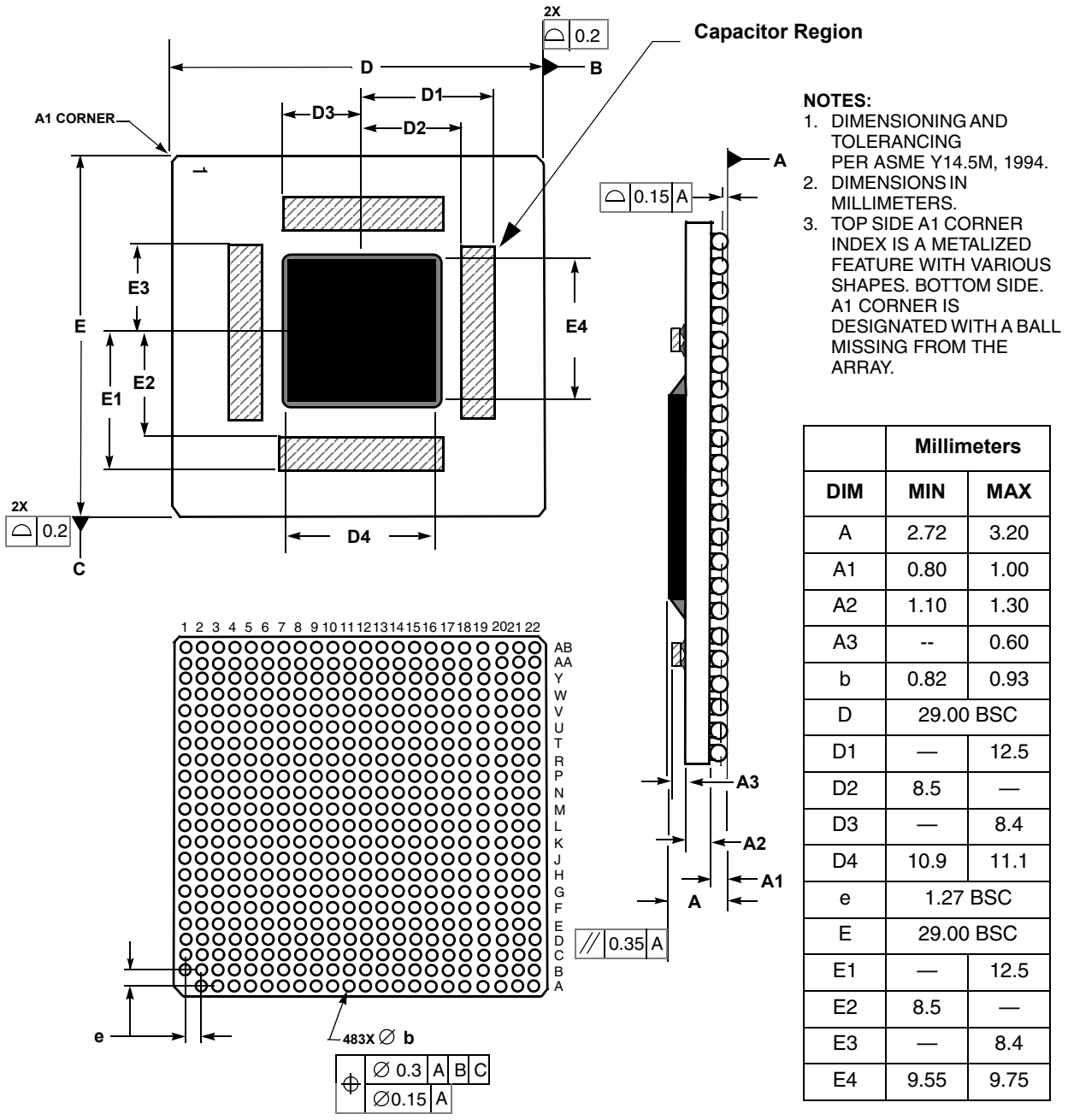
## 8.4 Package Parameters for the MPC7457, 483 CBGA or RoHS BGA

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483 ceramic ball grid array (CBGA).

| | |
|---|---|
| Package outline | 29 × 29 mm |
| Interconnects | 483 (22 × 22 ball array – 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | — |
| Maximum module height | 3.22 mm |
| Ball diameter | 0.89 mm (35 mil) |

## 8.5 Mechanical Dimensions for the MPC7457, 483 CBGA or RoHS BGA

Figure 22 provides the mechanical dimensions and bottom surface nomenclature for the MPC7457, 483 CBGA package.




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE. A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

| | Millimeters | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.72 | 3.20 |
| A1 | 0.80 | 1.00 |
| A2 | 1.10 | 1.30 |
| A3 | -- | 0.60 |
| b | 0.82 | 0.93 |
| D | 29.00 BSC | |
| D1 | — | 12.5 |
| D2 | 8.5 | — |
| D3 | — | 8.4 |
| D4 | 10.9 | 11.1 |
| e | 1.27 BSC | |
| E | 29.00 BSC | |
| E1 | — | 12.5 |
| E2 | 8.5 | — |
| E3 | — | 8.4 |
| E4 | 9.55 | 9.75 |

**Figure 22. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7457, 483 CBGA or RoHS BGA Package**

**Table 21. Impedance Characteristics**
$V_{DD}$ = 1.5 V, $OV_{DD}$ = 1.8 V ± 5%, $T_j$ = 5°–85°C

| Impedance | | Processor Bus | L3 Bus | Unit |
|---|---|---|---|---|
| $Z_0$ | Typical | 33–42 | 34–42 | Ω |
| | Maximum | 31–51 | 32–44 | Ω |

## 9.6 Pull-Up/Pull-Down Resistor Requirements

The MPC7457 requires high-resistive (weak: 4.7-kΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being for factory test must be pulled up to $OV_{DD}$ or down to GND to ensure proper device operation. For the MPC7447, 360 BGA, the pins that must be pulled up to $OV_{DD}$ are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. For the MPC7457, 483 BGA, the pins that must be pulled up to $OV_{DD}$ are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:5]; the pins that must be pulled down are: L1_TSTCLK and TEST[6]. The $\overline{\text{CKSTP\_IN}}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 kΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7457 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 kΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

If pull-down resistors are used to configure BVSEL or L3VSEL, the resistors should be less than 250 Ω (see Table 16). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7457 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7457 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information about this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7457 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If extended addressing is not used, A[0:3] are unused and must be pulled low to GND through weak pull-down resistors. If the MPC7457 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L3 interface does not normally require pull-up resistors. Unused L3_ADDR signals are driven low when the SRAM is configured to be less than 1 M in size via L3CR. For example, L3_ADD[18] will be driven low if the SRAM size is configured to be 2 M; likewise, L3_ADDR[18:17] will be driven low if the SRAM size is configured to be 1 M.

## 9.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 26 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

| | |
|---|---|
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105-3668<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-5102 |

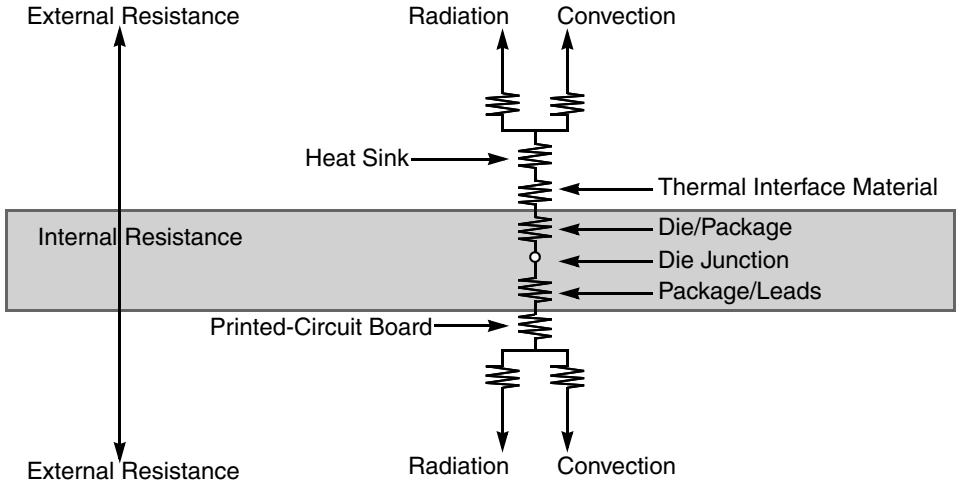
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

### 9.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (actually top-of-die since silicon die is exposed) thermal resistance
- The die junction-to-ball thermal resistance

Figure 28 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.




(Note the internal versus external package resistance.)

**Figure 28. C4 Package with Heat Sink Mounted to a Printed-Circuit Board**

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

example, assuming a $T_a$ of 30°C, a $T_r$ of 5°C, a CBGA package $R_{\theta JC}$ = 0.1, and a typical power consumption ($P_d$) of 18.7 W, the following expression for $T_j$ is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 18.7\ W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the MPC7447 and MPC7457 thermal model is shown in Figure 30. Four volumes will be used to represent this device. Two of the volumes, solder ball, and air and substrate, are modeled using the package outline size of the package. The other two, die, and bump and underfill, have the same size as the die. The silicon die should be modeled 9.64 × 11.0 × 0.74 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 9.64 × 11.0 × 0.069 mm (or as a collapsed volume) with orthotropic material properties: 0.6 W/(m • K) in the xy-plane and 2 W/(m • K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm (MPC7447) or 29 × 29 × 1.2 mm (MPC7457), and this volume has 18 W/(m • K) isotropic conductivity. The solder ball and air layer is modeled with the same horizontal dimensions as the substrate and is 0.9 mm thick. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 3.8 W/(m • K) in the direction of the z-axis.

| Conductivity | Value | Unit |
|---|---|---|
| **Bump and Underfill** | | |
| $k_x$ | 0.6 | W/(m • K) |
| $k_y$ | 0.6 | |
| $k_z$ | 2 | |
| **Substrate** | | |
| k | 18 | |
| **Solder Ball and Air** | | |
| $k_x$ | 0.034 | |
| $k_y$ | 0.034 | |
| $k_z$ | 3.8 | |

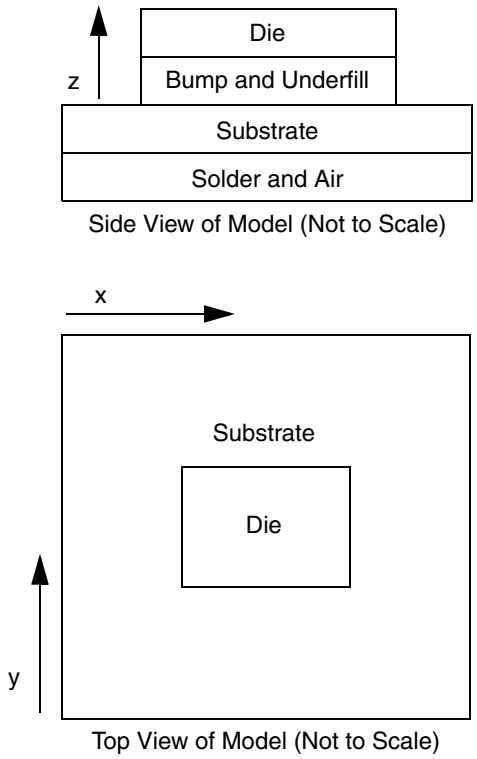



**Figure 30. Recommended Thermal Model of MPC7447 and MPC7457**

# 10 Part Numbering and Marking

Ordering information for the parts fully covered by this specification document is provided in Section 10.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision level code which refers to the die mask revision number. Section 10.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a referred to as a hardware specification addendum.

## 10.1 Part Numbers Fully Addressed by This Document

Table 22 provides the Freescale part numbering nomenclature for the MPC7457.

**Table 22. Part Numbering Nomenclature**

| MC | 74*x*7 | *xx* | *nnnn* | L | *x* |
|---|---|---|---|---|---|

| Product Code | Part Identifier | Package | Processor Frequency [1] | Application Modifier | Revision Level |
|---|---|---|---|---|---|
| PPC [2]<br>MC | 7457<br>7447 | RX = CBGA | 867<br>1000<br>1200<br>1267 | L: 1.3 V ± 50 mV<br>0° to 105°C | B: 1.1; PVR = 8002 0101 |
| MC | 7457 | RX = CBGA<br>VG = RoHS BGA | 867<br>1000<br>1200<br>1267 | | C: 1.2; PVR = 8002 0102 |

**Notes:**

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by a hardware specification addendum may support other maximum core frequencies.
2. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

## 10.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed are described in a separate addendum, which supplement and supersede this hardware specification. As such parts are released, these specifications will be listed in this section.

**Table 23. Part Numbers Addressed by MPC74x7RX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS01AD)**

| MC | 74*x*7 | *xx* | *nnnn* | N | *x* |
|---|---|---|---|---|---|

| Product Code | Part Identifier | Package | Processor Frequency | Application Modifier | Revision Level |
|---|---|---|---|---|---|
| PPC | 7457 | RX = CBGA | 1000<br>867<br>733<br>600 | N: 1.1 V ± 50 mV<br>0° to 105°C | B: 1.1; PVR = 8002 0101 |
| | 7447 | | 1000<br>867 | | |
| MC | 7447 | | 1000<br>867<br>733<br>600 | | B: 1.1; PVR = 8002 0101 |
| | 7457 | RX = CBGA<br>VG = RoHS BGA | 1000<br>867<br>733<br>600 | | C: 1.2; PVR = 8002 0102 |

# 11 Document Revision History

Table 26 provides a revision history for this hardware specification.

**Table 26. Document Revision History**

| Revision Number | Date | Substantive Change(s) |
|---|---|---|
| 8 | 04/09/2013 | Updated template.<br>Updated Table 14 “L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs”.<br>Moved Revision History to the end of the document. |
| 7 | 3/28/2006 | Updated template.<br>Section 2, reworded L1 and L2 cache descriptions.<br>Removed note references for $\overline{CI}$ and $\overline{WT}$ in Table 12.<br>Added VG package signifier for 7457 only. |
| 6 | 7/22/2005 | Revised Note in Section 9.2. |
| | | Added heat sink vendor to list in Section 9.8. |
| | | Corrected bump and underfill model dimension in Section 9.8.3. |
| 5 | 9/9/2004 | Updated document to new Freescale template. |
| | | Updated section numbering and changed reference from part number specifications to addendums. |
| | | Added Rev. 1.2 devices, including increased L3 clock max frequency to 250 MHz and improved L3 AC timing. |
| | | Table 5: Added CTE information. |
| | | Table 8: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations. |
| | | Table 13: Deleted note 9 and renumbered. |
| | | Table 14: Deleted note 5 and renumbered. |
| | | Table 17: Revised note 6. |
| | | Added Section 9.1.3. |
| | | Section 9.2: Changed filter resistor recommendations. Recommend 10 Ω resistor for all production devices, including production Rev. 1.1 devices. 400 Ω resistor needed only for early Rev. 1.1 devices. |
| | | Table 22: Reversed the order of revision numbers. |
| | | Added Tables 25 and 26. |
| 4.1 | | Section 9.1.1: Corrected note regarding different PLL configurations for earlier devices; all MPC7457 devices to date conform to this table. |
| | | Section 9.6: Added information about unused L3_ADDR signals. |
| | | Table 24: Changed title to include document order information for MPC74x7RXnnnnNx series part number specification. |

**Table 26. Document Revision History (continued)**

| Revision Number | Date | Substantive Change(s) |
|---|---|---|
| 4 | | Table 9: Corrected pin lists for input and output AC timing to correctly show $\overline{\text{HIT}}$ as an output-only signal |
| | | Added specifications for 1267 MHz devices; removed specs for 1300 MHz devices. |
| | | Section 5.2.3: Changed recommendations regarding use of L3 clock jitter in AC timing analysis. The L3 jitter is now fully comprehended in the AC timing specs and does not need to be included in the timing analysis. |
| 3 | | Corrected numerous errors in lists of pins associated with $t_{KHOV}$, $t_{KHOX}$, $t_{IVKH}$, and $t_{IXKH}$ in Table 9. |
| | | Added support for 1.5 V L3 interface voltage; issues fixed in Rev. 1.1. |
| | | Corrected typos in Table 12. |
| | | Added data to Table 2. |
| | | Clarified address bus pull-up resistor recommendations in Section 1.9.6. |
| | | Modified Table 9, Figure 5, and Figure 6 to more accurately show when the mode select inputs ($\overline{\text{BMODE}}$[0:1], L3VSEL, BVSEL) are sampled and AC timing requirements |
| | | Table 10: Added skew and jitter values. |
| | | Table 14: Added AC timing values. |
| | | Table 24: Updated to reflect past and current part numbers not fully covered by this document. |
| | | Table 6: Removed $CV_{IH}$ and $CV_{IL}$; $V_{IH}$ and $V_{IL}$ for SYSCLK input is the same as for other input signals, and is now noted accordingly in this table. |
| | | Table 7: Removed Doze mode power entry (but left footnote 4 for clarity); documentation change only. |
| | | Nontechnical formatting |
| 2 | | Added substrate capacitor information in Sections 1.8.3 and 1.8.6. |
| | | Increased minimum processor and VCO frequencies in Table 8 from 500 and 1000 MHz to 600 and 1200 MHz (respectively). |
| | | Corrected maximum processor frequency for 1300 MHz devices in Table 8 (changed from 1333 to 1300 MHz). |
| | | Added value for to $t_{L3CSKW1}$ Table 10. |
| | | Added L3OHCR information in Section 1.5.2.4.1. |
| | | Added values for $t_{CO}$ and $t_{ECI}$ to Table 11. |
| | | Added Note 8 to Table 13 and Note 6 to Table 14. |
| | | Changed resistor value in PLL filter in Figure 25 from 10 Ω to 400 Ω. |
| | | Added 867 MHz speed grade. |
| | | Corrected Product Code in Tables 22 and 23. |
| | | Added pull-up/pull-down recommendations for $\overline{\text{CKSTP\_IN}}$ and PLL_CFG[0:4] to Section 1.9.6. |
| 1.1 | | Nontechnical reformatting. |