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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.267GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7457rx1267lc

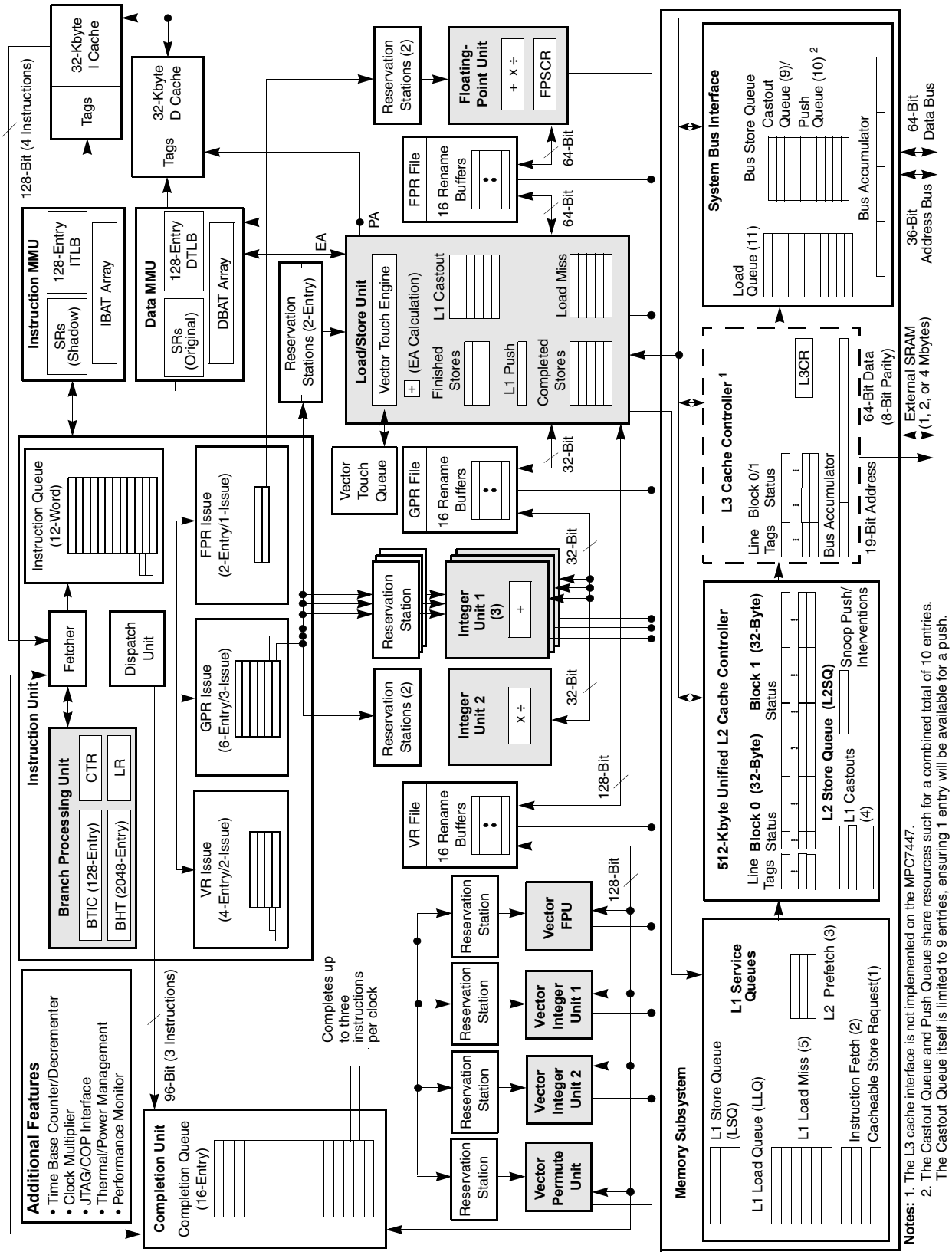


Figure 1. MPC7457 Block Diagram

  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.3-V processor core
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state.
  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and an MPC7457-specific thermal management exception.
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

3 Comparison with the MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441

Table 1 compares the key features of the MPC7457 with the key features of the earlier MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441. To achieve a higher frequency, the number of logic levels per cycle is reduced. Also, to achieve this higher frequency, the pipeline of the MPC7457 is extended (compared to the MPC7400), while maintaining the same level of performance as measured by the number of instructions executed per cycle (IPC).

Table 1. Microarchitecture Comparison

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Basic Pipeline Functions			
Logic inversions per cycle	18	18	18
Pipeline stages up to execute	5	5	5
Total pipeline stages (minimum)	7	7	7
Pipeline maximum instruction throughput	3 + Branch	3 + Branch	3 + Branch
Pipeline Resources			
Instruction buffer size	12	12	12
Completion buffer size	16	16	16
Renames (integer, float, vector)	16, 16, 16	16, 16, 16	16, 16, 16
Maximum Execution Throughput			
SFX	3	3	3
Vector	2 (any 2 of 4 units)	2 (any 2 of 4 units)	2 (any 2 of 4 units)
Scalar floating-point	1	1	1
Out-of-Order Window Size in Execution Queues			
SFX integer units	1 entry × 3 queues	1 entry × 3 queues	1 entry × 3 queues
Vector units	In order, 4 queues	In order, 4 queues	In order, 4 queues
Scalar floating-point unit	In order	In order	In order
Branch Processing Resources			
Prediction structures	BTIC, BHT, link stack	BTIC, BHT, link stack	BTIC, BHT, link stack
BTIC size, associativity	128-entry, 4-way	128-entry, 4-way	128-entry, 4-way
BHT size	2K-entry	2K-entry	2K-entry
Link stack depth	8	8	8
Unresolved branches supported	3	3	3
Branch taken penalty (BTIC hit)	1	1	1

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Cache level	L3	L3	L3
Total SRAM space supported	1 MB, 2MB, 4 MB [2]	1 MB, 2 MB	1 MB, 2 MB
On-chip tag logical size (cache space)	1 MB, 2 MB	1 MB, 2 MB	1 MB, 2 MB
Associativity	8-way	8-way	8-way
Number of 32-byte sectors/line	2, 4	2, 4	2, 4
Off-Chip data SRAM support	MSUG2 DDR, LW, PB2	MSUG2 DDR, LW, PB2	MSUG2 DDR, LW, PB2
Data path width	64	64	64
Direct mapped SRAM sizes	1 MB, 2 MB, 4 MB	1 MB, 2 MB	1 MB, 2 MB
Parity	Byte	Byte	Byte

Notes:

1. Not implemented on MPC7447, MPC7445, or MPC7441.
2. The MPC7457 supports up to 4 MB of SRAM, of which a maximum of 2 MB can be configured as cache memory; the remaining 2 MB may be unused or configured as private memory.

4 General Parameters

The following list provides a summary of the general parameters of the MPC7457:

Technology	0.13 µm CMOS, nine-layer metal
Die size	9.1 mm × 10.8 mm
Transistor count	58 million
Logic design	Fully-static
Packages	MPC7447: Surface mount 360 ceramic ball grid array (CBGA)
	MPC7457: Surface mount 483 ceramic ball grid array (CBGA)
Core power supply	1.3 V ±50 mV DC nominal
I/O power supply	1.8 V ±5% DC, or
	2.5 V ±5% DC, or
	1.5 V ±5% DC (L3 interface only, not implemented on MPC7447)

5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7457.

5.1 DC Electrical Characteristics

The tables in this section describe the MPC7457 DC electrical characteristics.Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings [1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.60	V	2
PLL supply voltage		AV_{DD}	–0.3 to 1.60	V	2
Processor bus supply voltage	BVSEL = 0	OV_{DD}	–0.3 to 1.95	V	3, 4
	BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	OV_{DD}	–0.3 to 2.7	V	3, 5
L3 bus supply voltage	L3VSEL = ¬$\overline{\text{HRESET}}$	GV_{DD}	–0.3 to 1.65	V	3, 6
	L3VSEL = 0	GV_{DD}	–0.3 to 1.95	V	3, 7
	L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	GV_{DD}	–0.3 to 2.7	V	3, 8
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3	V	9, 10
	L3 bus	V_{in}	–0.3 to GV_{DD} + 0.3	V	9, 10
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.3	V	
Storage temperature range		T_{stg}	–55 to 150	°C	

Notes:
1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{DD}/AV_{DD} must not exceed OV_{DD}/GV_{DD} by more than 1.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution**: OV_{DD}/GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8-V mode.
5. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5-V mode.
6. L3VSEL must be set to ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), such that the bus is in 1.5-V mode.
7. L3VSEL must be set to 0, such that the bus is in 1.8-V mode.
8. L3VSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5-V mode.
9. **Caution**: V_{in} must not exceed OV_{DD} or GV_{DD} by more than 0.3 V at any time including during power-on reset.
10. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Figure 2 shows the undershoot and overshoot voltage on the MPC7457.

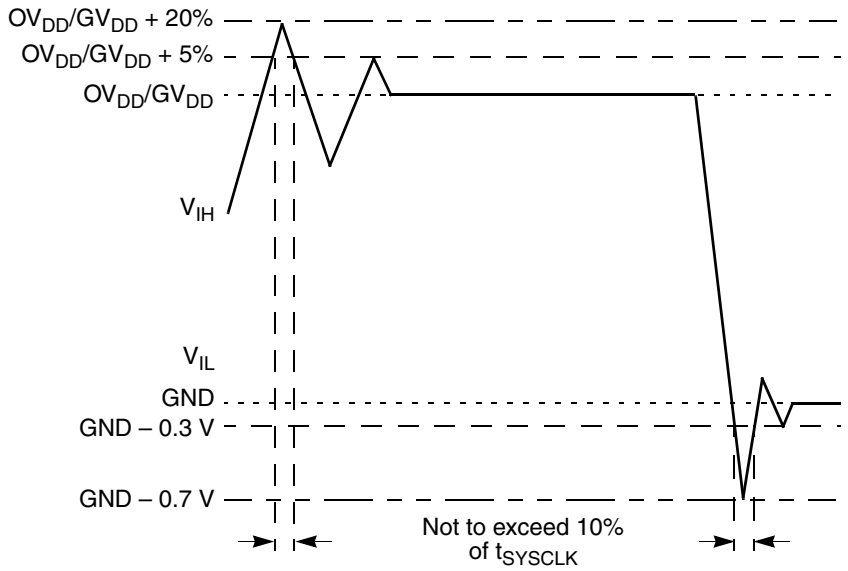


Figure 2. Overshoot/Undershoot Voltage

The MPC7457 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7457 core voltage must always be provided at nominal 1.3 V (see Table 4 for actual recommended core voltage). Voltage to the L3 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 3. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or GV_{DD} power pins.

Table 3. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L3VSEL Signal [1]	L3 Bus Input Threshold is Relative to:	Notes
0	1.8 V	0	1.8 V	2, 3
¬$\overline{\text{HRESET}}$	Not Available	¬$\overline{\text{HRESET}}$	1.5 V	2, 4
$\overline{\text{HRESET}}$	2.5 V	$\overline{\text{HRESET}}$	2.5 V	2
1	2.5 V	1	2.5 V	2

Notes:

1. Not implemented on MPC7447.
2. **Caution:** The input threshold selection must agree with the OV_{DD}/GV_{DD} voltages supplied. See notes in Table 2.
3. If used, pull-down resistors should be less than 250 Ω.
4. Applicable to L3 bus interface only. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

Table 9. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Revisions and Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{\text{TS}}$ is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue because any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ can be driven by multiple bus masters beginning the cycle of $\overline{\text{TS}}$. Timing is the same as $\overline{\text{ARTRY}}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{\text{BMODE}}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{\text{HRESET}}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 5 for sample timing.

Figure 4 provides the AC test load for the MPC7457.

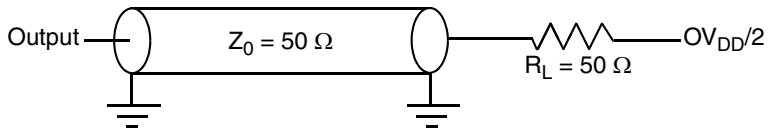


Figure 4. AC Test Load

Figure 5 provides the mode select input timing diagram for the MPC7457.

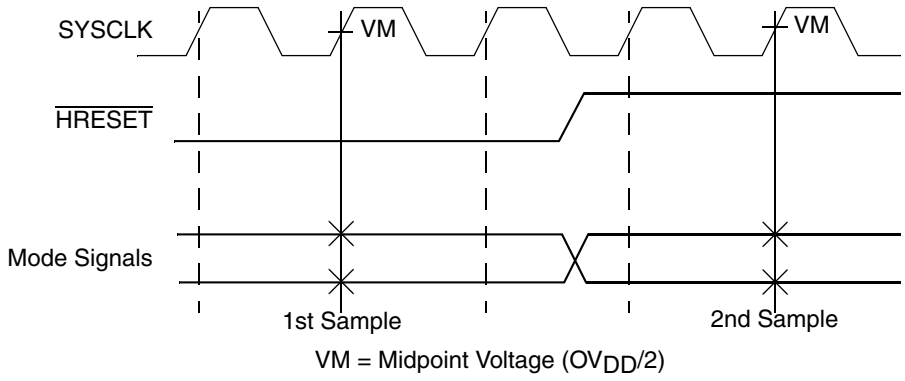


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7457.

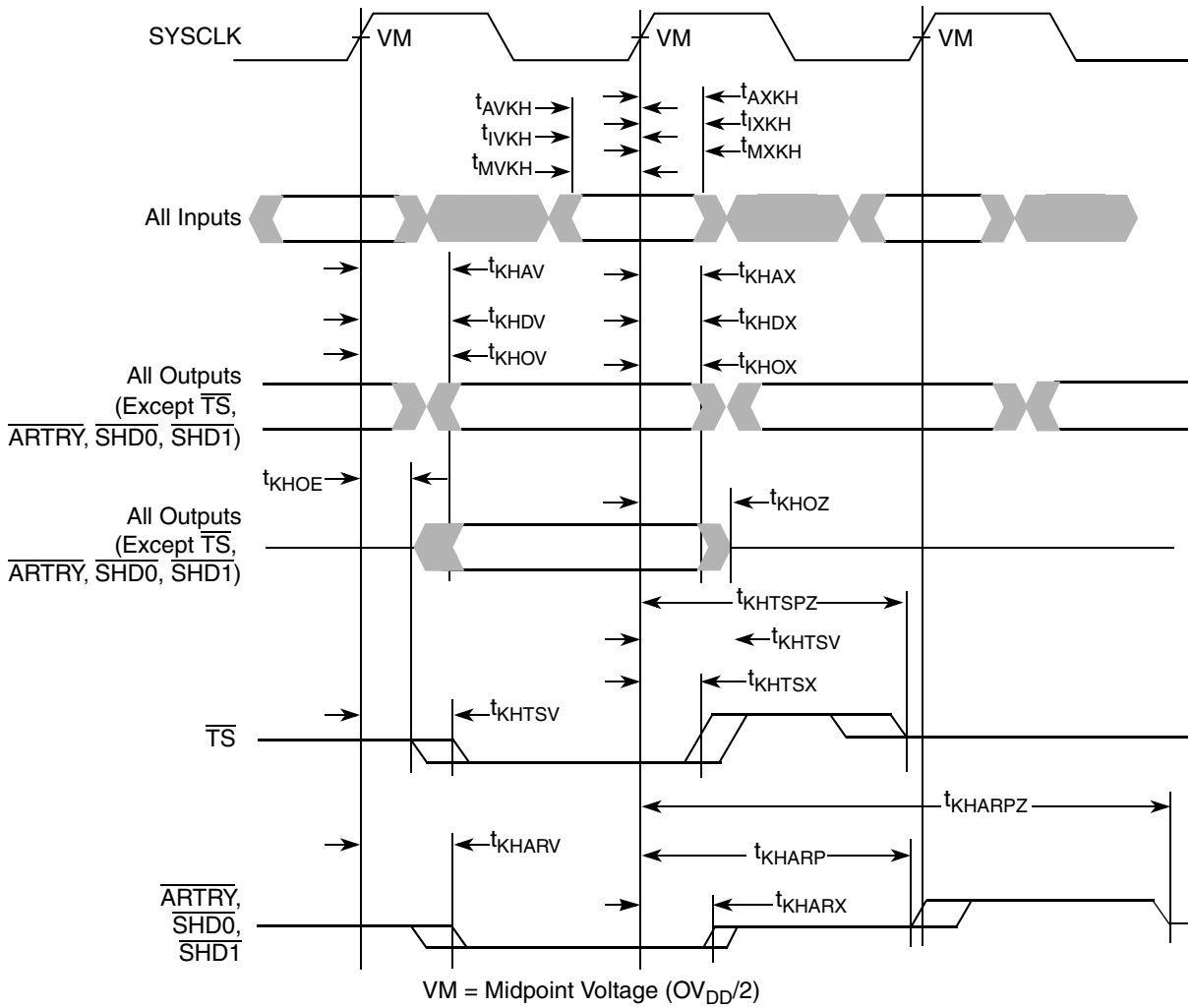


Figure 6. Input/Output Timing Diagram

Table 13. L3 Bus Interface AC Timing Specifications for MSUG2 (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [9]				Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)		Rev 1.2 (1.8-, 2.5-V I/O Modes)			
		Min	Max	Min	Max		
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	(t_{L3CLK}/4) + 0.65	—	(t_{L3CLK}/4) + 0.65	ns	

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLK*n* as shown in Figure 10. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the MPC7457 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLK*n* at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 8).
6. For DDR, the output data will typically lead the edge of L3_CLK*n* as shown in Figure 10. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock before the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
8. Assumes default value of L3OHCR. See Section 5.2.4.1, “Effects of L3OHCR Settings on L3 Bus AC Specifications,” for more information.
9. L3 I/O voltage mode must be configured by L3VSEL as described in Table 3, and voltage supplied at GV_{DD} must match mode selected as specified in Table 4. See Table 22 for revision level information and part marking.

Figure 12 shows the L3 bus timing diagrams for the MPC7457 interfaced to PB2 or Late Write SRAMs.

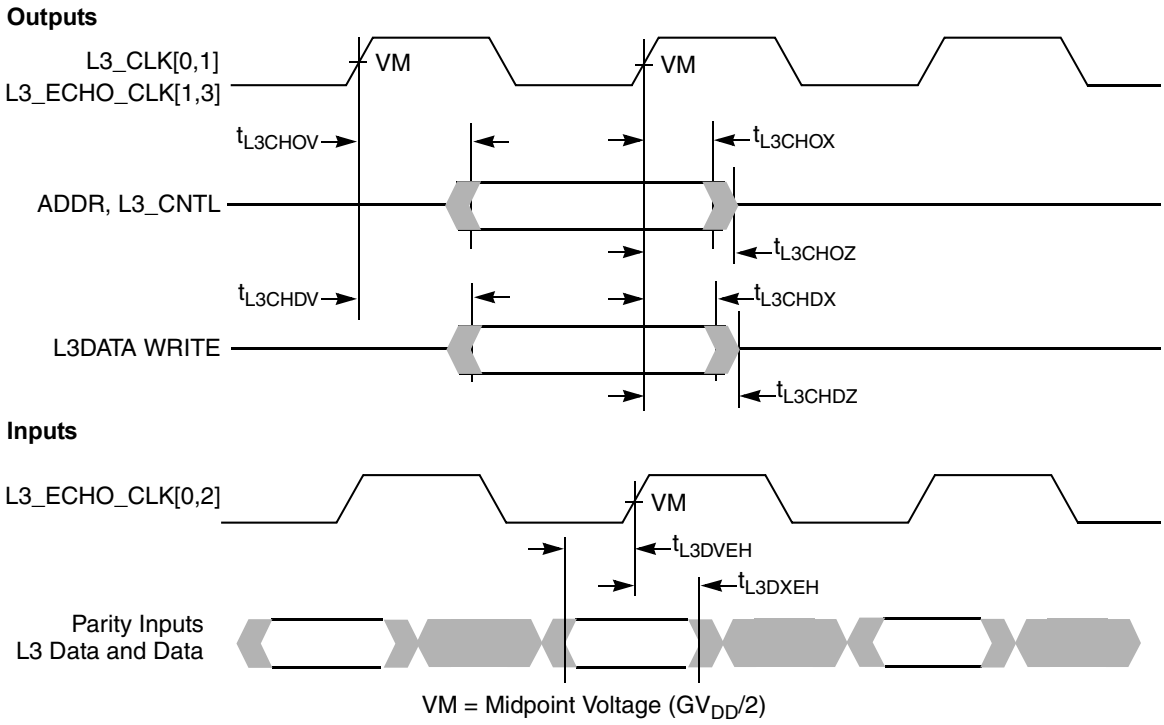


Figure 12. L3 Bus Timing Diagrams for Late Write or PB2 SRAMs

5.2.5 IEEE 1149.1 AC Timing Specifications

Table 15 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 14 through Figure 17.

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

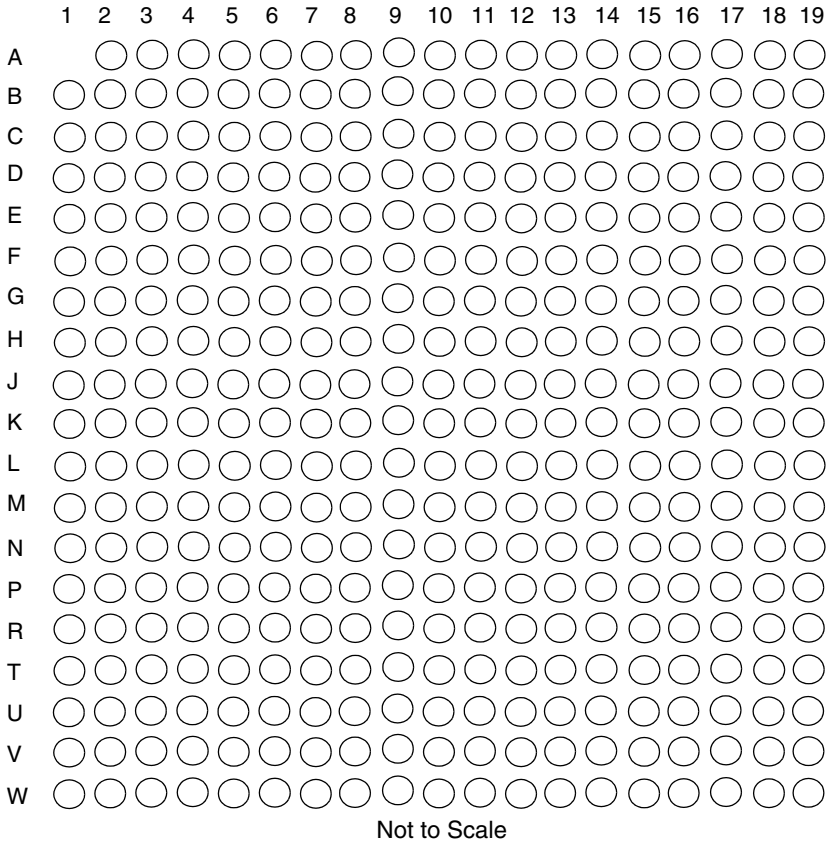
At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{JHJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3

6 Pin Assignments

Figure 18 (Part A) shows the pinout of the MPC7447, 360 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

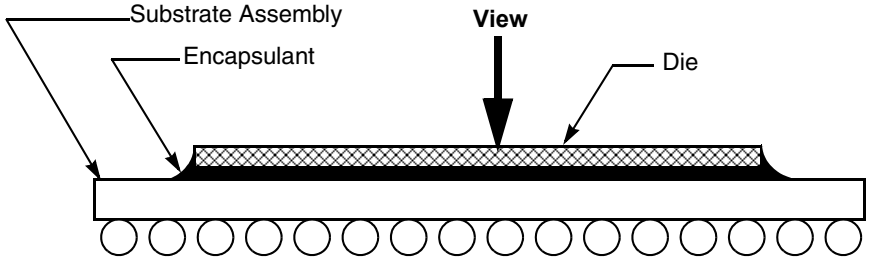


Figure 18. Pinout of the MPC7447, 360 CBGA Package as Viewed from the Top Surface

Table 16. Pinout Listing for the MPC7447, 360 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	—	—	N/A	
$\overline{\text{HIT}}$	B2	Low	Output	BVSEL	7
$\overline{\text{HRESET}}$	D8	Low	Input	BVSEL	
$\overline{\text{INT}}$	D4	Low	Input	BVSEL	
L1_TSTCLK	G8	High	Input	BVSEL	9
L2_TSTCLK	B3	High	Input	BVSEL	10
No Connect	A6, A13, A14, A15, A16, A17, A18, A19, B13, B14, B15, B16, B17, B18, B19, C13, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E12, E13, E14, E15, E16, E19, F12, F13, F14, F15, F16, F17, F18, F19, G11, G12, G13, G14, G15, G16, G19, H14, H15, H16, H17, H18, H19, J14, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L14, L15, L16, L17, L18, L19, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, P15, P16, P18, P19	—	—	—	11
$\overline{\text{LSSD\_MODE}}$	E8	Low	Input	BVSEL	6, 12
$\overline{\text{MCP}}$	C9	Low	Input	BVSEL	
OV_{DD}	B4, C2, C12, D5, E18, F2, G18, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14	—	—	N/A	
PLL_CFG[0:4]	B8, C8, C7, D7, A7	High	Input	BVSEL	
$\overline{\text{PMON\_IN}}$	D9	Low	Input	BVSEL	13
$\overline{\text{PMON\_OUT}}$	A9	Low	Output	BVSEL	
$\overline{\text{QACK}}$	G5	Low	Input	BVSEL	
$\overline{\text{QREQ}}$	P4	Low	Output	BVSEL	
$\overline{\text{SHD}}$[0:1]	E4, H5	Low	I/O	BVSEL	3
$\overline{\text{SMI}}$	F9	Low	Input	BVSEL	
$\overline{\text{SRESET}}$	A2	Low	Input	BVSEL	
SYSCLK	A10	—	Input	BVSEL	
$\overline{\text{TA}}$	K6	Low	Input	BVSEL	
TBEN	E1	High	Input	BVSEL	
$\overline{\text{TBST}}$	F11	Low	Output	BVSEL	
TCK	C6	High	Input	BVSEL	
TDI	B9	High	Input	BVSEL	6
TDO	A4	High	Output	BVSEL	

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
L1_TSTCLK	H4	High	Input	BVSEL	10
L2_TSTCLK	J2	High	Input	BVSEL	12
L3VSEL	A4	High	Input	N/A	6, 7
L3ADDR[18:0]	H11, F20, J16, E22, H18, G20, F22, G22, H20, K16, J18, H22, J20, J22, K18, K20, L16, K22, L18	High	Output	L3VSEL	
L3_CLK[0:1]	V22, C17	High	Output	L3VSEL	
$\overline{\text{L3\_CNTL}}$[0:1]	L20, L22	Low	Output	L3VSEL	
L3DATA[0:63]	AA19, AB20, U16, W18, AA20, AB21, AA21, T16, W20, U18, Y22, R16, V20, W22, T18, U20, N18, N20, N16, N22, M16, M18, M20, M22, R18, T20, U22, T22, R20, P18, R22, M15, G18, D22, E20, H16, C22, F18, D20, B22, G16, A21, G15, E17, A20, C19, C18, A19, A18, G14, E15, C16, A17, A16, C15, G13, C14, A14, E13, C13, G12, A13, E12, C12	High	I/O	L3VSEL	
L3DP[0:7]	AB19, AA22, P22, P16, C20, E16, A15, A12	High	I/O	L3VSEL	
L3_ECHO_CLK[0,2]	V18, E18	High	Input	L3VSEL	
L3_ECHO_CLK[1,3]	P20, E14	HIgh	I/O	L3VSEL	
$\overline{\text{LSSD\_MODE}}$	F6	Low	Input	BVSEL	7, 13
$\overline{\text{MCP}}$	B8	Low	Input	BVSEL	
No Connect	A8, A11, B6, B11, C11, D11, D3, D5, E11, E7, F2, F11, G2, H9	—	—	N/A	14
OV_{DD}	B3, C5, C7, C10, D2, E3, E9, F5, G3, G9, H7, J5, K3, L7, M5, N3, P7, R4, T3, U5, U7, U11, U15, V3, V9, V13, Y2, Y5, Y7, Y10, Y17, Y19, AA4, AA15	—	—	N/A	
PLL_CFG[0:4]	A2, F7, C2, D4, H8	High	Input	BVSEL	
$\overline{\text{PMON\_IN}}$	E6	Low	Input	BVSEL	15
$\overline{\text{PMON\_OUT}}$	B4	Low	Output	BVSEL	
$\overline{\text{QACK}}$	K7	Low	Input	BVSEL	
$\overline{\text{QREQ}}$	Y1	Low	Output	BVSEL	
$\overline{\text{SHD}}$[0:1]	L4, L8	Low	I/O	BVSEL	3
$\overline{\text{SMI}}$	G8	Low	Input	BVSEL	
$\overline{\text{SRESET}}$	G1	Low	Input	BVSEL	
SYSCLK	D6	—	Input	BVSEL	
$\overline{\text{TA}}$	N8	Low	Input	BVSEL	
TBEN	L3	High	Input	BVSEL	
$\overline{\text{TBST}}$	B7	Low	Output	BVSEL	
TCK	J7	High	Input	BVSEL	

8.4 Package Parameters for the MPC7457, 483 CBGA or RoHS BGA

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483 ceramic ball grid array (CBGA).

Package outline	29 × 29 mm
Interconnects	483 (22 × 22 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	—
Maximum module height	3.22 mm
Ball diameter	0.89 mm (35 mil)

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Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
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The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5°C/W. For

Table 22. Part Numbering Nomenclature

MC	74*x*7	*xx*	*nnnn*	L	*x*

Product Code	Part Identifier	Package	Processor Frequency [1]	Application Modifier	Revision Level
PPC [2] MC	7457 7447	RX = CBGA	867 1000 1200 1267	L: 1.3 V ± 50 mV 0° to 105°C	B: 1.1; PVR = 8002 0101
MC	7457	RX = CBGA VG = RoHS BGA	867 1000 1200 1267		C: 1.2; PVR = 8002 0102

Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by a hardware specification addendum may support other maximum core frequencies.
2. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

10.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed are described in a separate addendum, which supplement and supersede this hardware specification. As such parts are released, these specifications will be listed in this section.

Table 23. Part Numbers Addressed by MPC74x7RX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS01AD)

MC	74*x*7	*xx*	*nnnn*	N	*x*

Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
PPC	7457	RX = CBGA	1000 867 733 600	N: 1.1 V ± 50 mV 0° to 105°C	B: 1.1; PVR = 8002 0101
	7447		1000 867		
MC	7447		1000 867 733 600		B: 1.1; PVR = 8002 0101
	7457	RX = CBGA VG = RoHS BGA	1000 867 733 600		C: 1.2; PVR = 8002 0102

11 Document Revision History

Table 26 provides a revision history for this hardware specification.

Table 26. Document Revision History

Revision Number	Date	Substantive Change(s)
8	04/09/2013	Updated template. Updated Table 14 “L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs”. Moved Revision History to the end of the document.
7	3/28/2006	Updated template. Section 2, reworded L1 and L2 cache descriptions. Removed note references for $\overline{CI}$ and $\overline{WT}$ in Table 12. Added VG package signifier for 7457 only.
6	7/22/2005	Revised Note in Section 9.2.
		Added heat sink vendor to list in Section 9.8.
		Corrected bump and underfill model dimension in Section 9.8.3.
5	9/9/2004	Updated document to new Freescale template.
		Updated section numbering and changed reference from part number specifications to addendums.
		Added Rev. 1.2 devices, including increased L3 clock max frequency to 250 MHz and improved L3 AC timing.
		Table 5: Added CTE information.
		Table 8: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Table 13: Deleted note 9 and renumbered.
		Table 14: Deleted note 5 and renumbered.
		Table 17: Revised note 6.
		Added Section 9.1.3.
		Section 9.2: Changed filter resistor recommendations. Recommend 10 Ω resistor for all production devices, including production Rev. 1.1 devices. 400 Ω resistor needed only for early Rev. 1.1 devices.
		Table 22: Reversed the order of revision numbers.
		Added Tables 25 and 26.
4.1		Section 9.1.1: Corrected note regarding different PLL configurations for earlier devices; all MPC7457 devices to date conform to this table.
		Section 9.6: Added information about unused L3_ADDR signals.
		Table 24: Changed title to include document order information for MPC74x7RXnnnnNx series part number specification.

Table 26. Document Revision History (continued)

Revision Number	Date	Substantive Change(s)
4		Table 9: Corrected pin lists for input and output AC timing to correctly show $\overline{\text{HIT}}$ as an output-only signal
		Added specifications for 1267 MHz devices; removed specs for 1300 MHz devices.
		Section 5.2.3: Changed recommendations regarding use of L3 clock jitter in AC timing analysis. The L3 jitter is now fully comprehended in the AC timing specs and does not need to be included in the timing analysis.
3		Corrected numerous errors in lists of pins associated with t_{KHOV}, t_{KHOX}, t_{IVKH}, and t_{IXKH} in Table 9.
		Added support for 1.5 V L3 interface voltage; issues fixed in Rev. 1.1.
		Corrected typos in Table 12.
		Added data to Table 2.
		Clarified address bus pull-up resistor recommendations in Section 1.9.6.
		Modified Table 9, Figure 5, and Figure 6 to more accurately show when the mode select inputs ($\overline{\text{BMODE}}$[0:1], L3VSEL, BVSEL) are sampled and AC timing requirements
		Table 10: Added skew and jitter values.
		Table 14: Added AC timing values.
		Table 24: Updated to reflect past and current part numbers not fully covered by this document.
		Table 6: Removed CV_{IH} and CV_{IL}; V_{IH} and V_{IL} for SYSCLK input is the same as for other input signals, and is now noted accordingly in this table.
		Table 7: Removed Doze mode power entry (but left footnote 4 for clarity); documentation change only.
		Nontechnical formatting
2		Added substrate capacitor information in Sections 1.8.3 and 1.8.6.
		Increased minimum processor and VCO frequencies in Table 8 from 500 and 1000 MHz to 600 and 1200 MHz (respectively).
		Corrected maximum processor frequency for 1300 MHz devices in Table 8 (changed from 1333 to 1300 MHz).
		Added value for to $t_{L3CSKW1}$ Table 10.
		Added L3OHCR information in Section 1.5.2.4.1.
		Added values for t_{CO} and t_{ECI} to Table 11.
		Added Note 8 to Table 13 and Note 6 to Table 14.
		Changed resistor value in PLL filter in Figure 25 from 10 Ω to 400 Ω.
		Added 867 MHz speed grade.
		Corrected Product Code in Tables 22 and 23.
		Added pull-up/pull-down recommendations for $\overline{\text{CKSTP\_IN}}$ and PLL_CFG[0:4] to Section 1.9.6.
1.1		Nontechnical reformatting.

Table 26. Document Revision History (continued)

Revision Number	Date	Substantive Change(s)
1		Removed support for 1.5 V L3 interface voltage from Tables 3 and 4. 1.5 V I/O voltage is not supported in current MPC7457 devices.
		Added package thermal characteristics values to Table 5, made minor revisions to Section 1.9.8.
		Added preliminary AC timing values to Tables 10 and 12.
		Added footnotes to Table 17.
0		Initial release.

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