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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7457vg1000nc

- Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
- Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Minimum misprediction penalty	6	6	6
Execution Unit Timings (Latency-Throughput)			
Aligned load (integer, float, vector)	3-1, 4-1, 3-1	3-1, 4-1, 3-1	3-1, 4-1, 3-1
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2	4-2, 5-2, 4-2	4-2, 5-2, 4-2
L1 miss, L2 hit latency	9 data/13 instruction	9 data/13 instruction	9 data/13 instruction
SFX (aDd Sub, Shift, Rot, Cmp, logicals)	1-1	1-1	1-1
Integer multiply (32 × 8, 32 × 16, 32 × 32)	3-1, 3-1, 4-2	3-1, 3-1, 4-2	3-1, 3-1, 4-2
Scalar float	5-1	5-1	5-1
VSFX (vector simple)	1-1	1-1	1-1
VCFX (vector complex)	4-1	4-1	4-1
VFPU (vector float)	4-1	4-1	4-1
VPER (vector permute)	2-1	2-1	2-1
MMUs			
TLBs (instruction and data)	128-entry, 2-way	128-entry, 2-way	128-entry, 2-way
Tablewalk mechanism	Hardware + software	Hardware + software	Hardware + software
Instruction BATs/data BATs	8/8	8/8	4/4
L1 I Cache/D Cache Features			
Size	32K/32K	32K/32K	32K/32K
Associativity	8-way	8-way	8-way
Locking granularity	Way	Way	Way
Parity on I cache	Word	Word	Word
Parity on D cache	Byte	Byte	Byte
Number of D cache misses (load/store)	5/1	5/1	5/1
Data stream touch engines	4 streams	4 streams	4 streams
On-Chip Cache Features			
Cache level	L2	L2	L2
Size/associativity	512-Kbyte/8-way	256-Kbyte/8-way	256-Kbyte/8-way
Access width	256 bits	256 bits	256 bits
Number of 32-byte sectors/line	2	2	2
Parity	Byte	Byte	Byte
Off-Chip Cache Support [1]			

Table 4 provides the recommended operating conditions for the MPC7457.

Table 4. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value		Unit	Notes
			Min	Max		
Core supply voltage		V_{DD}	1.3 V ± 50 mV		V	
PLL supply voltage		AV_{DD}	1.3 V ± 50 mV		V	2
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 5%		V	
	BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	OV_{DD}	2.5 V ± 5%		V	
L3 bus supply voltage	L3VSEL = 0	GV_{DD}	1.8 V ± 5%		V	
	L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	GV_{DD}	2.5 V ± 5%		V	
	L3VSEL = ¬$\overline{\text{HRESET}}$	GV_{DD}	1.5 V ± 5%		V	3
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	V	
	L3 bus	V_{in}	GND	GV_{DD}	V	
	JTAG signals	V_{in}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. This voltage is the input to the filter discussed in Section 9.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

Table 5 provides the package thermal characteristics for the MPC7457.

Table 5. Package Thermal Characteristics [1]

Characteristic	Symbol	Value		Unit	Notes
		MPC7447	MPC7457		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	22	20	°C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	14	14	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	16	15	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	11	11	°C/W	2, 4
Junction-to-board thermal resistance	$R_{\theta JB}$	6	6	°C/W	5
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	°C/W	6

Table 5. Package Thermal Characteristics [1] (continued)

Characteristic	Symbol	Value		Unit	Notes
		MPC7447	MPC7457		
Coefficient of thermal expansion		6.8	6.8	ppm/°C	

Notes:
1. Refer to Section 9.8, "Thermal Management Information," for more details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7457.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs including SYSCLK)	1.5	V_{IH}	$GV_{DD} \times 0.65$	$GV_{DD} + 0.3$	V	2
	1.8		$OV_{DD}/GV_{DD} \times 0.65$	$OV_{DD}/GV_{DD} + 0.3$	V	
	2.5		1.7	$OV_{DD}/GV_{DD} + 0.3$	V	
Input low voltage (all inputs including SYSCLK)	1.5	V_{IL}	–0.3	$GV_{DD} \times 0.35$	V	2, 6
	1.8		–0.3	$OV_{DD}/GV_{DD} \times 0.35$	V	
	2.5		–0.3	0.7	V	
Input leakage current, $V_{in} = GV_{DD}/OV_{DD}$	—	I_{in}	—	30	µA	2, 3
High-impedance (off-state) leakage current, $V_{in} = GV_{DD}/OV_{DD}$	—	I_{TSI}	—	30	µA	2, 3, 4
Output high voltage, $I_{OH} = –5$ mA	1.5	V_{OH}	$OV_{DD}/GV_{DD} – 0.45$	—	V	6
	1.8		$OV_{DD}/GV_{DD} – 0.45$	—	V	
	2.5		1.8	—	V	
Output low voltage, $I_{OL} = 5$ mA	1.5	V_{OL}	—	0.45	V	6
	1.8		—	0.45	V	
	2.5		—	0.6	V	

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		867 MHz		1000 MHz		1200 MHz		1267 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Internal PLL relock time		—	100	—	100	—	100	—	100	µs	7

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, “PLL Configuration,” for valid PLL_CFG[0:4] settings.
2. Assumes lightly-loaded, single-processor system; see Section 5.2.1, “Clock AC Specifications” for more information.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver’s closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

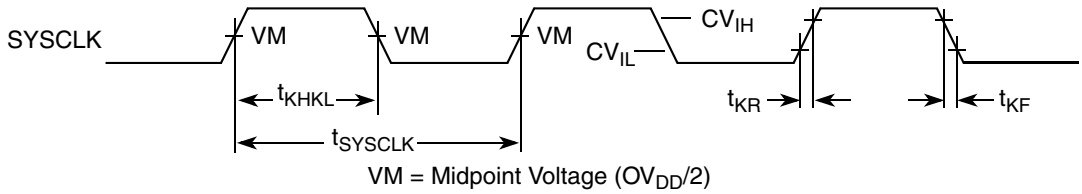

Figure 3. SYSCLK Input Timing Diagram

5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 as defined in Figure 4 and Figure 5. Timing specifications for the L3 bus are provided in Section 5.2.3, “L3 Clock AC Specifications.”

Table 9. Processor Bus AC Timing Specifications [1]

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Revisions and Speed Grades		Unit	Notes
		Min	Max		
Input setup times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:3], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1], BMODE[0:1], BMODE[0:1], BVSEL, L3VSEL	 t_{AVKH} t_{DVKH} t_{IVKH} t_{MVKH}	 1.8 1.8 1.8 1.8	 — — — —	ns 8
Input hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, TT[0:3], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, HD[0:1] BMODE[0:1], BVSEL, L3VSEL	 t_{AXKH} t_{DXKH} t_{IXKH} t_{MXKH}	 0 0 0 0	 — — — —	ns 8
Output valid times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BR, CI, CKSTP_IN, DRDY, DTI[0:3], GBL, HIT, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:3], TS, SHD[0:1], WT	 t_{KHAV} t_{KHDV} t_{KHOV}	 — — —	 2.0 2.0 2.0	ns	
Output hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BR, CI, CKSTP_IN, DRDY, DTI[0:3], GBL, HIT, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:3], TS, SHD[0:1], WT	 t_{KHAX} t_{KHDX} t_{KHOX}	 0.5 0.5 0.5	 — — —	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	
SYSCLK to output high impedance (all except TS, ARTRY, SHD0, SHD1)	t_{KHOZ}	—	3.5	ns	
SYSCLK to TS high impedance after precharge	t_{KHTSPZ}	—	1	t_{SYSCLK}	3, 4, 5
Maximum delay to ARTRY/SHD0/SHD1 precharge	t_{KHARP}	—	1	t_{SYSCLK}	3, 5 6, 7

Table 9. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Revisions and Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{\text{TS}}$ is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue because any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ can be driven by multiple bus masters beginning the cycle of $\overline{\text{TS}}$. Timing is the same as $\overline{\text{ARTRY}}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{\text{BMODE}}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{\text{HRESET}}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 5 for sample timing.

Figure 4 provides the AC test load for the MPC7457.

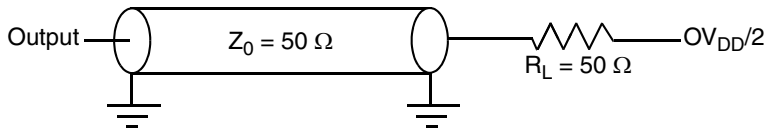

Figure 4. AC Test Load

Figure 12 shows the L3 bus timing diagrams for the MPC7457 interfaced to PB2 or Late Write SRAMs.

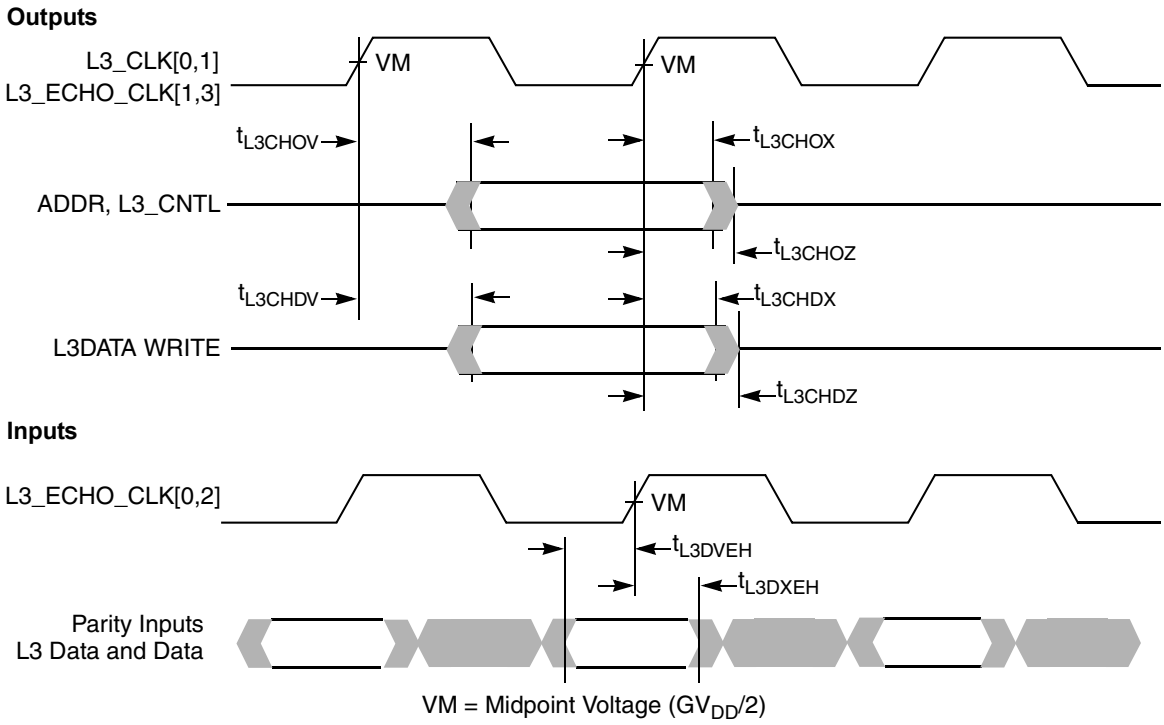

Figure 12. L3 Bus Timing Diagrams for Late Write or PB2 SRAMs

5.2.5 IEEE 1149.1 AC Timing Specifications

Table 15 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 14 through Figure 17.

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{JHJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 13). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 13 provides the AC test load for TDO and the boundary-scan outputs of the MPC7457.

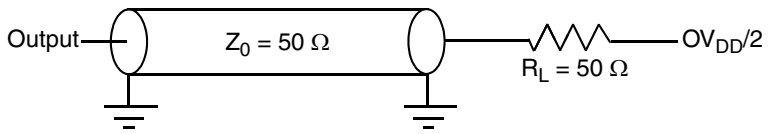

Figure 13. Alternate AC Test Load for the JTAG Interface

Figure 14 provides the JTAG clock input timing diagram.

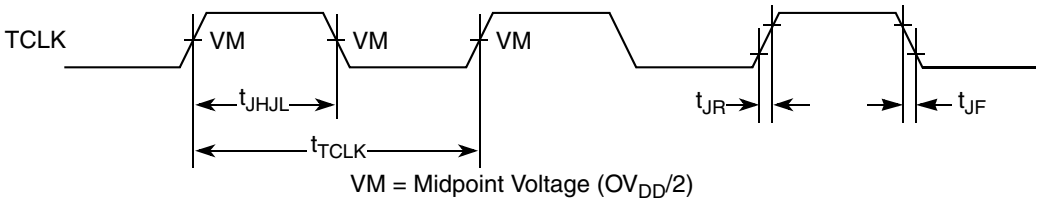

Figure 14. JTAG Clock Input Timing Diagram

Figure 15 provides the $\overline{\text{TRST}}$ timing diagram.

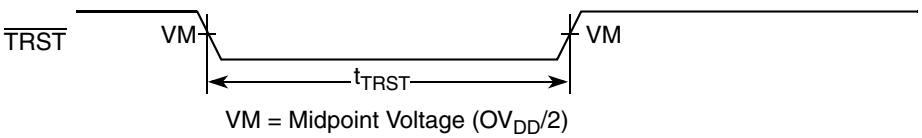

Figure 15. $\overline{\text{TRST}}$ Timing Diagram

Figure 16 provides the boundary-scan timing diagram.

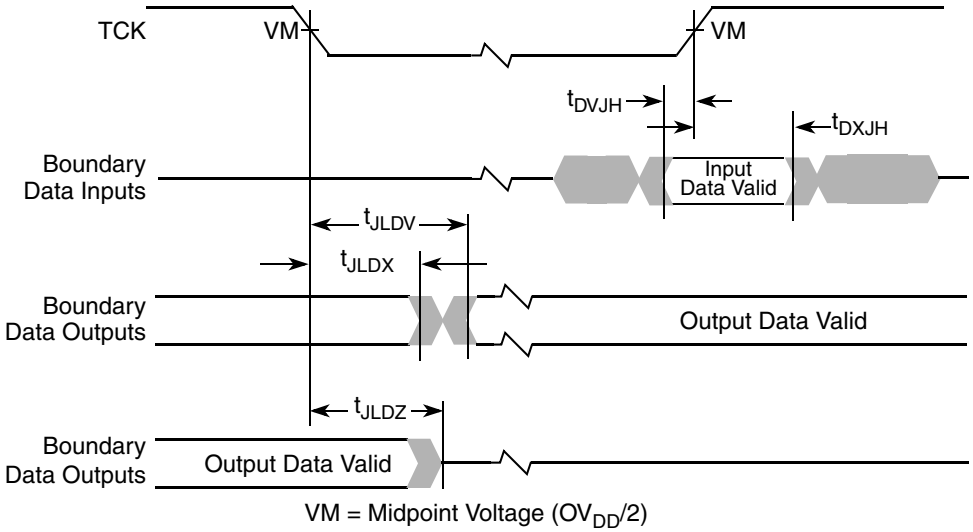

Figure 16. Boundary-Scan Timing Diagram

Figure 17 provides the test access port timing diagram.

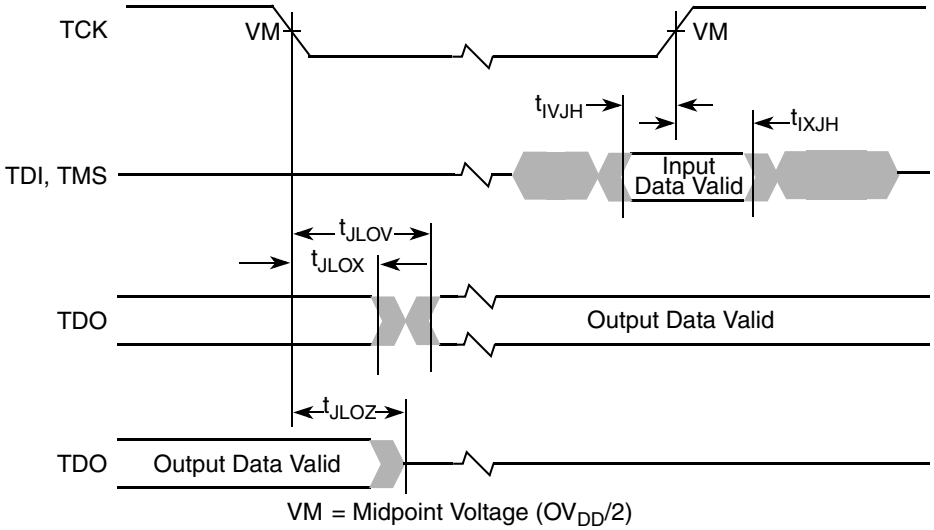

Figure 17. Test Access Port Timing Diagram

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
AV_{DD}	B2	—	Input	N/A	
$\overline{BG}$	R3	Low	Input	BVSEL	
$\overline{BMODE0}$	C6	Low	Input	BVSEL	4
$\overline{BMODE1}$	C4	Low	Input	BVSEL	5
$\overline{BR}$	K1	Low	Output	BVSEL	
BVSEL	G6	High	Input	N/A	6, 7
$\overline{CI}$	R1	Low	Output	BVSEL	
$\overline{CKSTP\_IN}$	F3	Low	Input	BVSEL	
$\overline{CKSTP\_OUT}$	K6	Low	Output	BVSEL	
CLK_OUT	N1	High	Output	BVSEL	
D[0:63]	AB15, T14, R14, AB13, V14, U14, AB14, W16, AA11, Y11, U12, W13, Y14, U13, T12, W12, AB12, R12, AA13, AB11, Y12, V11, T11, R11, W10, T10, W11, V10, R10, U10, AA10, U9, V7, T8, AB4, Y6, AB7, AA6, Y8, AA7, W8, AB10, AA16, AB16, AB17, Y18, AB18, Y16, AA18, W14, R13, W15, AA14, V16, W6, AA12, V6, AB9, AB6, R7, R9, AA9, AB8, W9	High	I/O	BVSEL	
$\overline{DBG}$	V1	Low	Input	BVSEL	
DP[0:7]	AA2, AB3, AB2, AA8, R8, W5, U8, AB5	High	I/O	BVSEL	
$\overline{DRDY}$	T6	Low	Output	BVSEL	8
DTI[0:3])	P2, T5, U3, P6	High	Input	BVSEL	9
EXT_QUAL	B9	High	Input	BVSEL	10
$\overline{GBL}$	M4	Low	I/O	BVSEL	
GND	A22, B1, B5, B12, B14, B16, B18, B20, C3, C9, C21, D7, D13, D15, D17, D19, E2, E5, E21, F10, F12, F14, F16, F19, G4, G7, G17, G21, H13, H15, H19, H5, J3, J10, J12, J14, J17, J21, K5, K9, K11, K13, K15, K19, L10, L12, L14, L17, L21, M3, M6, M9, M11, M13, M19, N10, N12, N14, N17, N21, P3, P9, P11, P13, P15, P19, R17, R21, T13, T15, T19, T4, T7, T9, U17, U21, V2, V5, V8, V12, V15, V19, W7, W17, W21, Y3, Y9, Y13, Y15, Y20, AA5, AA17, AB1, AB22	—	—	N/A	
GV_{DD}	B13, B15, B17, B19, B21, D12, D14, D16, D18, D21, E19, F13, F15, F17, F21, G19, H12, H14, H17, H21, J19, K17, K21, L19, M17, M21, N19, P17, P21, R15, R19, T17, T21, U19, V17, V21, W19, Y21	—	—	N/A	11
$\overline{HIT}$	K2	Low	Output	BVSEL	8
$\overline{HRESET}$	A3	Low	Input	BVSEL	
$\overline{INT}$	J6	Low	Input	BVSEL	

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
L1_TSTCLK	H4	High	Input	BVSEL	10
L2_TSTCLK	J2	High	Input	BVSEL	12
L3VSEL	A4	High	Input	N/A	6, 7
L3ADDR[18:0]	H11, F20, J16, E22, H18, G20, F22, G22, H20, K16, J18, H22, J20, J22, K18, K20, L16, K22, L18	High	Output	L3VSEL	
L3_CLK[0:1]	V22, C17	High	Output	L3VSEL	
$\overline{\text{L3\_CNTL}}$[0:1]	L20, L22	Low	Output	L3VSEL	
L3DATA[0:63]	AA19, AB20, U16, W18, AA20, AB21, AA21, T16, W20, U18, Y22, R16, V20, W22, T18, U20, N18, N20, N16, N22, M16, M18, M20, M22, R18, T20, U22, T22, R20, P18, R22, M15, G18, D22, E20, H16, C22, F18, D20, B22, G16, A21, G15, E17, A20, C19, C18, A19, A18, G14, E15, C16, A17, A16, C15, G13, C14, A14, E13, C13, G12, A13, E12, C12	High	I/O	L3VSEL	
L3DP[0:7]	AB19, AA22, P22, P16, C20, E16, A15, A12	High	I/O	L3VSEL	
L3_ECHO_CLK[0,2]	V18, E18	High	Input	L3VSEL	
L3_ECHO_CLK[1,3]	P20, E14	HIgh	I/O	L3VSEL	
$\overline{\text{LSSD\_MODE}}$	F6	Low	Input	BVSEL	7, 13
$\overline{\text{MCP}}$	B8	Low	Input	BVSEL	
No Connect	A8, A11, B6, B11, C11, D11, D3, D5, E11, E7, F2, F11, G2, H9	—	—	N/A	14
OV_{DD}	B3, C5, C7, C10, D2, E3, E9, F5, G3, G9, H7, J5, K3, L7, M5, N3, P7, R4, T3, U5, U7, U11, U15, V3, V9, V13, Y2, Y5, Y7, Y10, Y17, Y19, AA4, AA15	—	—	N/A	
PLL_CFG[0:4]	A2, F7, C2, D4, H8	High	Input	BVSEL	
$\overline{\text{PMON\_IN}}$	E6	Low	Input	BVSEL	15
$\overline{\text{PMON\_OUT}}$	B4	Low	Output	BVSEL	
$\overline{\text{QACK}}$	K7	Low	Input	BVSEL	
$\overline{\text{QREQ}}$	Y1	Low	Output	BVSEL	
$\overline{\text{SHD}}$[0:1]	L4, L8	Low	I/O	BVSEL	3
$\overline{\text{SMI}}$	G8	Low	Input	BVSEL	
$\overline{\text{SRESET}}$	G1	Low	Input	BVSEL	
SYSCLK	D6	—	Input	BVSEL	
$\overline{\text{TA}}$	N8	Low	Input	BVSEL	
TBEN	L3	High	Input	BVSEL	
$\overline{\text{TBST}}$	B7	Low	Output	BVSEL	
TCK	J7	High	Input	BVSEL	

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
TDI	E4	High	Input	BVSEL	7
TDO	H1	High	Output	BVSEL	
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL	
TEST[0:5]	B10, H6, H10, D8, F9, F8	—	Input	BVSEL	13
TEST[6]	A9	—	Input	BVSEL	10
TMS	K4	High	Input	BVSEL	7
$\overline{\text{TRST}}$	C1	Low	Input	BVSEL	7, 16
$\overline{\text{TS}}$	P5	Low	I/O	BVSEL	3
TSIZ[0:2]	L1,H3,D1	High	Output	BVSEL	
TT[0:4]	F1, F4, K8, A5, E1	High	I/O	BVSEL	
$\overline{\text{WT}}$	L2	Low	Output	BVSEL	
V_{DD}	J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14	—	—	N/A	
VDD_SENSE[0:1]	G11, J8	—	—	N/A	17

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); GV_{DD} supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals $\overline{\text{L3\_CNTL}}$[0:1]; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). For actual recommended value of V_{in} or supply voltages, see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. See Table 3 for bus voltage configuration information. If used, pull-down resistors should be less than 250 Ω.
7. Internal pull up on die.
8. Ignored in 60x bus mode.
9. These signals must be pulled down to GND if unused or if the MPC7457 is in 60x bus mode.
10. These input signals for factory use only and must be pulled down to GND for normal machine operation.
11. Power must be supplied to GV_{DD}, even when the L3 interface is disabled or unused.
12. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
14. These signals are for factory use only and must be left unconnected for normal machine operation.
15. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
16. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
17. These pins are internally connected to V_{DD}. They are intended to allow an external device to detect the core voltage level present at the processor core. If unused, they must be connected directly to V_{DD} or left unconnected.

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the CBGA package.

8.1 Package Parameters for the MPC7447, 360 CBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.24 mm
Ball diameter	0.89 mm (35 mil)

8.4 Package Parameters for the MPC7457, 483 CBGA or RoHS BGA

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483 ceramic ball grid array (CBGA).

Package outline	29 × 29 mm
Interconnects	483 (22 × 22 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	—
Maximum module height	3.22 mm
Ball diameter	0.89 mm (35 mil)

Table 21. Impedance Characteristics
V_{DD} = 1.5 V, OV_{DD} = 1.8 V ± 5%, T_j = 5°–85°C

Impedance		Processor Bus	L3 Bus	Unit
Z_0	Typical	33–42	34–42	Ω
	Maximum	31–51	32–44	Ω

9.6 Pull-Up/Pull-Down Resistor Requirements

The MPC7457 requires high-resistive (weak: 4.7-kΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being for factory test must be pulled up to OV_{DD} or down to GND to ensure proper device operation. For the MPC7447, 360 BGA, the pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. For the MPC7457, 483 BGA, the pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:5]; the pins that must be pulled down are: L1_TSTCLK and TEST[6]. The $\overline{\text{CKSTP\_IN}}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 kΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7457 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 kΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

If pull-down resistors are used to configure BVSEL or L3VSEL, the resistors should be less than 250 Ω (see Table 16). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7457 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7457 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information about this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7457 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If extended addressing is not used, A[0:3] are unused and must be pulled low to GND through weak pull-down resistors. If the MPC7457 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L3 interface does not normally require pull-up resistors. Unused L3_ADDR signals are driven low when the SRAM is configured to be less than 1 M in size via L3CR. For example, L3_ADD[18] will be driven low if the SRAM size is configured to be 2 M; likewise, L3_ADDR[18:17] will be driven low if the SRAM size is configured to be 1 M.

9.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 26 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

9.8.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 29 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 27). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure and is recommended due to the high power dissipation of the MPC7457. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

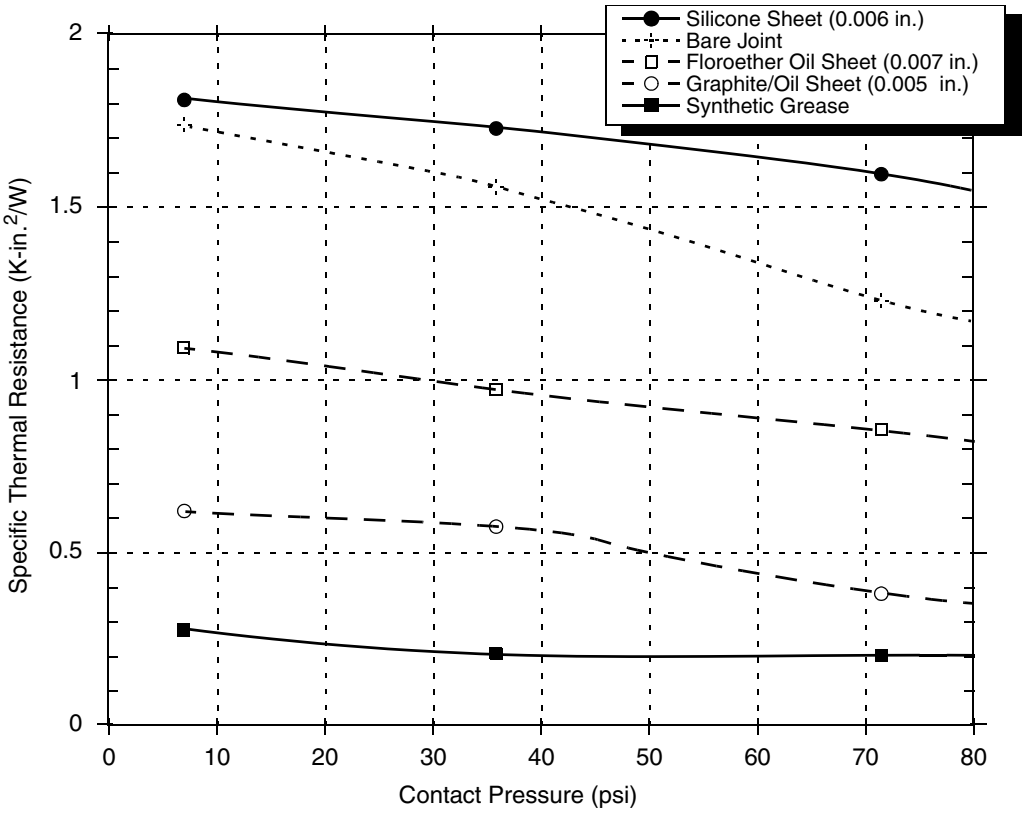

Figure 29. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

Conductivity	Value	Unit
Bump and Underfill		
k_x	0.6	W/(m • K)
k_y	0.6	
k_z	2	
Substrate		
k	18	
Solder Ball and Air		
k_x	0.034	
k_y	0.034	
k_z	3.8	

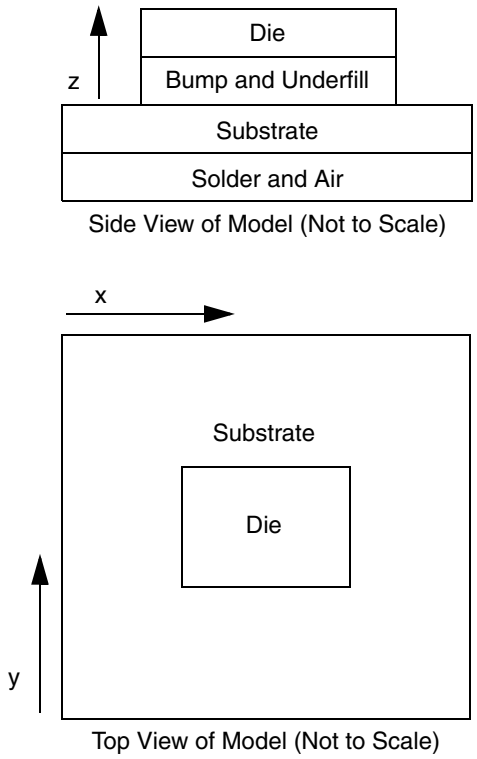

Figure 30. Recommended Thermal Model of MPC7447 and MPC7457

10 Part Numbering and Marking

Ordering information for the parts fully covered by this specification document is provided in Section 10.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision level code which refers to the die mask revision number. Section 10.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a referred to as a hardware specification addendum.

10.1 Part Numbers Fully Addressed by This Document

Table 22 provides the Freescale part numbering nomenclature for the MPC7457.

11 Document Revision History

Table 26 provides a revision history for this hardware specification.

Table 26. Document Revision History

Revision Number	Date	Substantive Change(s)
8	04/09/2013	Updated template. Updated Table 14 “L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs”. Moved Revision History to the end of the document.
7	3/28/2006	Updated template. Section 2, reworded L1 and L2 cache descriptions. Removed note references for $\overline{CI}$ and $\overline{WT}$ in Table 12. Added VG package signifier for 7457 only.
6	7/22/2005	Revised Note in Section 9.2.
		Added heat sink vendor to list in Section 9.8.
		Corrected bump and underfill model dimension in Section 9.8.3.
5	9/9/2004	Updated document to new Freescale template.
		Updated section numbering and changed reference from part number specifications to addendums.
		Added Rev. 1.2 devices, including increased L3 clock max frequency to 250 MHz and improved L3 AC timing.
		Table 5: Added CTE information.
		Table 8: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Table 13: Deleted note 9 and renumbered.
		Table 14: Deleted note 5 and renumbered.
		Table 17: Revised note 6.
		Added Section 9.1.3.
		Section 9.2: Changed filter resistor recommendations. Recommend 10 Ω resistor for all production devices, including production Rev. 1.1 devices. 400 Ω resistor needed only for early Rev. 1.1 devices.
		Table 22: Reversed the order of revision numbers.
		Added Tables 25 and 26.
4.1		Section 9.1.1: Corrected note regarding different PLL configurations for earlier devices; all MPC7457 devices to date conform to this table.
		Section 9.6: Added information about unused L3_ADDR signals.
		Table 24: Changed title to include document order information for MPC74x7RXnnnnNx series part number specification.