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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.267GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc7457vg1267lc

1 Overview

The MPC7457 is the fourth implementation of the fourth generation (G4) microprocessors from Freescale. The MPC7457 implements the full PowerPC 32-bit architecture and is targeted at networking and computing systems applications. The MPC7457 consists of a processor core, a 512-Kbyte L2, and an internal L3 tag and controller that support a glueless backside L3 cache through a dedicated high-bandwidth interface. The MPC7447 is identical to the MPC7457 except that it does not support the L3 cache interface.

Figure 1 shows a block diagram of the MPC7457. The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit.

The memory storage subsystem supports the MPX bus protocol and a subset of the 60x bus protocol to main memory and other system resources. The L3 interface supports 1, 2, or 4 Mbytes of external SRAM for L3 cache and/or private memory data. For systems implementing 4 Mbytes of SRAM, a maximum of 2 Mbytes may be used as cache; the remaining 2 Mbytes must be private memory.

Note that the MPC7457 is a footprint-compatible, drop-in replacement in a MPC7455 application if the core power supply is 1.3 V.

2 Features

This section summarizes features of the MPC7457 implementation of the PowerPC architecture.

Major features of the MPC7457 are as follows:

- High-performance, superscalar microprocessor
  - As many as four instructions can be fetched from the instruction cache at a time.
  - As many as three instructions can be dispatched to the issue queues at a time.
  - As many as 12 instructions can be in the instruction queue (IQ).
  - As many as 16 instructions can be at some stage of execution simultaneously.
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history (BHT) with 2 bits per entry for 4 levels of prediction—not-taken, strongly not-taken, taken, and strongly taken
    - Up to three outstanding speculative branches

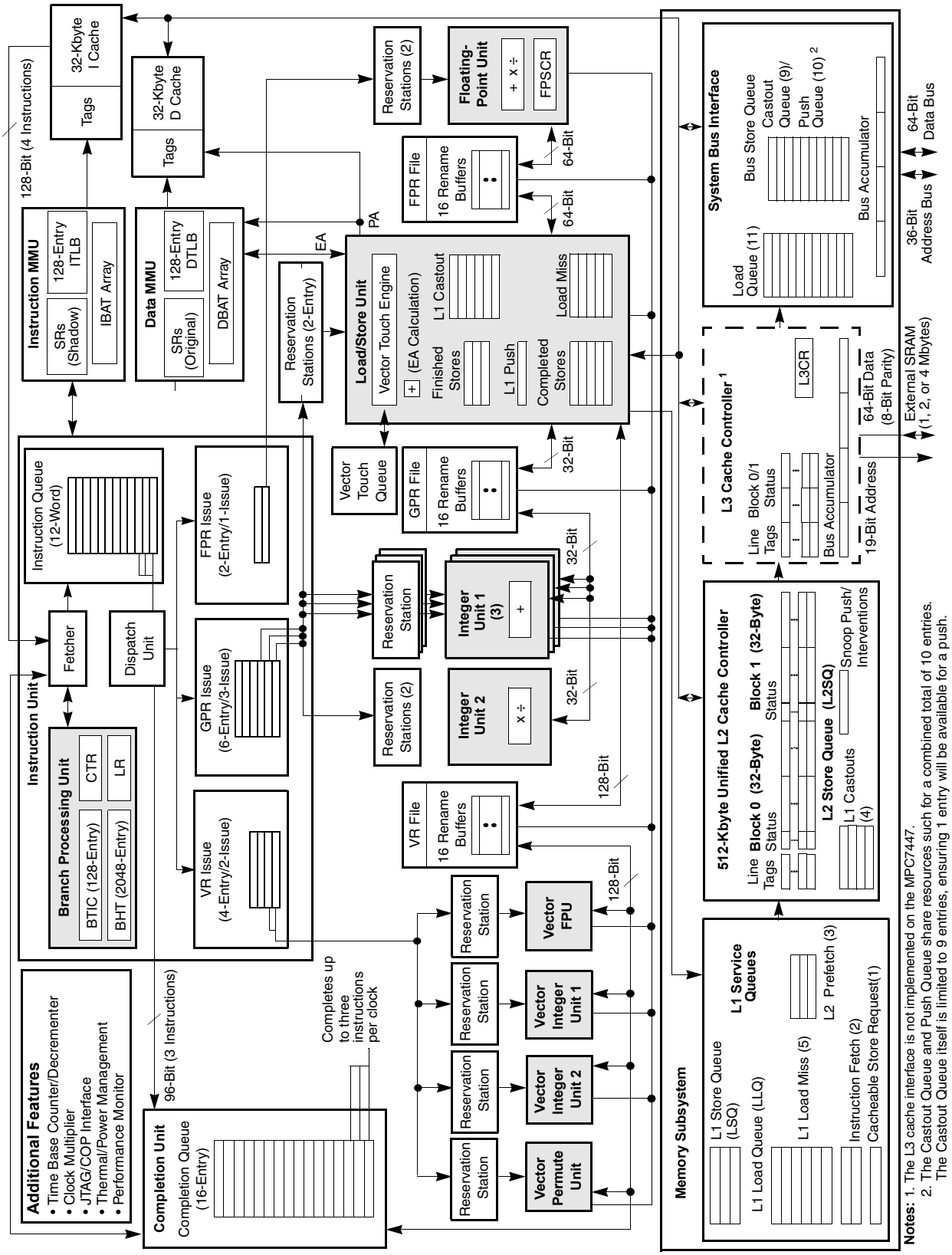


Figure 1. MPC7457 Block Diagram

- Four integer units (IUs) that share 32 GPRs for integer operands
  - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions
  - IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions
- Five-stage FPU and a 32-entry FPR file
  - Fully IEEE 754-1985 compliant FPU for both single- and double-precision operations
  - Supports non-IEEE mode for time-critical operations
  - Hardware support for denormalized numbers
  - Thirty-two 64-bit FPRs for single- or double-precision operands
- Four vector units and 32-entry vector register file (VRs)
  - Vector permute unit (VPU)
  - Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**)
  - Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**)
  - Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half-word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - Dedicated adder calculates effective addresses (EAs)
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues FIQ, VIQ, and GIQ can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can be dispatched only from the three lowest IQ entries—IQ0, IQ1, and IQ2
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle

  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.3-V processor core
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state.
  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and an MPC7457-specific thermal management exception.
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

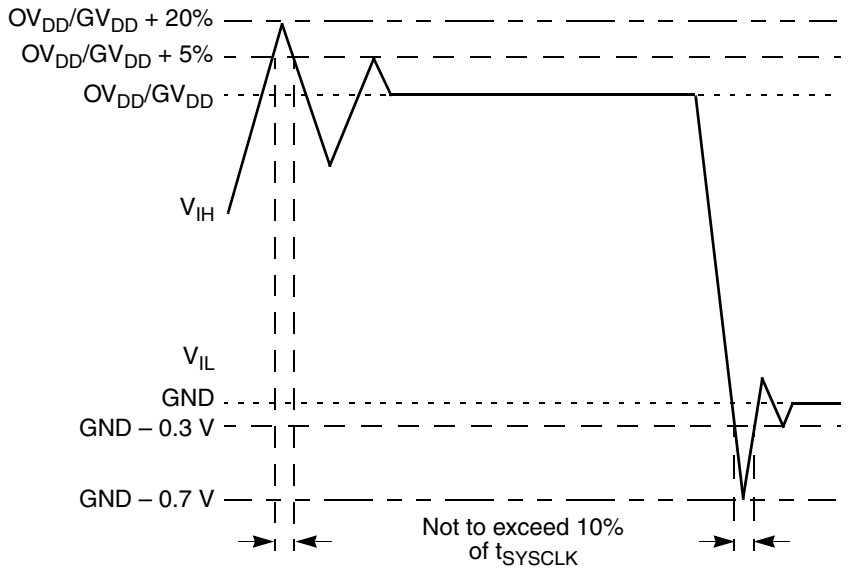


Figure 2. Overshoot/Undershoot Voltage

The MPC7457 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7457 core voltage must always be provided at nominal 1.3 V (see Table 4 for actual recommended core voltage). Voltage to the L3 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 3. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or GV_{DD} power pins.

Table 3. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L3VSEL Signal [1]	L3 Bus Input Threshold is Relative to:	Notes
0	1.8 V	0	1.8 V	2, 3
¬$\overline{\text{HRESET}}$	Not Available	¬$\overline{\text{HRESET}}$	1.5 V	2, 4
$\overline{\text{HRESET}}$	2.5 V	$\overline{\text{HRESET}}$	2.5 V	2
1	2.5 V	1	2.5 V	2

Notes:

1. Not implemented on MPC7447.
2. **Caution:** The input threshold selection must agree with the OV_{DD}/GV_{DD} voltages supplied. See notes in Table 2.
3. If used, pull-down resistors should be less than 250 Ω.
4. Applicable to L3 bus interface only. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

Table 9. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Revisions and Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{\text{TS}}$ is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue because any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ can be driven by multiple bus masters beginning the cycle of $\overline{\text{TS}}$. Timing is the same as $\overline{\text{ARTRY}}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{\text{BMODE}}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{\text{HRESET}}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 5 for sample timing.

Figure 4 provides the AC test load for the MPC7457.

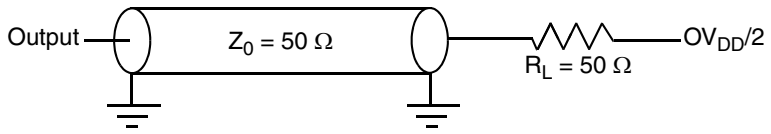


Figure 4. AC Test Load

Figure 5 provides the mode select input timing diagram for the MPC7457.

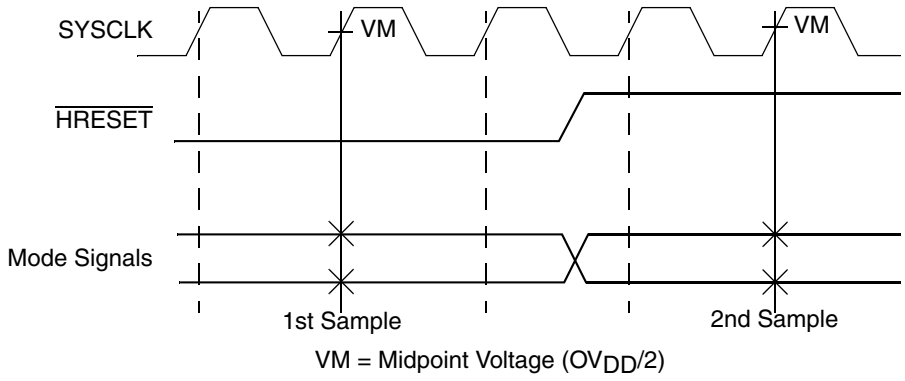


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7457.

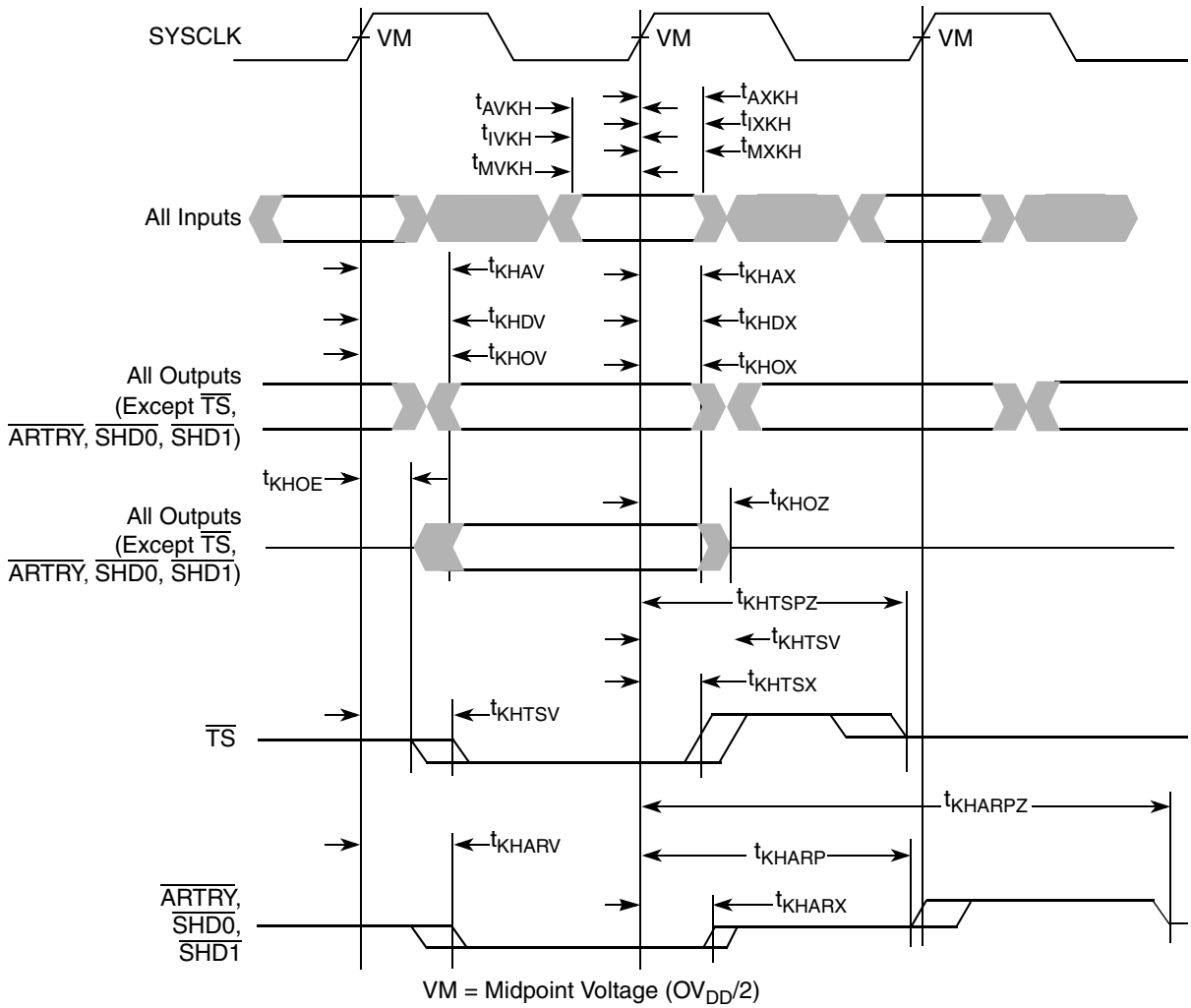


Figure 6. Input/Output Timing Diagram

Table 11. Sample Points Calculation Parameters

Parameter	Symbol	Max	Unit	Notes
Delay from processor clock to internal_L3_CLK	t_{AC}	3/4	t_{L3_CLK}	1
Delay from internal_L3_CLK to L3_CLK[*n*] output pins	t_{CO}	3	ns	2
Delay from L3_ECHO_CLK[*n*] to receive latch	t_{ECI}	3	ns	3

Notes:

1. This specification describes a logical offset between the internal clock edge used to launch the L3 address and control signals (this clock edge is phase-aligned with the processor clock edge) and the internal clock edge used to launch the L3_CLK[*n*] signals. With proper board routing, this offset ensures that the L3_CLK[*n*] edge will arrive at the SRAM within a valid address window and provide adequate setup and hold time. This offset is reflected in the L3 bus interface AC timing specifications, but must also be separately accounted for in the calculation of sample points and, thus, is specified here.
2. This specification is the delay from a rising or falling edge on the internal_L3_CLK signal to the corresponding rising or falling edge at the L3CLK[*n*] pins.
3. This specification is the delay from a rising or falling edge of L3_ECHO_CLK[*n*] to data valid and ready to be sampled from the FIFO.

5.2.4.1 Effects of L3OHCR Settings on L3 Bus AC Specifications

The AC timing of the L3 interface can be adjusted using the L3 Output Hold Control Register (L3OCHR). Each field controls the timing for a group of signals. The AC timing specifications presented herein represent the AC timing when the register contains the default value of 0x0000_0000. Incrementing a field delays the associated signals, increasing the output valid time and hold time of the affected signals. In the special case of delaying an L3_CLK signal, the net effect is to decrease the output valid and output hold times of all signals being latched relative to that clock signal. The amount of delay added is summarized in Table 12. Note that these settings affect output timing parameters only and do not impact input timing parameters of the L3 bus in any way.

Table 12. Effect of L3OHCR Settings on L3 Bus AC Timing

At recommended operating conditions. See Table 4.

Field Name[1]	Affected Signals	Value	Output Valid Time		Output Hold Time		Unit	Notes
			Parameter Symbol [2]	Change [3]	Parameter Symbol [2]	Change [3]		
L3AOH	L3_ADDR[18:0], L3_CNTL[0:1]	0b00	t_{L3CHOV}	0	t_{L3CHOX}	0	ps	4
		0b01		+50		+50		
		0b10		+100		+100		
		0b11		+150		+150		

Table 13. L3 Bus Interface AC Timing Specifications for MSUG2 (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [9]				Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)		Rev 1.2 (1.8-, 2.5-V I/O Modes)			
		Min	Max	Min	Max		
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	(t_{L3CLK}/4) + 0.65	—	(t_{L3CLK}/4) + 0.65	ns	

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLK*n* as shown in Figure 10. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the MPC7457 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLK*n* at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 8).
6. For DDR, the output data will typically lead the edge of L3_CLK*n* as shown in Figure 10. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock before the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
8. Assumes default value of L3OHCR. See Section 5.2.4.1, “Effects of L3OHCR Settings on L3 Bus AC Specifications,” for more information.
9. L3 I/O voltage mode must be configured by L3VSEL as described in Table 3, and voltage supplied at GV_{DD} must match mode selected as specified in Table 4. See Table 22 for revision level information and part marking.

Table 14. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs

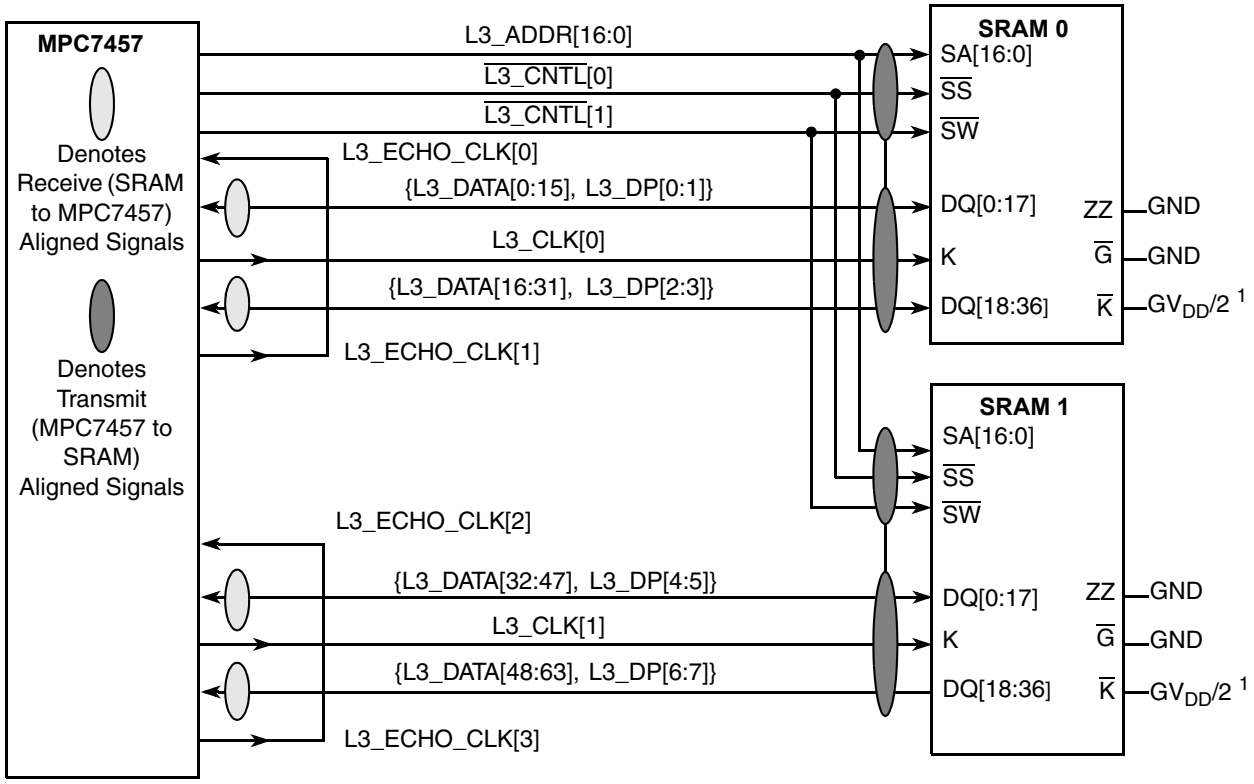
At recommended operating conditions. See Table 4.

Parameter	Symbol	All Revisions and L3 I/O Voltage Modes		Unit	Notes
		Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	0.75	ns	1, 2
Setup times: Data and parity	t_{L3DVEH}	0.1	—	ns	2, 3
Input hold times: Data and parity	t_{L3DXEH}	0.7	—	ns	2, 3
Valid times: Data and parity	t_{L3CHDV}	—	2.5	ns	2, 4, 5
Valid times: All other outputs	t_{L3CHOV}	—	1.8	ns	5
Output hold times: Data and parity	t_{L3CHDX}	1.4	—	ns	2, 4, 5
Output hold times: All other outputs	t_{L3CHOX}	1.0	—	ns	2, 5
L3_CLK to high impedance: Data and parity	t_{L3CHDZ}	—	3.0	ns	2
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	3.0	ns	2

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. Timing behavior and characterization are currently being evaluated.
3. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
4. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLK*n* to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
5. Assumes default value of L3OHCR. See Section 5.2.4.1, “Effects of L3OHCR Settings on L3 Bus AC Specifications,” for more information.

Figure 11 shows the typical connection diagram for the MPC7457 interfaced to PB2 SRAMs or Late Write SRAMs.



Note:
1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 11. Typical Synchronous 1-MByte L3 Cache Late Write or PB2 Interface

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 13). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 13 provides the AC test load for TDO and the boundary-scan outputs of the MPC7457.

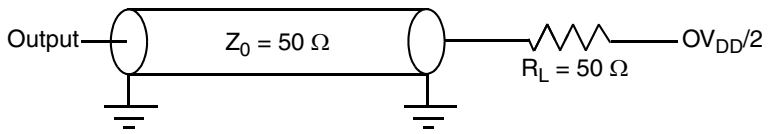


Figure 13. Alternate AC Test Load for the JTAG Interface

Figure 14 provides the JTAG clock input timing diagram.

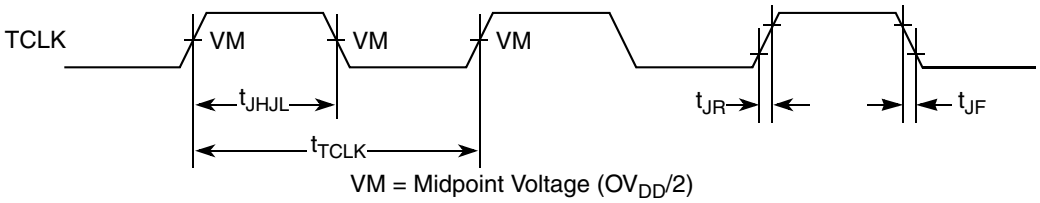


Figure 14. JTAG Clock Input Timing Diagram

Figure 15 provides the $\overline{\text{TRST}}$ timing diagram.

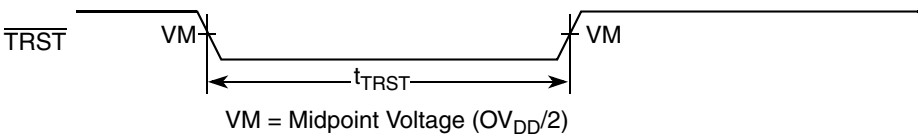


Figure 15. $\overline{\text{TRST}}$ Timing Diagram

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
TDI	E4	High	Input	BVSEL	7
TDO	H1	High	Output	BVSEL	
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL	
TEST[0:5]	B10, H6, H10, D8, F9, F8	—	Input	BVSEL	13
TEST[6]	A9	—	Input	BVSEL	10
TMS	K4	High	Input	BVSEL	7
$\overline{\text{TRST}}$	C1	Low	Input	BVSEL	7, 16
$\overline{\text{TS}}$	P5	Low	I/O	BVSEL	3
TSIZ[0:2]	L1,H3,D1	High	Output	BVSEL	
TT[0:4]	F1, F4, K8, A5, E1	High	I/O	BVSEL	
$\overline{\text{WT}}$	L2	Low	Output	BVSEL	
V_{DD}	J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14	—	—	N/A	
VDD_SENSE[0:1]	G11, J8	—	—	N/A	17

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); GV_{DD} supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals $\overline{\text{L3\_CNTL}}$[0:1]; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). For actual recommended value of V_{in} or supply voltages, see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. See Table 3 for bus voltage configuration information. If used, pull-down resistors should be less than 250 Ω.
7. Internal pull up on die.
8. Ignored in 60x bus mode.
9. These signals must be pulled down to GND if unused or if the MPC7457 is in 60x bus mode.
10. These input signals for factory use only and must be pulled down to GND for normal machine operation.
11. Power must be supplied to GV_{DD}, even when the L3 interface is disabled or unused.
12. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
14. These signals are for factory use only and must be left unconnected for normal machine operation.
15. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
16. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
17. These pins are internally connected to V_{DD}. They are intended to allow an external device to detect the core voltage level present at the processor core. If unused, they must be connected directly to V_{DD} or left unconnected.

8.4 Package Parameters for the MPC7457, 483 CBGA or RoHS BGA

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483 ceramic ball grid array (CBGA).

Package outline	29 × 29 mm
Interconnects	483 (22 × 22 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	—
Maximum module height	3.22 mm
Ball diameter	0.89 mm (35 mil)

The $\overline{\text{QACK}}$ signal shown in Figure 26 is usually connected to the PCI bridge chip in a system and is an input to the MPC7457 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7457 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

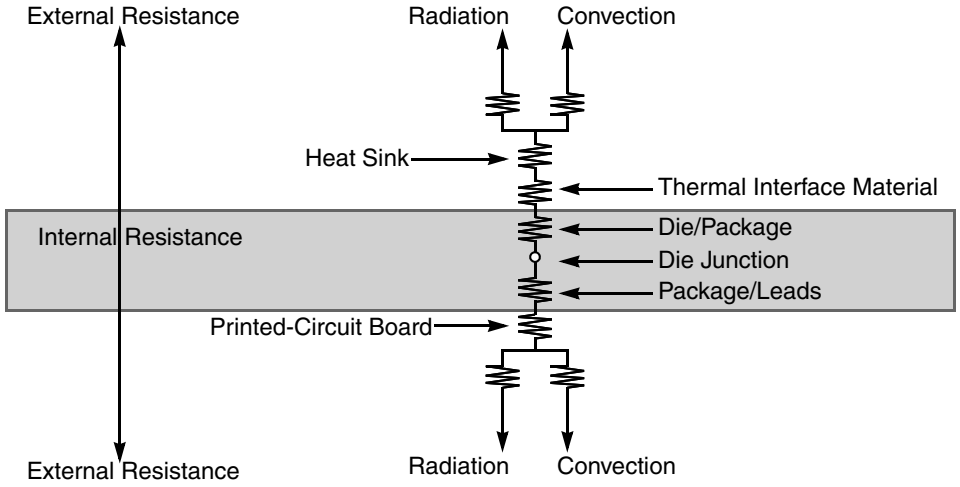
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

9.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (actually top-of-die since silicon die is exposed) thermal resistance
- The die junction-to-ball thermal resistance

Figure 28 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance.)

Figure 28. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

Conductivity	Value	Unit
Bump and Underfill		
k_x	0.6	W/(m • K)
k_y	0.6	
k_z	2	
Substrate		
k	18	
Solder Ball and Air		
k_x	0.034	
k_y	0.034	
k_z	3.8	

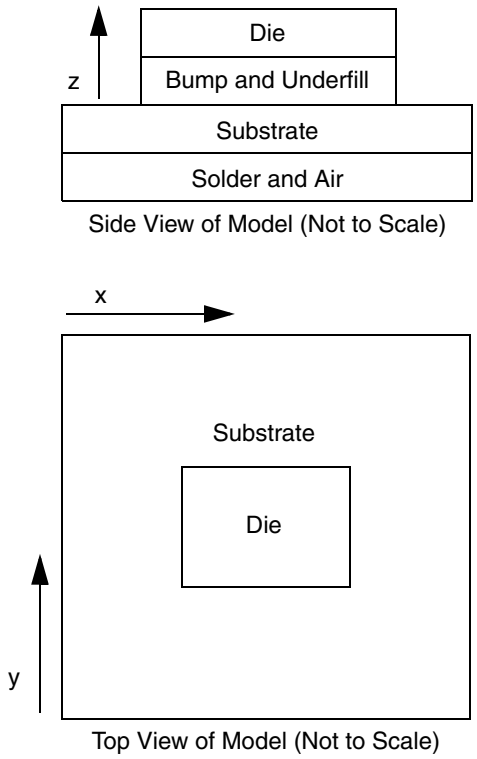


Figure 30. Recommended Thermal Model of MPC7447 and MPC7457

10 Part Numbering and Marking

Ordering information for the parts fully covered by this specification document is provided in Section 10.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision level code which refers to the die mask revision number. Section 10.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a referred to as a hardware specification addendum.

10.1 Part Numbers Fully Addressed by This Document

Table 22 provides the Freescale part numbering nomenclature for the MPC7457.

Table 22. Part Numbering Nomenclature

MC	74*x*7	*xx*	*nnnn*	L	*x*

Product Code	Part Identifier	Package	Processor Frequency [1]	Application Modifier	Revision Level
PPC [2] MC	7457 7447	RX = CBGA	867 1000 1200 1267	L: 1.3 V ± 50 mV 0° to 105°C	B: 1.1; PVR = 8002 0101
MC	7457	RX = CBGA VG = RoHS BGA	867 1000 1200 1267		C: 1.2; PVR = 8002 0102

Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by a hardware specification addendum may support other maximum core frequencies.
2. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

10.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed are described in a separate addendum, which supplement and supersede this hardware specification. As such parts are released, these specifications will be listed in this section.

Table 23. Part Numbers Addressed by MPC74x7RX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS01AD)

MC	74*x*7	*xx*	*nnnn*	N	*x*

Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
PPC	7457	RX = CBGA	1000 867 733 600	N: 1.1 V ± 50 mV 0° to 105°C	B: 1.1; PVR = 8002 0101
	7447		1000 867		
MC	7447		1000 867 733 600		B: 1.1; PVR = 8002 0101
	7457	RX = CBGA VG = RoHS BGA	1000 867 733 600		C: 1.2; PVR = 8002 0102

Table 24. Part Numbers Addressed by MPC7457TRX*nnnn*LB Series Hardware Specifications Addendum (Document Order No. MPC7457ECS02AD)

MC	7457	T	RX	*nnnn*	L	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7457	T = Extended Temperature Device	RX = CBGA	1000 1267	L: 1.3 V ± 50 mV –40° to 105°C	C: 1.2; PVR = 8002 0102

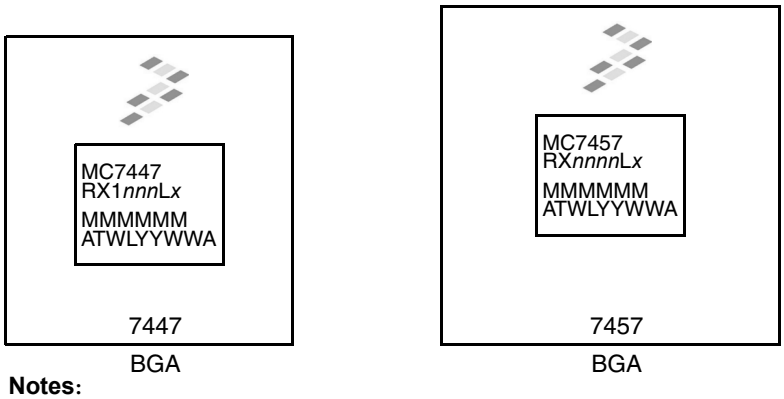
Table 25. Part Numbers Addressed by MPC7457TRX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS03AD)

MC	74*x*7	T	RX	*nnnn*	N	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7447	T = Extended Temperature Device	RX = CBGA	733 1000	N: 1.1 V ± 50 mV –40° to 105°C	B: 1.1; PVR = 8002 0101
	7457					C: 1.2; PVR = 8002 0102

10.3 Part Marking

Parts are marked as the examples shown in Figure 31.



Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.

Figure 31. Part Marking for BGA Device

Table 26. Document Revision History (continued)

Revision Number	Date	Substantive Change(s)
1		Removed support for 1.5 V L3 interface voltage from Tables 3 and 4. 1.5 V I/O voltage is not supported in current MPC7457 devices.
		Added package thermal characteristics values to Table 5, made minor revisions to Section 1.9.8.
		Added preliminary AC timing values to Tables 10 and 12.
		Added footnotes to Table 17.
0		Initial release.