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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7457rx1000nc

  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.3-V processor core
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state.
  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and an MPC7457-specific thermal management exception.
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Cache level	L3	L3	L3
Total SRAM space supported	1 MB, 2MB, 4 MB [2]	1 MB, 2 MB	1 MB, 2 MB
On-chip tag logical size (cache space)	1 MB, 2 MB	1 MB, 2 MB	1 MB, 2 MB
Associativity	8-way	8-way	8-way
Number of 32-byte sectors/line	2, 4	2, 4	2, 4
Off-Chip data SRAM support	MSUG2 DDR, LW, PB2	MSUG2 DDR, LW, PB2	MSUG2 DDR, LW, PB2
Data path width	64	64	64
Direct mapped SRAM sizes	1 MB, 2 MB, 4 MB	1 MB, 2 MB	1 MB, 2 MB
Parity	Byte	Byte	Byte

Notes:

1. Not implemented on MPC7447, MPC7445, or MPC7441.
2. The MPC7457 supports up to 4 MB of SRAM, of which a maximum of 2 MB can be configured as cache memory; the remaining 2 MB may be unused or configured as private memory.

4 General Parameters

The following list provides a summary of the general parameters of the MPC7457:

Technology	0.13 µm CMOS, nine-layer metal
Die size	9.1 mm × 10.8 mm
Transistor count	58 million
Logic design	Fully-static
Packages	MPC7447: Surface mount 360 ceramic ball grid array (CBGA)
	MPC7457: Surface mount 483 ceramic ball grid array (CBGA)
Core power supply	1.3 V ±50 mV DC nominal
I/O power supply	1.8 V ±5% DC, or
	2.5 V ±5% DC, or
	1.5 V ±5% DC (L3 interface only, not implemented on MPC7447)

5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7457.

5.1 DC Electrical Characteristics

The tables in this section describe the MPC7457 DC electrical characteristics.Table 2 provides the absolute maximum ratings.

Table 4 provides the recommended operating conditions for the MPC7457.

Table 4. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value		Unit	Notes
			Min	Max		
Core supply voltage		V_{DD}	1.3 V ± 50 mV		V	
PLL supply voltage		AV_{DD}	1.3 V ± 50 mV		V	2
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 5%		V	
	BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	OV_{DD}	2.5 V ± 5%		V	
L3 bus supply voltage	L3VSEL = 0	GV_{DD}	1.8 V ± 5%		V	
	L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	GV_{DD}	2.5 V ± 5%		V	
	L3VSEL = ¬$\overline{\text{HRESET}}$	GV_{DD}	1.5 V ± 5%		V	3
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	V	
	L3 bus	V_{in}	GND	GV_{DD}	V	
	JTAG signals	V_{in}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. This voltage is the input to the filter discussed in Section 9.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

Table 5 provides the package thermal characteristics for the MPC7457.

Table 5. Package Thermal Characteristics [1]

Characteristic	Symbol	Value		Unit	Notes
		MPC7447	MPC7457		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	22	20	°C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	14	14	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	16	15	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	11	11	°C/W	2, 4
Junction-to-board thermal resistance	$R_{\theta JB}$	6	6	°C/W	5
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	°C/W	6

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		867 MHz		1000 MHz		1200 MHz		1267 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Internal PLL relock time		—	100	—	100	—	100	—	100	µs	7

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, “PLL Configuration,” for valid PLL_CFG[0:4] settings.
2. Assumes lightly-loaded, single-processor system; see Section 5.2.1, “Clock AC Specifications” for more information.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver’s closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

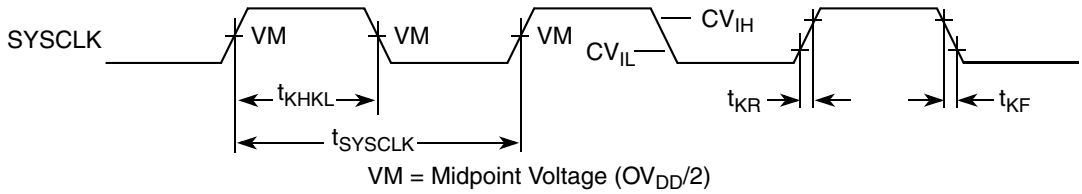


Figure 3. SYSCLK Input Timing Diagram

5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 as defined in Figure 4 and Figure 5. Timing specifications for the L3 bus are provided in Section 5.2.3, “L3 Clock AC Specifications.”

Table 9. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Revisions and Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{\text{TS}}$ is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue because any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ can be driven by multiple bus masters beginning the cycle of $\overline{\text{TS}}$. Timing is the same as $\overline{\text{ARTRY}}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{\text{BMODE}}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{\text{HRESET}}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 5 for sample timing.

Figure 4 provides the AC test load for the MPC7457.

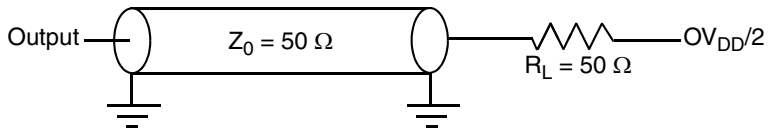


Figure 4. AC Test Load

Figure 5 provides the mode select input timing diagram for the MPC7457.

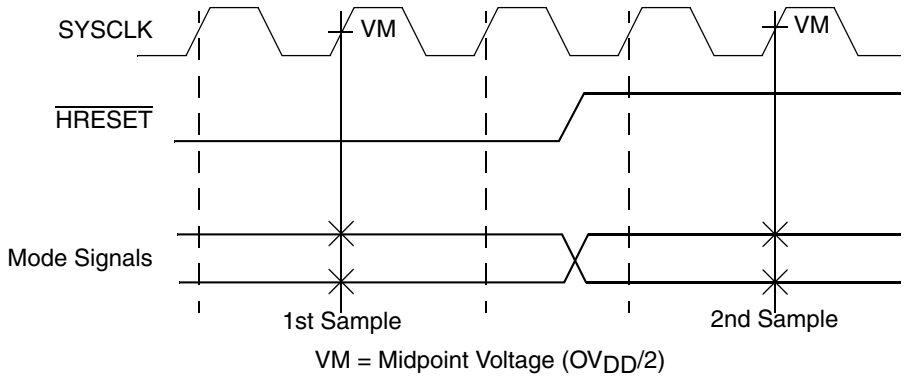


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7457.

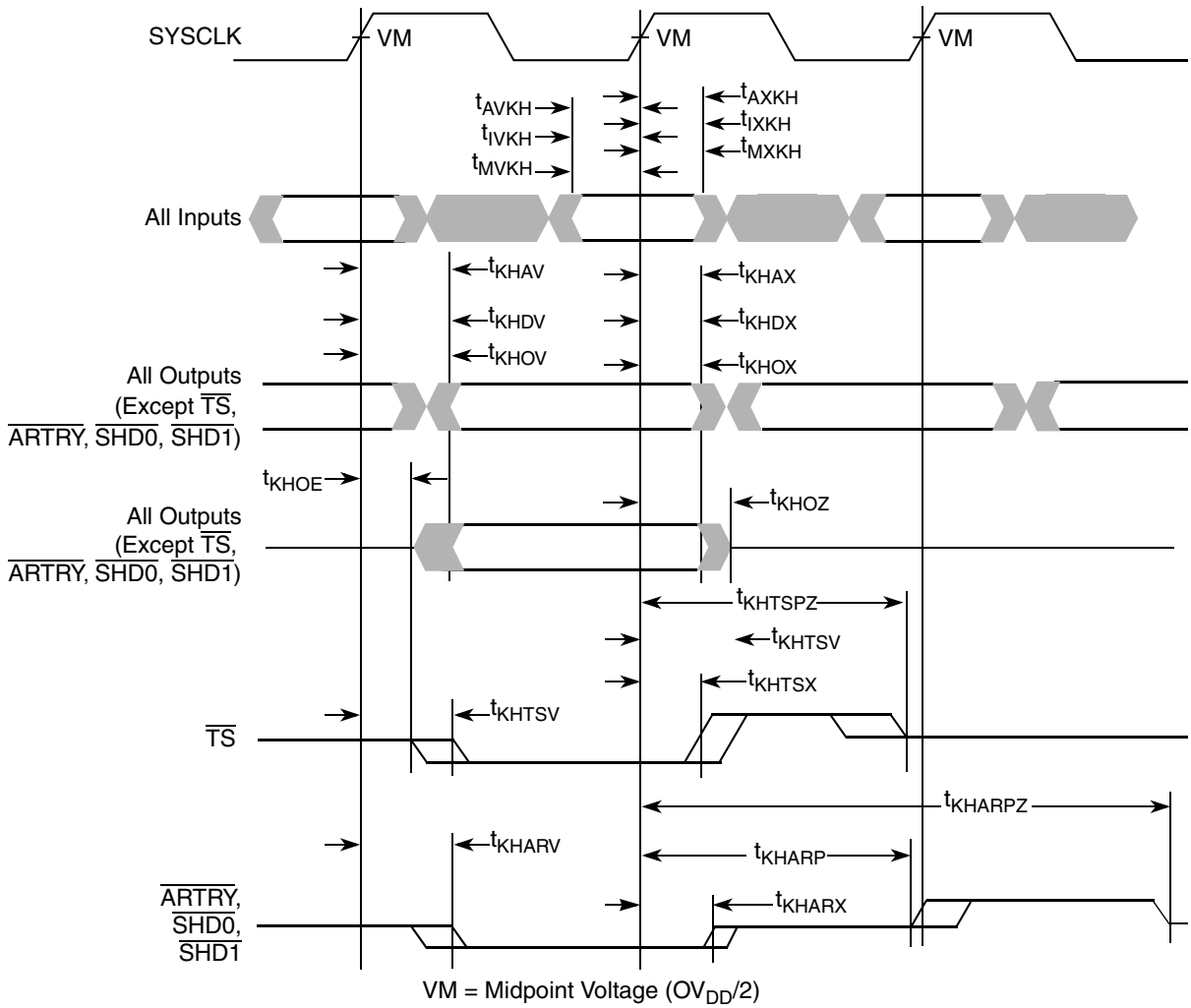


Figure 6. Input/Output Timing Diagram

5.2.4 L3 Bus AC Specifications

The MPC7457 L3 interface supports three different types of SRAM: source-synchronous, double data rate (DDR) MSUG2 SRAM, Late Write SRAMs, and pipeline burst (PB2) SRAMs. Each requires a different protocol on the L3 interface and a different routing of the L3 clock signals. The type of SRAM is programmed in L3CR[22:23] and the MPC7457 then follows the appropriate protocol for that type. The designer must connect and route the L3 signals appropriately for each type of SRAM. Following are some observations about the L3 interface.

- The routing for the point-to-point signals (L3_CLK[0:1], L3DATA[0:63], L3DP[0:7], and L3_ECHO_CLK[0:3]) to a particular SRAM must be delay matched.
- For 1-Mbyte of SRAM, use L3_ADDR[16:0] (L3_ADDR[0] is LSB)
- For 2-Mbyte of SRAM, use L3_ADDR[17:0] (L3_ADDR[0] is LSB)
- For 4-Mbyte of SRAM, use L3_ADDR[18:0] (L3_ADDR[0] is LSB)
- No pull-up resistors are required for the L3 interface
- For high-speed operations, L3 interface address and control signals should be a ‘T’ with minimal stubs to the two loads; data and clock signals should be point-to-point to their single load. Figure 8 shows the AC test load for the L3 interface.

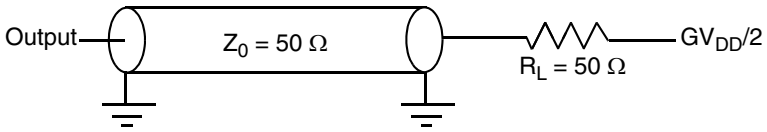


Figure 8. AC Test Load for the L3 Interface

In general, if routing is short, delay-matched, and designed for incident wave reception and minimal reflection, there is a high probability that the AC timing of the MPC7457 L3 interface will meet the maximum frequency operation of appropriately chosen SRAMs. This is despite the pessimistic, guard-banded AC specifications (see Table 12, Table 13, and Table 14), the limitations of functional testers described in Section 5.2.3, “L3 Clock AC Specifications,” and the uncertainty of clocks and signals which inevitably make worst-case critical path timing analysis pessimistic.

More specifically, certain signals within groups should be delay-matched with others in the same group while intergroup routing is less critical. Only the address and control signals are common to both SRAMs and additional timing margin is available for these signals. The double-clocked data signals are grouped with individual clocks as shown in Figure 9 or Figure 11, depending on the type of SRAM. For example, for the MSUG2 DDR SRAM (see Figure 9); L3DATA[0:31], L3DP[0:3], and L3_CLK[0] form a closely coupled group of outputs from the MPC7457; while L3DATA[0:15], L3DP[0:1], and L3_ECHO_CLK[0] form a closely coupled group of inputs.

The *MPC7450 RISC Microprocessor Family User’s Manual* refers to logical settings called ‘sample points’ used in the synchronization of reads from the receive FIFO. The computation of the correct value for this setting is system-dependent and is described in the *MPC7450 RISC Microprocessor Family User’s Manual*. Three specifications are used in this calculation and are given in Table 11. It is essential that all three specifications are included in the calculations to determine the sample points, as incorrect settings can result in errors and unpredictable behavior. For more information, see the *MPC7450 RISC Microprocessor Family User’s Manual.*

Table 12. Effect of L3OHCR Settings on L3 Bus AC Timing (continued)

At recommended operating conditions. See Table 4.

Field Name[1]	Affected Signals	Value	Output Valid Time		Output Hold Time		Unit	Notes
			Parameter Symbol [2]	Change [3]	Parameter Symbol [2]	Change [3]		
L3CLK*n*_OH	All signals latched by SRAM connected to L3_CLK*n*	0b000	t_{L3CHOV}, t_{L3CHDV}, t_{L3CLDV}	0	t_{L3CHOX}, t_{L3CHDX}, t_{L3CLDX}	0	ps	4
		0b001		– 50		– 50		5
		0b010		– 100		– 100		5
		0b011		– 150		– 150		5
		0b100		– 200		– 200		5
		0b101		– 250		– 250		5
		0b110		– 300		– 300		5
		0b111		– 350		– 350		5
L3DOH*n*	L3_DATA[*n*:*n*+7], L3_DP[*n*/8]	0b000	t_{L3CHDV}, t_{L3CLDV}	0	t_{L3CHDX}, t_{L3CLDX}	0	ps	4
		0b001		+ 50		+ 50		
		0b010		+ 100		+ 100		
		0b011		+ 150		+ 150		
		0b100		+ 200		+ 200		
		0b101		+ 250		+ 250		
		0b111		+ 300		+ 300		
		0b111		+ 350		+ 350		

Notes:

1. See the *MPC7450 RISC Microprocessor Family User's Manual* for specific information regarding L3OHCR.
2. See Table 13 and Table 14 for more information.
3. Approximate delay verified by simulation; not tested or characterized.
4. Default value.
5. Increasing values of L3CLK*n*_OH delay the L3_CLK*n* signal, effectively decreasing the output valid and output hold times of all signals latched relative to that clock signal by the SRAM; see Figure 9 and Figure 11.

5.2.4.2 L3 Bus AC Specifications for DDR MSUG2 SRAMs

When using DDR MSUG2 SRAMs at the L3 interface, the parts should be connected as shown in Figure 9. Outputs from the MPC7457 are actually launched on the edges of an internal clock phase-aligned to SYSCLK (adjusted for core and L3 frequency divisors). L3_CLK0 and L3_CLK1 are this internal clock output with 90° phase delay, so outputs are shown synchronous to L3_CLK0 and L3_CLK1. Output valid times are typically negative when referenced to L3_CLK*n* because the data is launched one-quarter period before L3_CLK*n* to provide adequate setup time at the SRAM after the delay-matched address, control, data, and L3_CLK*n* signals have propagated across the printed-wiring board.

Inputs to the MPC7457 are source-synchronous with the CQ clock generated by the DDR MSUG2 SRAMs. These CQ clocks are received on the L3_ECHO_CLK*n* inputs of the MPC7457. An internal circuit delays the incoming L3_ECHO_CLK*n* signal such that it is positioned within the valid data

Table 13. L3 Bus Interface AC Timing Specifications for MSUG2 (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [9]				Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)		Rev 1.2 (1.8-, 2.5-V I/O Modes)			
		Min	Max	Min	Max		
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	(t_{L3CLK}/4) + 0.65	—	(t_{L3CLK}/4) + 0.65	ns	

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLK*n* as shown in Figure 10. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the MPC7457 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLK*n* at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 8).
6. For DDR, the output data will typically lead the edge of L3_CLK*n* as shown in Figure 10. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock before the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
8. Assumes default value of L3OHCR. See Section 5.2.4.1, “Effects of L3OHCR Settings on L3 Bus AC Specifications,” for more information.
9. L3 I/O voltage mode must be configured by L3VSEL as described in Table 3, and voltage supplied at GV_{DD} must match mode selected as specified in Table 4. See Table 22 for revision level information and part marking.

Figure 12 shows the L3 bus timing diagrams for the MPC7457 interfaced to PB2 or Late Write SRAMs.

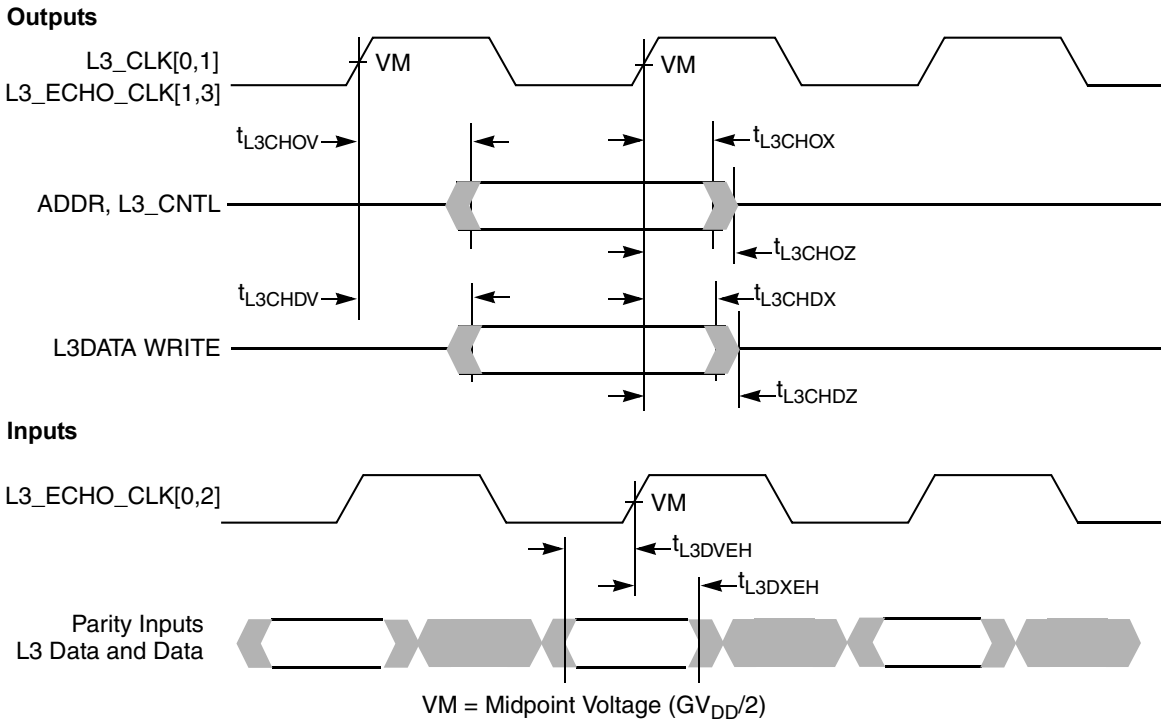


Figure 12. L3 Bus Timing Diagrams for Late Write or PB2 SRAMs

5.2.5 IEEE 1149.1 AC Timing Specifications

Table 15 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 14 through Figure 17.

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
TCK frequency of operation	f_{TCLK}	0	33.3	MHz	
TCK cycle time	t_{TCLK}	30	—	ns	
TCK clock pulse width measured at 1.4 V	t_{JHJL}	15	—	ns	
TCK rise and fall times	t_{JR} and t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times: Boundary-scan data TMS, TDI	 t_{DVJH} t_{IVJH}	 4 0	 — —	ns	3
Input hold times: Boundary-scan data TMS, TDI	 t_{DXJH} t_{IXJH}	 20 25	 — —	ns	3

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 13). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 13 provides the AC test load for TDO and the boundary-scan outputs of the MPC7457.

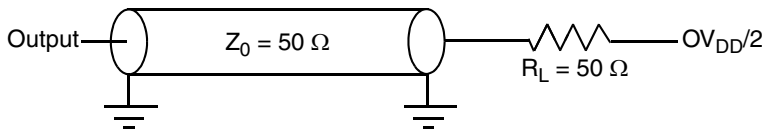


Figure 13. Alternate AC Test Load for the JTAG Interface

Figure 14 provides the JTAG clock input timing diagram.

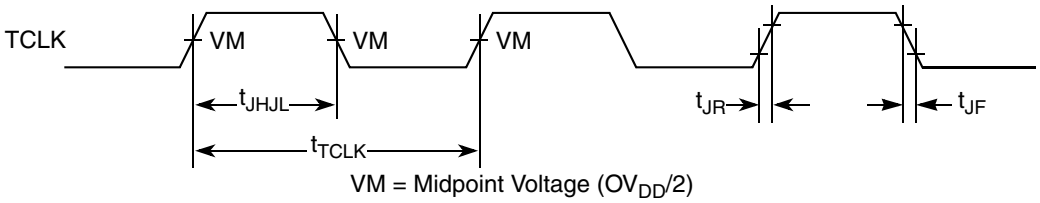


Figure 14. JTAG Clock Input Timing Diagram

Figure 15 provides the $\overline{\text{TRST}}$ timing diagram.

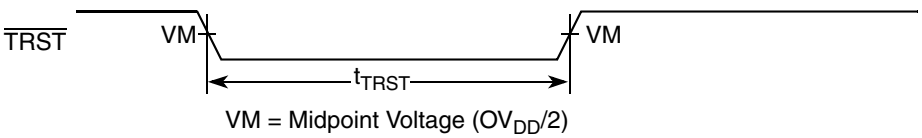
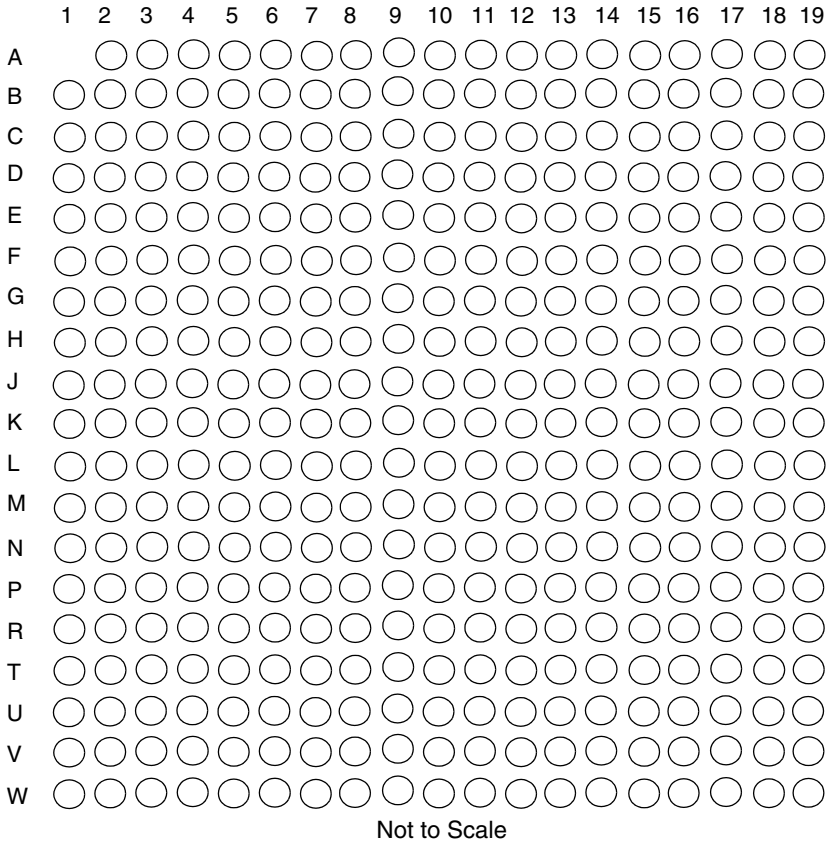


Figure 15. $\overline{\text{TRST}}$ Timing Diagram

6 Pin Assignments

Figure 18 (Part A) shows the pinout of the MPC7447, 360 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

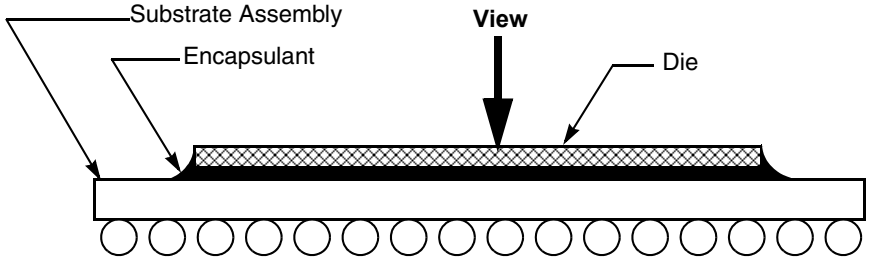


Figure 18. Pinout of the MPC7447, 360 CBGA Package as Viewed from the Top Surface

Table 16. Pinout Listing for the MPC7447, 360 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
$\overline{\text{TEA}}$	L1	Low	Input	BVSEL	
TEST[0:3]	A12, B6, B10, E10	—	Input	BVSEL	12
TEST[4]	D10	—	Input	BVSEL	9
TMS	F1	High	Input	BVSEL	6
$\overline{\text{TRST}}$	A5	Low	Input	BVSEL	6, 14
$\overline{\text{TS}}$	L4	Low	I/O	BVSEL	3
TSIZ[0:2]	G6, F7, E7	High	Output	BVSEL	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	BVSEL	
$\overline{\text{WT}}$	D3	Low	Output	BVSEL	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	N/A	

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). To program the I/O voltage, connect BVSEL to either GND (selects 1.8 V) or to $\overline{\text{HRESET}}$ (selects 2.5 V). If used, the pull-down resistor should be less than 250 Ω. For actual recommended value of V_{in} or supply voltages see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7447 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by $\neg\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7447 is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
A[0:35]	E10, N4, E8, N5, C8, R2, A7, M2, A6, M1, A10, U2, N2, P8, M8, W4, N6, U6, R5, Y4, P1, P4, R6, M7, N7, AA3, U4, W2, W1, W3, V4, AA1, D10, J4, G10, D9	High	I/O	BVSEL	2
$\overline{\text{AACK}}$	U1	Low	Input	BVSEL	
AP[0:4]	L5, L6, J1, H2, G5	High	I/O	BVSEL	
$\overline{\text{ARTRY}}$	T2	Low	I/O	BVSEL	3

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
TDI	E4	High	Input	BVSEL	7
TDO	H1	High	Output	BVSEL	
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL	
TEST[0:5]	B10, H6, H10, D8, F9, F8	—	Input	BVSEL	13
TEST[6]	A9	—	Input	BVSEL	10
TMS	K4	High	Input	BVSEL	7
$\overline{\text{TRST}}$	C1	Low	Input	BVSEL	7, 16
$\overline{\text{TS}}$	P5	Low	I/O	BVSEL	3
TSIZ[0:2]	L1,H3,D1	High	Output	BVSEL	
TT[0:4]	F1, F4, K8, A5, E1	High	I/O	BVSEL	
$\overline{\text{WT}}$	L2	Low	Output	BVSEL	
V_{DD}	J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14	—	—	N/A	
VDD_SENSE[0:1]	G11, J8	—	—	N/A	17

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); GV_{DD} supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals $\overline{\text{L3\_CNTL}}$[0:1]; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). For actual recommended value of V_{in} or supply voltages, see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. See Table 3 for bus voltage configuration information. If used, pull-down resistors should be less than 250 Ω.
7. Internal pull up on die.
8. Ignored in 60x bus mode.
9. These signals must be pulled down to GND if unused or if the MPC7457 is in 60x bus mode.
10. These input signals for factory use only and must be pulled down to GND for normal machine operation.
11. Power must be supplied to GV_{DD}, even when the L3 interface is disabled or unused.
12. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
14. These signals are for factory use only and must be left unconnected for normal machine operation.
15. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
16. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
17. These pins are internally connected to V_{DD}. They are intended to allow an external device to detect the core voltage level present at the processor core. If unused, they must be connected directly to V_{DD} or left unconnected.

9 System Design Information

This section provides system and thermal design recommendations for successful application of the MPC7457.

9.1 Clocks

The following sections provide more detailed information regarding the clocking of the MPC7457.

9.1.1 Core Clocks and PLL Configuration

The MPC7457 PLL is configured by the PLL_CFG[0:4] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7457 is shown in Table 18 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 1-GHz column in Table 8. Note that these configurations were different in some earlier MPC7450-family devices and care should be taken when upgrading to the MPC7457 to verify the correct PLL settings for an application.

Table 18. MPC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts

PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
01000	2x	2x								
10000	3x	2x								
10100	4x	2x								667 (1333)
10110	5x	2x							667 (1333)	835 (1670)
10010	5.5x	2x							733 (1466)	919 (1837)
11010	6x	2x						600 (1200)	800 (1600)	1002 (2004)
01010	6.5x	2x						650 (1300)	866 (1730)	1086 (2171)
00100	7x	2x						700 (1400)	931 (1862)	1169 (2338)
00010	7.5x	2x					623 (1245)	750 (1500)	1000 (2000)	1253 (2505)
11000	8x	2x				600 (1200)	664 (1328)	800 (1600)	1064 (2128)	
01100	8.5x	2x				638 (1276)	706 (1412)	850 (1700)	1131 (2261)	

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L3 interface does not normally require pull-up resistors. Unused L3_ADDR signals are driven low when the SRAM is configured to be less than 1 M in size via L3CR. For example, L3_ADD[18] will be driven low if the SRAM size is configured to be 2 M; likewise, L3_ADDR[18:17] will be driven low if the SRAM size is configured to be 1 M.

9.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 26 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

9.8.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 29 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 27). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure and is recommended due to the high power dissipation of the MPC7457. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

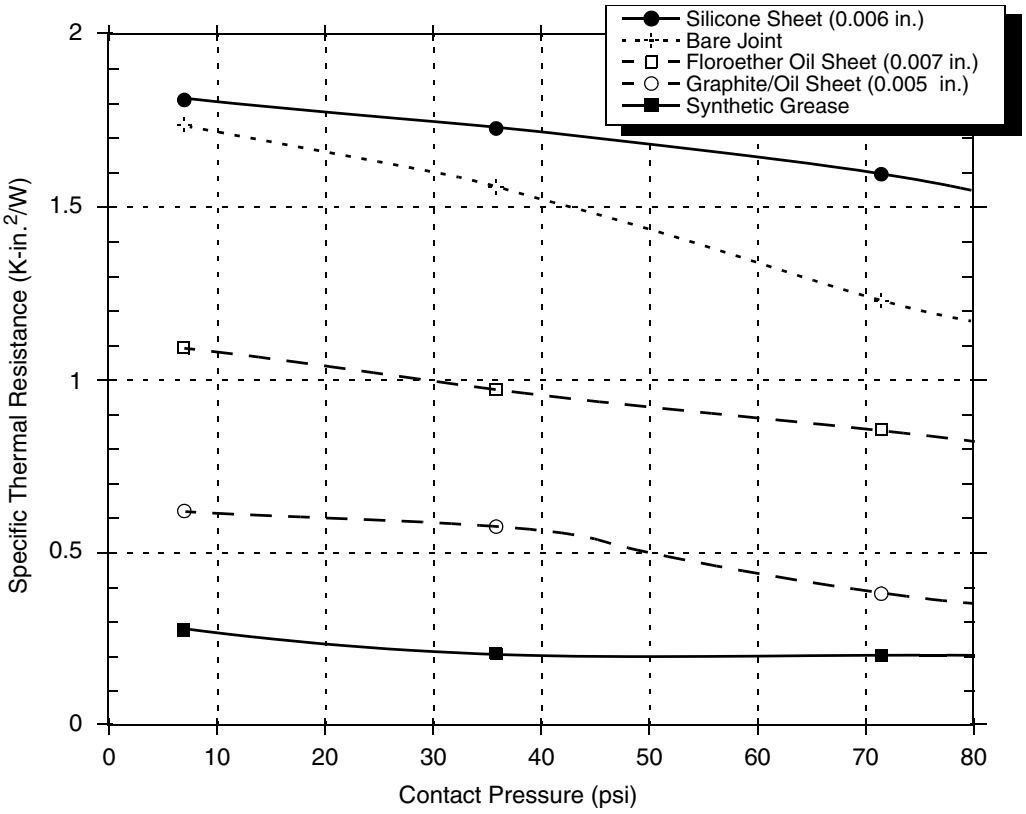


Figure 29. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

example, assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 18.7\ W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the MPC7447 and MPC7457 thermal model is shown in Figure 30. Four volumes will be used to represent this device. Two of the volumes, solder ball, and air and substrate, are modeled using the package outline size of the package. The other two, die, and bump and underfill, have the same size as the die. The silicon die should be modeled 9.64 × 11.0 × 0.74 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 9.64 × 11.0 × 0.069 mm (or as a collapsed volume) with orthotropic material properties: 0.6 W/(m • K) in the xy-plane and 2 W/(m • K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm (MPC7447) or 29 × 29 × 1.2 mm (MPC7457), and this volume has 18 W/(m • K) isotropic conductivity. The solder ball and air layer is modeled with the same horizontal dimensions as the substrate and is 0.9 mm thick. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 3.8 W/(m • K) in the direction of the z-axis.

Table 26. Document Revision History (continued)

Revision Number	Date	Substantive Change(s)
4		Table 9: Corrected pin lists for input and output AC timing to correctly show $\overline{\text{HIT}}$ as an output-only signal
		Added specifications for 1267 MHz devices; removed specs for 1300 MHz devices.
		Section 5.2.3: Changed recommendations regarding use of L3 clock jitter in AC timing analysis. The L3 jitter is now fully comprehended in the AC timing specs and does not need to be included in the timing analysis.
3		Corrected numerous errors in lists of pins associated with t_{KHOV}, t_{KHOX}, t_{IVKH}, and t_{IXKH} in Table 9.
		Added support for 1.5 V L3 interface voltage; issues fixed in Rev. 1.1.
		Corrected typos in Table 12.
		Added data to Table 2.
		Clarified address bus pull-up resistor recommendations in Section 1.9.6.
		Modified Table 9, Figure 5, and Figure 6 to more accurately show when the mode select inputs ($\overline{\text{BMODE}}$[0:1], L3VSEL, BVSEL) are sampled and AC timing requirements
		Table 10: Added skew and jitter values.
		Table 14: Added AC timing values.
		Table 24: Updated to reflect past and current part numbers not fully covered by this document.
		Table 6: Removed CV_{IH} and CV_{IL}; V_{IH} and V_{IL} for SYSCLK input is the same as for other input signals, and is now noted accordingly in this table.
		Table 7: Removed Doze mode power entry (but left footnote 4 for clarity); documentation change only.
		Nontechnical formatting
2		Added substrate capacitor information in Sections 1.8.3 and 1.8.6.
		Increased minimum processor and VCO frequencies in Table 8 from 500 and 1000 MHz to 600 and 1200 MHz (respectively).
		Corrected maximum processor frequency for 1300 MHz devices in Table 8 (changed from 1333 to 1300 MHz).
		Added value for to $t_{L3CSKW1}$ Table 10.
		Added L3OHCR information in Section 1.5.2.4.1.
		Added values for t_{CO} and t_{ECI} to Table 11.
		Added Note 8 to Table 13 and Note 6 to Table 14.
		Changed resistor value in PLL filter in Figure 25 from 10 Ω to 400 Ω.
		Added 867 MHz speed grade.
		Corrected Product Code in Tables 22 and 23.
		Added pull-up/pull-down recommendations for $\overline{\text{CKSTP\_IN}}$ and PLL_CFG[0:4] to Section 1.9.6.
1.1		Nontechnical reformatting.

Table 26. Document Revision History (continued)

Revision Number	Date	Substantive Change(s)
1		Removed support for 1.5 V L3 interface voltage from Tables 3 and 4. 1.5 V I/O voltage is not supported in current MPC7457 devices.
		Added package thermal characteristics values to Table 5, made minor revisions to Section 1.9.8.
		Added preliminary AC timing values to Tables 10 and 12.
		Added footnotes to Table 17.
0		Initial release.