Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	733MHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7457rx733nc

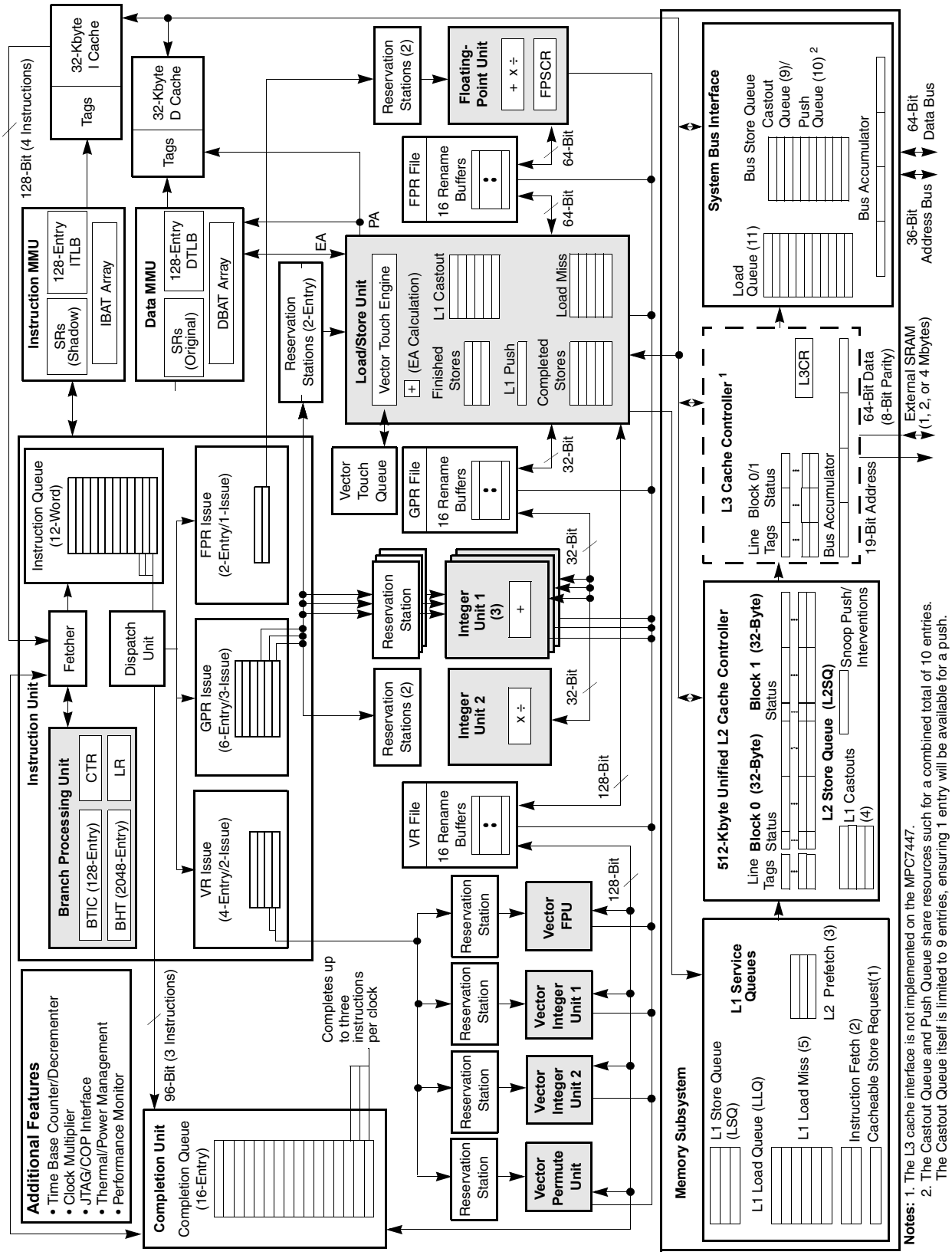


Figure 1. MPC7457 Block Diagram

  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.3-V processor core
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state.
  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and an MPC7457-specific thermal management exception.
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

Table 4 provides the recommended operating conditions for the MPC7457.

Table 4. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value		Unit	Notes
			Min	Max		
Core supply voltage		V_{DD}	1.3 V ± 50 mV		V	
PLL supply voltage		AV_{DD}	1.3 V ± 50 mV		V	2
Processor bus supply voltage	BVSEL = 0	OV_{DD}	1.8 V ± 5%		V	
	BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	OV_{DD}	2.5 V ± 5%		V	
L3 bus supply voltage	L3VSEL = 0	GV_{DD}	1.8 V ± 5%		V	
	L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	GV_{DD}	2.5 V ± 5%		V	
	L3VSEL = ¬$\overline{\text{HRESET}}$	GV_{DD}	1.5 V ± 5%		V	3
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	V	
	L3 bus	V_{in}	GND	GV_{DD}	V	
	JTAG signals	V_{in}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. This voltage is the input to the filter discussed in Section 9.2, “PLL Power Supply Filtering,” and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

Table 5 provides the package thermal characteristics for the MPC7457.

Table 5. Package Thermal Characteristics [1]

Characteristic	Symbol	Value		Unit	Notes
		MPC7447	MPC7457		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	22	20	°C/W	2, 3
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	14	14	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	16	15	°C/W	2, 4
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	11	11	°C/W	2, 4
Junction-to-board thermal resistance	$R_{\theta JB}$	6	6	°C/W	5
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	°C/W	6

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		867 MHz		1000 MHz		1200 MHz		1267 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Internal PLL relock time		—	100	—	100	—	100	—	100	µs	7

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, “PLL Configuration,” for valid PLL_CFG[0:4] settings.
2. Assumes lightly-loaded, single-processor system; see Section 5.2.1, “Clock AC Specifications” for more information.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver’s closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

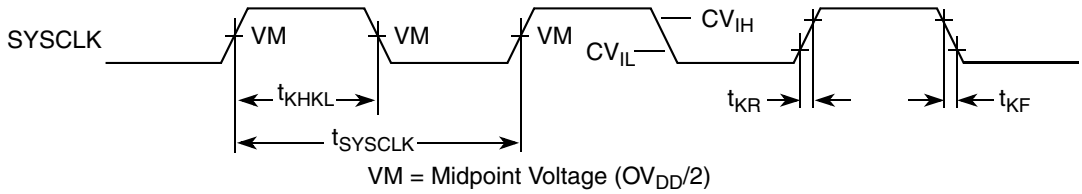


Figure 3. SYSCLK Input Timing Diagram

5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 as defined in Figure 4 and Figure 5. Timing specifications for the L3 bus are provided in Section 5.2.3, “L3 Clock AC Specifications.”

5.2.3 L3 Clock AC Specifications

The L3_CLK frequency is programmed by the L3 configuration register core-to-L3 divisor ratio. See Table 18 for example core and L3 frequencies at various divisors. Table 10 provides the potential range of L3_CLK output AC timing specifications as defined in Figure 7.

The maximum L3_CLK frequency is the core frequency divided by two. Given the high core frequencies available in the MPC7457, however, most SRAM designs will be not be able to operate in this mode using current technology and, as a result, will select a greater core-to-L3 divisor to provide a longer L3_CLK period for read and write access to the L3 SRAMs. Therefore, the typical L3_CLK frequency shown in Table 10 is considered to be the practical maximum in a typical system. The maximum L3_CLK frequency for any application of the MPC7457 will be a function of the AC timings of the MPC7457, the AC timings for the SRAM, bus loading, and printed-circuit board trace length, and may be greater or less than the value given in Table 10. Note that SYSCLK input jitter and L3_CLK[0:1] output jitter are already comprehended in the L3 bus AC timing specifications and do not need to be separately accounted for in an L3 AC timing analysis. Clock skews, where applicable, do need to be accounted for in an AC timing analysis.

Freescale is similarly limited by system constraints and cannot perform tests of the L3 interface on a socketed part on a functional tester at the maximum frequencies of Table 10. Therefore, functional operation and AC timing information are tested at core-to-L3 divisors which result in L3 frequencies at 250 MHz or lower.

Table 10. L3_CLK Output AC Timing Specifications

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [6]						Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)			Rev 1.2 (1.8-, 2.5-V I/O Modes)				
		Min	Typ	Max	Min	Typ	Max		
L3 clock frequency	f_{L3_CLK}	—	200	—	—	250	—	MHz	1
L3 clock cycle time	t_{L3_CLK}	—	5.0	—	—	4.0	—	ns	1
L3 clock duty cycle	t_{CHCL}/t_{L3_CLK}	—	50	—	—	50	—	%	2
L3 clock output-to-output skew (L3_CLK0 to L3_CLK1)	$t_{L3CSKW1}$	—	—	100	—	—	100	ps	3
L3 clock output-to-output skew (L3_CLK[0:1] to L3_ECHO_CLK[1,3])	$t_{L3CSKW2}$	—	—	100	—	—	100	ps	4

Table 10. L3_CLK Output AC Timing Specifications (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [6]						Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)			Rev 1.2 (1.8-, 2.5-V I/O Modes)				
		Min	Typ	Max	Min	Typ	Max		
L3 clock jitter		—	—	± 75	—	—	± 75	ps	5

Notes:

1. The maximum L3 clock frequency (and minimum L3 clock period) will be system dependent. See Section 5.2.3, "L3 Clock AC Specifications," for an explanation that this maximum frequency is not functionally tested at speed by Freescale. The minimum L3 clock frequency and period are f_{SYSCLK} and t_{SYSCLK}, respectively.
2. The nominal duty cycle of the L3 output clocks is 50% measured at midpoint voltage.
3. Maximum possible skew between L3_CLK0 and L3_CLK1. This parameter is critical to the address and control signals which are common to both SRAM chips in the L3.
4. Maximum possible skew between L3_CLK0 and L3_ECHO_CLK1 or between L3_CLK1 and L3_ECHO_CLK3 for PB2 or Late Write SRAM. This parameter is critical to the read data signals because the processor uses the feedback loop to latch data driven from the SRAM, each of which drives data based on L3_CLK0 or L3_CLK1.
5. Guaranteed by design and not tested. The input jitter on SYSCLK affects L3 output clocks and the L3 address, data, and control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L3 timing analysis. The clock-to-clock jitter shown here is uncertainty in the internal clock period caused by supply voltage noise or thermal effects. This is also comprehended in the AC timing specifications and need not be considered in the L3 timing analysis.
6. L3 I/O voltage mode must be configured by L3VSEL as described in Table 3, and voltage supplied at GV_{DD} must match mode selected as specified in Table 4. See Table 22 for revision level information and part marking.

The L3_CLK timing diagram is shown in Figure 7.

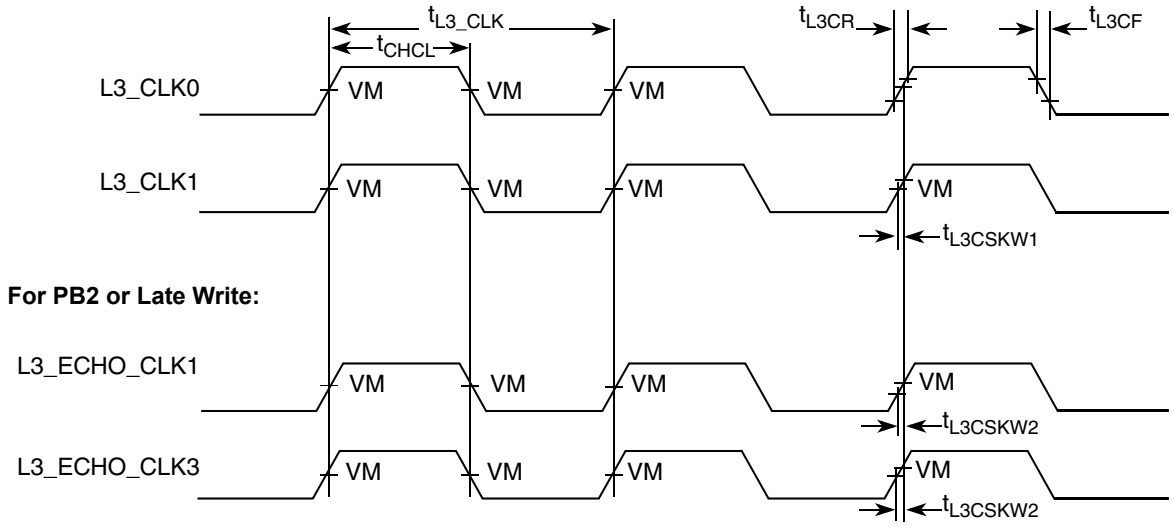


Figure 7. L3_CLK_OUT Output Timing Diagram

Table 12. Effect of L3OHCR Settings on L3 Bus AC Timing (continued)

At recommended operating conditions. See Table 4.

Field Name[1]	Affected Signals	Value	Output Valid Time		Output Hold Time		Unit	Notes
			Parameter Symbol [2]	Change [3]	Parameter Symbol [2]	Change [3]		
L3CLK*n*_OH	All signals latched by SRAM connected to L3_CLK*n*	0b000	t_{L3CHOV}, t_{L3CHDV}, t_{L3CLDV}	0	t_{L3CHOX}, t_{L3CHDX}, t_{L3CLDX}	0	ps	4
		0b001		– 50		– 50		5
		0b010		– 100		– 100		5
		0b011		– 150		– 150		5
		0b100		– 200		– 200		5
		0b101		– 250		– 250		5
		0b110		– 300		– 300		5
		0b111		– 350		– 350		5
L3DOH*n*	L3_DATA[*n*:*n*+7], L3_DP[*n*/8]	0b000	t_{L3CHDV}, t_{L3CLDV}	0	t_{L3CHDX}, t_{L3CLDX}	0	ps	4
		0b001		+ 50		+ 50		
		0b010		+ 100		+ 100		
		0b011		+ 150		+ 150		
		0b100		+ 200		+ 200		
		0b101		+ 250		+ 250		
		0b111		+ 300		+ 300		
		0b111		+ 350		+ 350		

Notes:

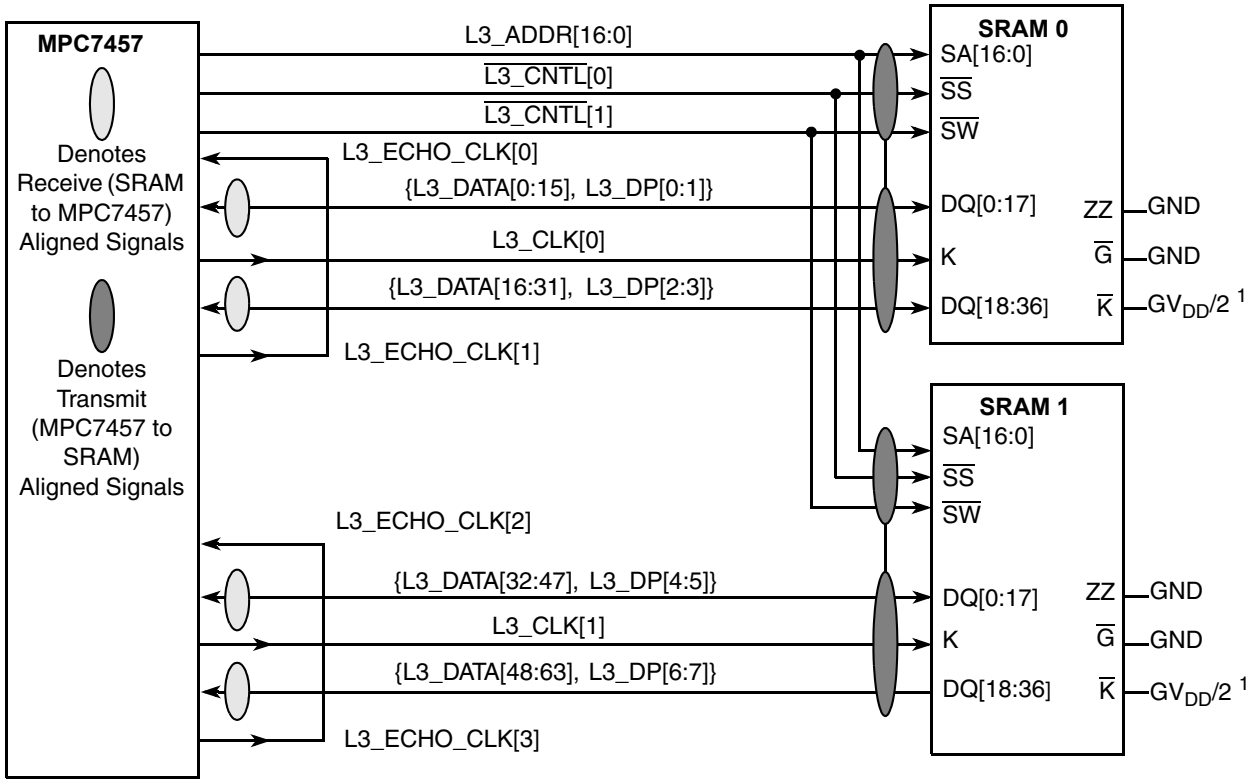
1. See the *MPC7450 RISC Microprocessor Family User's Manual* for specific information regarding L3OHCR.
2. See Table 13 and Table 14 for more information.
3. Approximate delay verified by simulation; not tested or characterized.
4. Default value.
5. Increasing values of L3CLK*n*_OH delay the L3_CLK*n* signal, effectively decreasing the output valid and output hold times of all signals latched relative to that clock signal by the SRAM; see Figure 9 and Figure 11.

5.2.4.2 L3 Bus AC Specifications for DDR MSUG2 SRAMs

When using DDR MSUG2 SRAMs at the L3 interface, the parts should be connected as shown in Figure 9. Outputs from the MPC7457 are actually launched on the edges of an internal clock phase-aligned to SYSCLK (adjusted for core and L3 frequency divisors). L3_CLK0 and L3_CLK1 are this internal clock output with 90° phase delay, so outputs are shown synchronous to L3_CLK0 and L3_CLK1. Output valid times are typically negative when referenced to L3_CLK*n* because the data is launched one-quarter period before L3_CLK*n* to provide adequate setup time at the SRAM after the delay-matched address, control, data, and L3_CLK*n* signals have propagated across the printed-wiring board.

Inputs to the MPC7457 are source-synchronous with the CQ clock generated by the DDR MSUG2 SRAMs. These CQ clocks are received on the L3_ECHO_CLK*n* inputs of the MPC7457. An internal circuit delays the incoming L3_ECHO_CLK*n* signal such that it is positioned within the valid data

Figure 11 shows the typical connection diagram for the MPC7457 interfaced to PB2 SRAMs or Late Write SRAMs.



Note:
1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 11. Typical Synchronous 1-MByte L3 Cache Late Write or PB2 Interface

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 13). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 13 provides the AC test load for TDO and the boundary-scan outputs of the MPC7457.

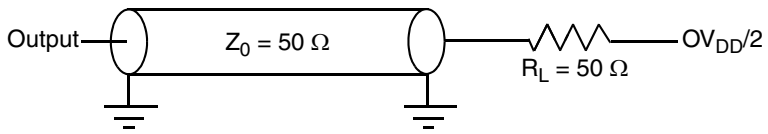


Figure 13. Alternate AC Test Load for the JTAG Interface

Figure 14 provides the JTAG clock input timing diagram.

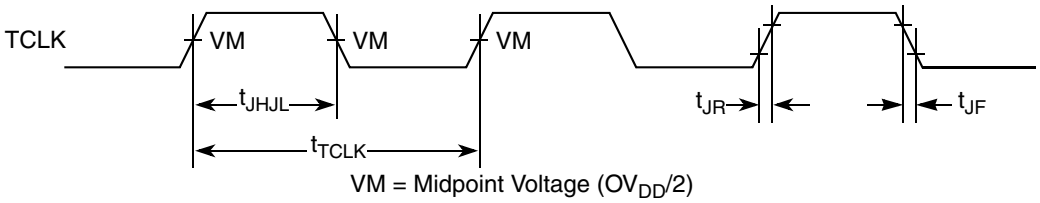


Figure 14. JTAG Clock Input Timing Diagram

Figure 15 provides the $\overline{\text{TRST}}$ timing diagram.

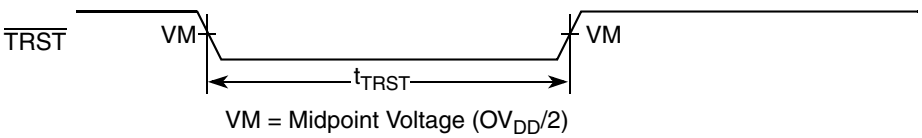
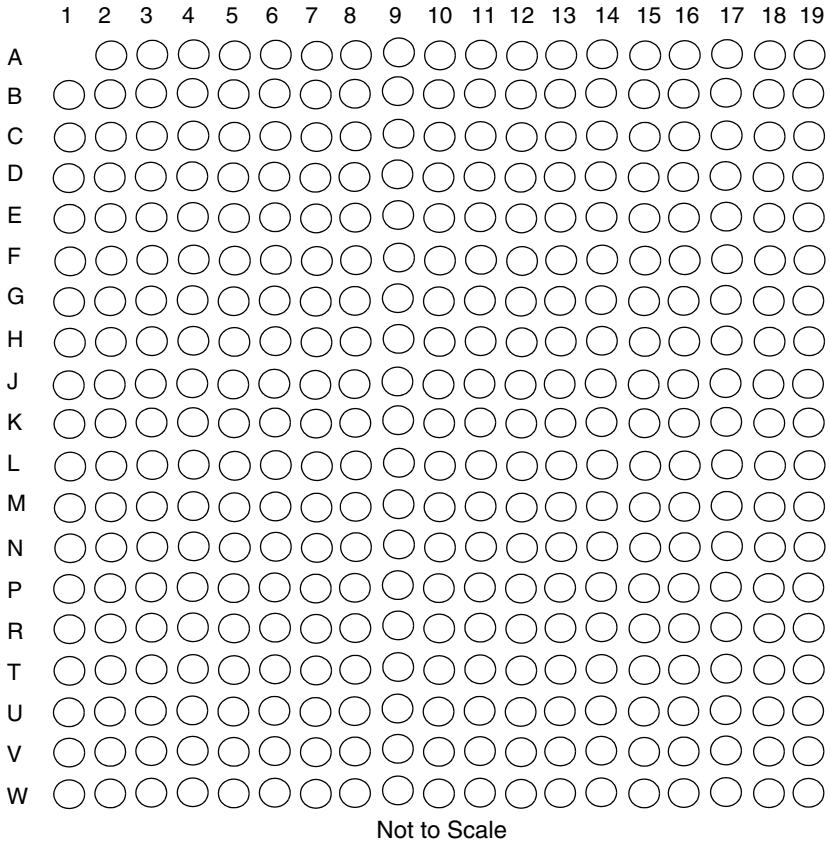


Figure 15. $\overline{\text{TRST}}$ Timing Diagram

6 Pin Assignments

Figure 18 (Part A) shows the pinout of the MPC7447, 360 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

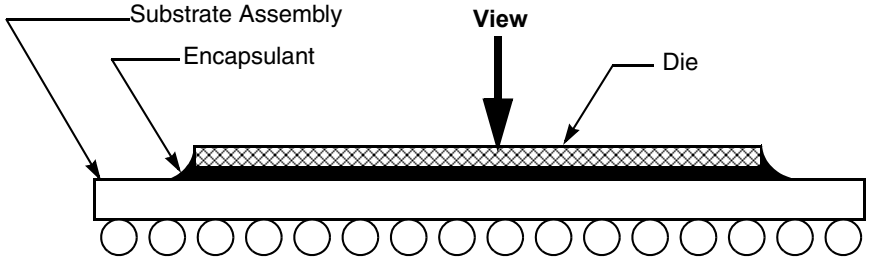


Figure 18. Pinout of the MPC7447, 360 CBGA Package as Viewed from the Top Surface

7 Pinout Listings

Table 16 provides the pinout listing for the MPC7447, 360 CBGA package. Table 17 provides the pinout listing for the MPC7457, 483 CBGA package.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.

Table 16. Pinout Listing for the MPC7447, 360 CBGA Package

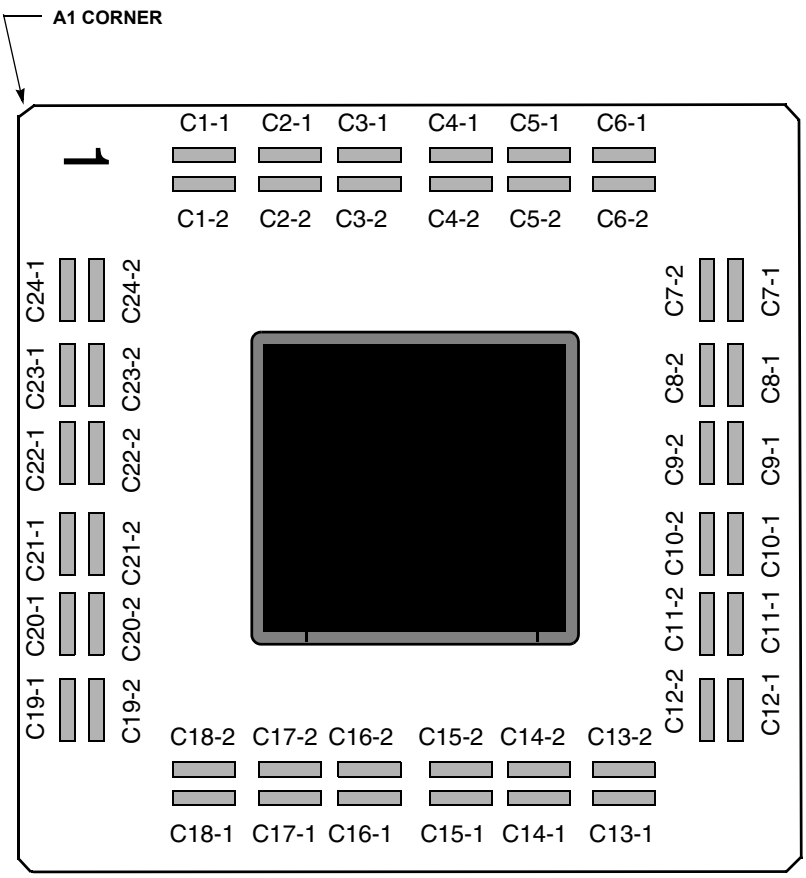
Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	BVSEL	2
$\overline{\text{AACK}}$	R1	Low	Input	BVSEL	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	BVSEL	
$\overline{\text{ARTRY}}$	N2	Low	I/O	BVSEL	3
AV_{DD}	A8	—	Input	N/A	
$\overline{\text{BG}}$	M1	Low	Input	BVSEL	
$\overline{\text{BMODE0}}$	G9	Low	Input	BVSEL	4
$\overline{\text{BMODE1}}$	F8	Low	Input	BVSEL	5
$\overline{\text{BR}}$	D2	Low	Output	BVSEL	
BVSEL	B7	High	Input	BVSEL	1, 6
$\overline{\text{CI}}$	J1	Low	Output	BVSEL	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	BVSEL	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	BVSEL	
CLK_OUT	H2	High	Output	BVSEL	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	BVSEL	
$\overline{\text{DBG}}$	M2	Low	Input	BVSEL	
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	BVSEL	
$\overline{\text{DRDY}}$	R3	Low	Output	BVSEL	7
DTI[0:3]	G1, K1, P1, N1	High	Input	BVSEL	8
EXT_QUAL	A11	High	Input	BVSEL	9
$\overline{\text{GBL}}$	E2	Low	I/O	BVSEL	

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
L1_TSTCLK	H4	High	Input	BVSEL	10
L2_TSTCLK	J2	High	Input	BVSEL	12
L3VSEL	A4	High	Input	N/A	6, 7
L3ADDR[18:0]	H11, F20, J16, E22, H18, G20, F22, G22, H20, K16, J18, H22, J20, J22, K18, K20, L16, K22, L18	High	Output	L3VSEL	
L3_CLK[0:1]	V22, C17	High	Output	L3VSEL	
$\overline{\text{L3\_CNTL}}$[0:1]	L20, L22	Low	Output	L3VSEL	
L3DATA[0:63]	AA19, AB20, U16, W18, AA20, AB21, AA21, T16, W20, U18, Y22, R16, V20, W22, T18, U20, N18, N20, N16, N22, M16, M18, M20, M22, R18, T20, U22, T22, R20, P18, R22, M15, G18, D22, E20, H16, C22, F18, D20, B22, G16, A21, G15, E17, A20, C19, C18, A19, A18, G14, E15, C16, A17, A16, C15, G13, C14, A14, E13, C13, G12, A13, E12, C12	High	I/O	L3VSEL	
L3DP[0:7]	AB19, AA22, P22, P16, C20, E16, A15, A12	High	I/O	L3VSEL	
L3_ECHO_CLK[0,2]	V18, E18	High	Input	L3VSEL	
L3_ECHO_CLK[1,3]	P20, E14	HIgh	I/O	L3VSEL	
$\overline{\text{LSSD\_MODE}}$	F6	Low	Input	BVSEL	7, 13
$\overline{\text{MCP}}$	B8	Low	Input	BVSEL	
No Connect	A8, A11, B6, B11, C11, D11, D3, D5, E11, E7, F2, F11, G2, H9	—	—	N/A	14
OV_{DD}	B3, C5, C7, C10, D2, E3, E9, F5, G3, G9, H7, J5, K3, L7, M5, N3, P7, R4, T3, U5, U7, U11, U15, V3, V9, V13, Y2, Y5, Y7, Y10, Y17, Y19, AA4, AA15	—	—	N/A	
PLL_CFG[0:4]	A2, F7, C2, D4, H8	High	Input	BVSEL	
$\overline{\text{PMON\_IN}}$	E6	Low	Input	BVSEL	15
$\overline{\text{PMON\_OUT}}$	B4	Low	Output	BVSEL	
$\overline{\text{QACK}}$	K7	Low	Input	BVSEL	
$\overline{\text{QREQ}}$	Y1	Low	Output	BVSEL	
$\overline{\text{SHD}}$[0:1]	L4, L8	Low	I/O	BVSEL	3
$\overline{\text{SMI}}$	G8	Low	Input	BVSEL	
$\overline{\text{SRESET}}$	G1	Low	Input	BVSEL	
SYSCLK	D6	—	Input	BVSEL	
$\overline{\text{TA}}$	N8	Low	Input	BVSEL	
TBEN	L3	High	Input	BVSEL	
$\overline{\text{TBST}}$	B7	Low	Output	BVSEL	
TCK	J7	High	Input	BVSEL	

8.6 Substrate Capacitors for the MPC7457, 483 CBGA or RoHS BGA

Figure 23 shows the connectivity of the substrate capacitor pads for the MPC7457, 483 CBGA or RoHS BGA. All capacitors are 100 nF.



Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

Figure 23. Substrate Bypass Capacitors for the MPC7457, 483 CBGA or RoHS BGA

9.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7457 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 24 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 CBGA footprint and very close to the periphery of the 483 CBGA footprint, without the inductance of vias.

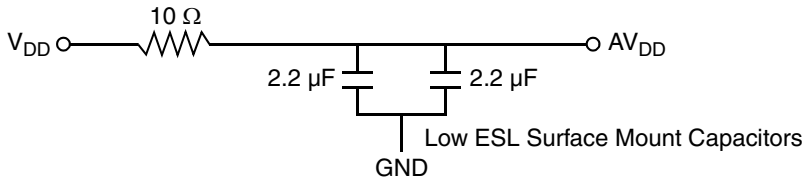


Figure 24. PLL Power Supply Filter Circuit

NOTE

All production 7447 and 7457 Rev. B devices require a 400 Ω resistor instead of the 10 Ω resistor shown above. All production 7457 Rev. C devices require a 10 Ω resistor. For more information, see the *MPC7450 Family Chip Errata for the MPC7457 and MPC7447*.

9.3 Decoupling Recommendations

Due to the MPC7457 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7457 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7457 system, and the MPC7457 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pin of the MPC7457. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}/GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. If compromises must be made due to board constraints, V_{DD} pins should receive the highest priority for decoupling.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, GV_{DD}, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L3 interface does not normally require pull-up resistors. Unused L3_ADDR signals are driven low when the SRAM is configured to be less than 1 M in size via L3CR. For example, L3_ADD[18] will be driven low if the SRAM size is configured to be 2 M; likewise, L3_ADDR[18:17] will be driven low if the SRAM size is configured to be 1 M.

9.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 26, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 26 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 26; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 26 is usually connected to the PCI bridge chip in a system and is an input to the MPC7457 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7457 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5°C/W. For

example, assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 18.7\ W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the MPC7447 and MPC7457 thermal model is shown in Figure 30. Four volumes will be used to represent this device. Two of the volumes, solder ball, and air and substrate, are modeled using the package outline size of the package. The other two, die, and bump and underfill, have the same size as the die. The silicon die should be modeled 9.64 × 11.0 × 0.74 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 9.64 × 11.0 × 0.069 mm (or as a collapsed volume) with orthotropic material properties: 0.6 W/(m • K) in the xy-plane and 2 W/(m • K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm (MPC7447) or 29 × 29 × 1.2 mm (MPC7457), and this volume has 18 W/(m • K) isotropic conductivity. The solder ball and air layer is modeled with the same horizontal dimensions as the substrate and is 0.9 mm thick. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 3.8 W/(m • K) in the direction of the z-axis.

Table 24. Part Numbers Addressed by MPC7457TRX*nnnn*LB Series Hardware Specifications Addendum (Document Order No. MPC7457ECS02AD)

MC	7457	T	RX	*nnnn*	L	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7457	T = Extended Temperature Device	RX = CBGA	1000 1267	L: 1.3 V ± 50 mV –40° to 105°C	C: 1.2; PVR = 8002 0102

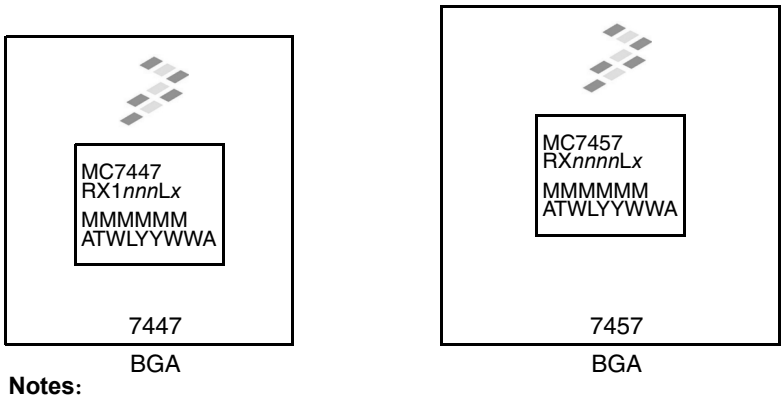
Table 25. Part Numbers Addressed by MPC7457TRX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS03AD)

MC	74*x*7	T	RX	*nnnn*	N	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7447	T = Extended Temperature Device	RX = CBGA	733 1000	N: 1.1 V ± 50 mV –40° to 105°C	B: 1.1; PVR = 8002 0101
	7457					C: 1.2; PVR = 8002 0102

10.3 Part Marking

Parts are marked as the examples shown in Figure 31.



Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.

Figure 31. Part Marking for BGA Device

11 Document Revision History

Table 26 provides a revision history for this hardware specification.

Table 26. Document Revision History

Revision Number	Date	Substantive Change(s)
8	04/09/2013	Updated template. Updated Table 14 “L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs”. Moved Revision History to the end of the document.
7	3/28/2006	Updated template. Section 2, reworded L1 and L2 cache descriptions. Removed note references for $\overline{CI}$ and $\overline{WT}$ in Table 12. Added VG package signifier for 7457 only.
6	7/22/2005	Revised Note in Section 9.2.
		Added heat sink vendor to list in Section 9.8.
		Corrected bump and underfill model dimension in Section 9.8.3.
5	9/9/2004	Updated document to new Freescale template.
		Updated section numbering and changed reference from part number specifications to addendums.
		Added Rev. 1.2 devices, including increased L3 clock max frequency to 250 MHz and improved L3 AC timing.
		Table 5: Added CTE information.
		Table 8: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Table 13: Deleted note 9 and renumbered.
		Table 14: Deleted note 5 and renumbered.
		Table 17: Revised note 6.
		Added Section 9.1.3.
		Section 9.2: Changed filter resistor recommendations. Recommend 10 Ω resistor for all production devices, including production Rev. 1.1 devices. 400 Ω resistor needed only for early Rev. 1.1 devices.
		Table 22: Reversed the order of revision numbers.
		Added Tables 25 and 26.
4.1		Section 9.1.1: Corrected note regarding different PLL configurations for earlier devices; all MPC7457 devices to date conform to this table.
		Section 9.6: Added information about unused L3_ADDR signals.
		Table 24: Changed title to include document order information for MPC74x7RXnnnnNx series part number specification.