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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	867MHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc7457rx867nc

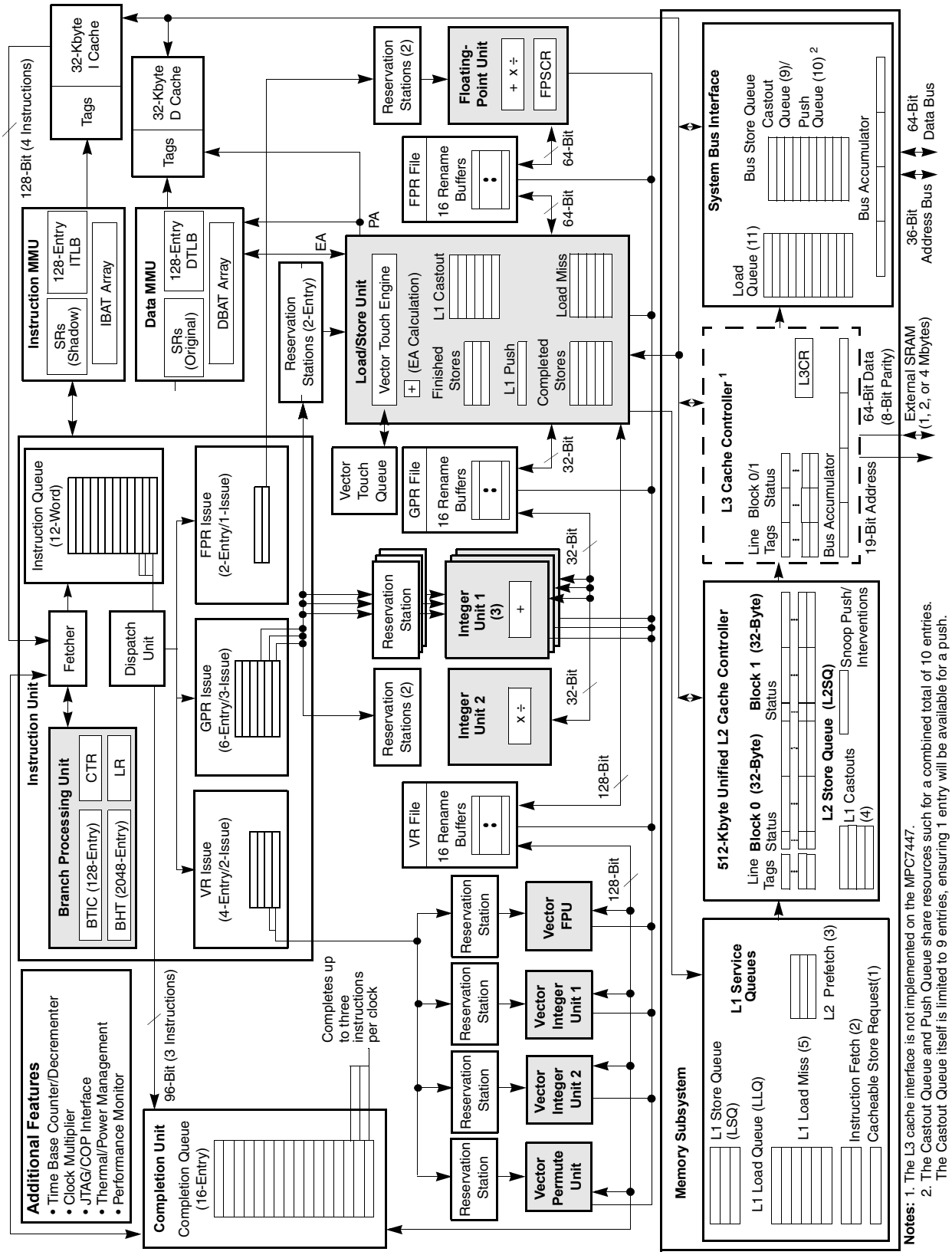


Figure 1. MPC7457 Block Diagram

- Four integer units (IUs) that share 32 GPRs for integer operands
  - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions
  - IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions
- Five-stage FPU and a 32-entry FPR file
  - Fully IEEE 754-1985 compliant FPU for both single- and double-precision operations
  - Supports non-IEEE mode for time-critical operations
  - Hardware support for denormalized numbers
  - Thirty-two 64-bit FPRs for single- or double-precision operands
- Four vector units and 32-entry vector register file (VRs)
  - Vector permute unit (VPU)
  - Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**)
  - Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**)
  - Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half-word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - Dedicated adder calculates effective addresses (EAs)
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues FIQ, VIQ, and GIQ can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can be dispatched only from the three lowest IQ entries—IQ0, IQ1, and IQ2
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle

3 Comparison with the MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441

Table 1 compares the key features of the MPC7457 with the key features of the earlier MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441. To achieve a higher frequency, the number of logic levels per cycle is reduced. Also, to achieve this higher frequency, the pipeline of the MPC7457 is extended (compared to the MPC7400), while maintaining the same level of performance as measured by the number of instructions executed per cycle (IPC).

Table 1. Microarchitecture Comparison

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Basic Pipeline Functions			
Logic inversions per cycle	18	18	18
Pipeline stages up to execute	5	5	5
Total pipeline stages (minimum)	7	7	7
Pipeline maximum instruction throughput	3 + Branch	3 + Branch	3 + Branch
Pipeline Resources			
Instruction buffer size	12	12	12
Completion buffer size	16	16	16
Renames (integer, float, vector)	16, 16, 16	16, 16, 16	16, 16, 16
Maximum Execution Throughput			
SFX	3	3	3
Vector	2 (any 2 of 4 units)	2 (any 2 of 4 units)	2 (any 2 of 4 units)
Scalar floating-point	1	1	1
Out-of-Order Window Size in Execution Queues			
SFX integer units	1 entry × 3 queues	1 entry × 3 queues	1 entry × 3 queues
Vector units	In order, 4 queues	In order, 4 queues	In order, 4 queues
Scalar floating-point unit	In order	In order	In order
Branch Processing Resources			
Prediction structures	BTIC, BHT, link stack	BTIC, BHT, link stack	BTIC, BHT, link stack
BTIC size, associativity	128-entry, 4-way	128-entry, 4-way	128-entry, 4-way
BHT size	2K-entry	2K-entry	2K-entry
Link stack depth	8	8	8
Unresolved branches supported	3	3	3
Branch taken penalty (BTIC hit)	1	1	1

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Minimum misprediction penalty	6	6	6
Execution Unit Timings (Latency-Throughput)			
Aligned load (integer, float, vector)	3-1, 4-1, 3-1	3-1, 4-1, 3-1	3-1, 4-1, 3-1
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2	4-2, 5-2, 4-2	4-2, 5-2, 4-2
L1 miss, L2 hit latency	9 data/13 instruction	9 data/13 instruction	9 data/13 instruction
SFX (aDd Sub, Shift, Rot, Cmp, logicals)	1-1	1-1	1-1
Integer multiply (32 × 8, 32 × 16, 32 × 32)	3-1, 3-1, 4-2	3-1, 3-1, 4-2	3-1, 3-1, 4-2
Scalar float	5-1	5-1	5-1
VSFX (vector simple)	1-1	1-1	1-1
VCFX (vector complex)	4-1	4-1	4-1
VFPU (vector float)	4-1	4-1	4-1
VPER (vector permute)	2-1	2-1	2-1
MMUs			
TLBs (instruction and data)	128-entry, 2-way	128-entry, 2-way	128-entry, 2-way
Tablewalk mechanism	Hardware + software	Hardware + software	Hardware + software
Instruction BATs/data BATs	8/8	8/8	4/4
L1 I Cache/D Cache Features			
Size	32K/32K	32K/32K	32K/32K
Associativity	8-way	8-way	8-way
Locking granularity	Way	Way	Way
Parity on I cache	Word	Word	Word
Parity on D cache	Byte	Byte	Byte
Number of D cache misses (load/store)	5/1	5/1	5/1
Data stream touch engines	4 streams	4 streams	4 streams
On-Chip Cache Features			
Cache level	L2	L2	L2
Size/associativity	512-Kbyte/8-way	256-Kbyte/8-way	256-Kbyte/8-way
Access width	256 bits	256 bits	256 bits
Number of 32-byte sectors/line	2	2	2
Parity	Byte	Byte	Byte
Off-Chip Cache Support [1]			

5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7457. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 1.5.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency; see Section 1.11, "Ordering Information."

5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 6 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 8 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the MPC7457 will be a function of the AC timings of the MPC7457, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8. For information regarding the use of spread spectrum clock generators, see Section 9.1.3, "System Bus Clock (SYSCLK) and Spread Spectrum Sources." PLL configuration and bus-to-core multiplier information is found in Section 9.1.1, "Core Clocks and PLL Configuration."

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		867 MHz		1000 MHz		1200 MHz		1267 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	600	867	600	1000	600	1200	600	1267	MHz	1
VCO frequency	f_{VCO}	1200	1733	1200	2000	1200	2400	1200	2534	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	167	33	167	33	167	33	167	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	6.0	30	6.0	30	6.0	30	6.0	30	ns	2
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	1.0	—	1.0	—	1.0	—	1.0	ns	3
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter		—	150	—	150	—	150	—	150	ps	5, 6

Table 13. L3 Bus Interface AC Timing Specifications for MSUG2 (continued)

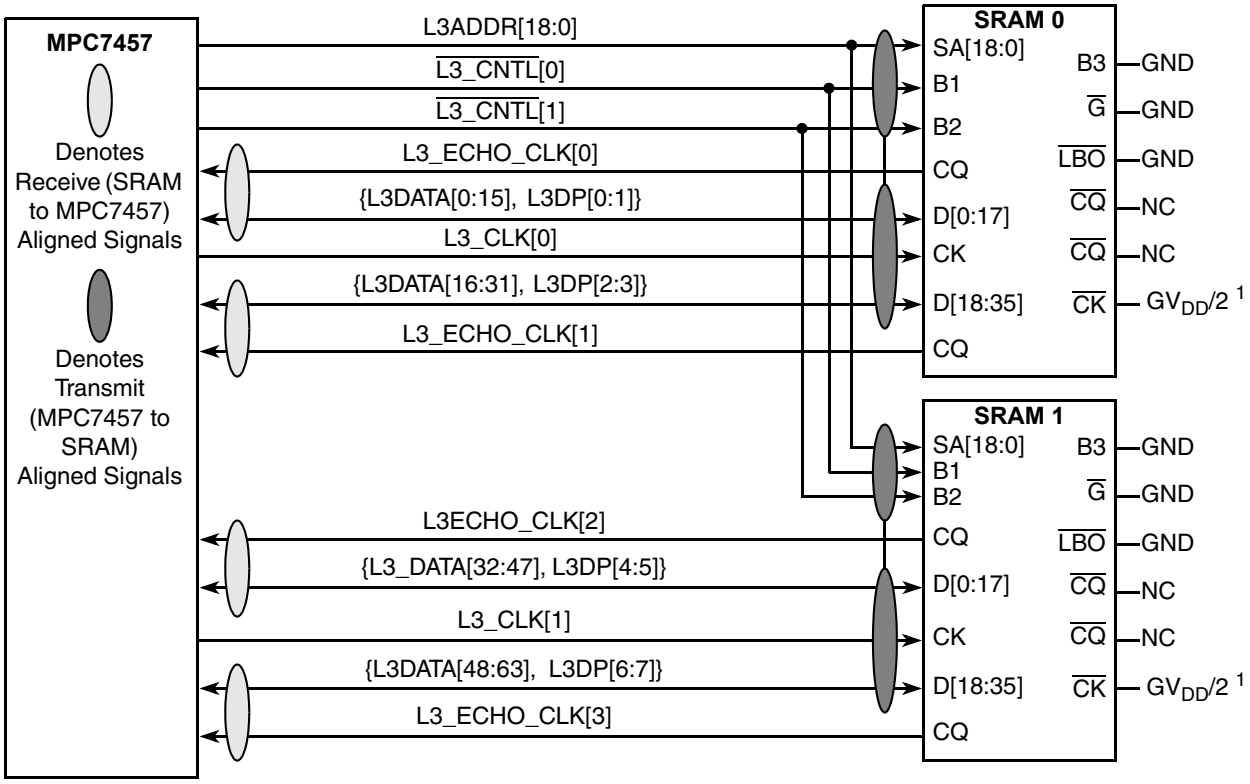
At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [9]				Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)		Rev 1.2 (1.8-, 2.5-V I/O Modes)			
		Min	Max	Min	Max		
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	(t_{L3CLK}/4) + 0.65	—	(t_{L3CLK}/4) + 0.65	ns	

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. For DDR, all input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising or falling edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
3. For DDR, the input data will typically follow the edge of L3_ECHO_CLK*n* as shown in Figure 10. For consistency with other input setup time specifications, this will be treated as negative input setup time.
4. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the MPC7457 can latch an input signal that is valid for only a short time before and a short time after the midpoint between the rising and falling (or falling and rising) edges of L3_ECHO_CLK*n* at any frequency.
5. All output specifications are measured from the midpoint voltage of the rising (or for DDR write data, also the falling) edge of L3_CLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 8).
6. For DDR, the output data will typically lead the edge of L3_CLK*n* as shown in Figure 10. For consistency with other output valid time specifications, this will be treated as negative output valid time.
7. t_{L3_CLK}/4 is one-fourth the period of L3_CLK*n*. This parameter indicates that the specified output signal is actually launched by an internal clock delayed in phase by 90°. Therefore, there is a frequency component to the output valid and output hold times such that the specified output signal will be valid for approximately one L3_CLK period starting three-fourths of a clock before the edge on which the SRAM will sample it and ending one-fourth of a clock period after the edge it will be sampled.
8. Assumes default value of L3OHCR. See Section 5.2.4.1, “Effects of L3OHCR Settings on L3 Bus AC Specifications,” for more information.
9. L3 I/O voltage mode must be configured by L3VSEL as described in Table 3, and voltage supplied at GV_{DD} must match mode selected as specified in Table 4. See Table 22 for revision level information and part marking.

Figure 9 shows the typical connection diagram for the MPC7457 interfaced to MSUG2 DDR SRAMs.



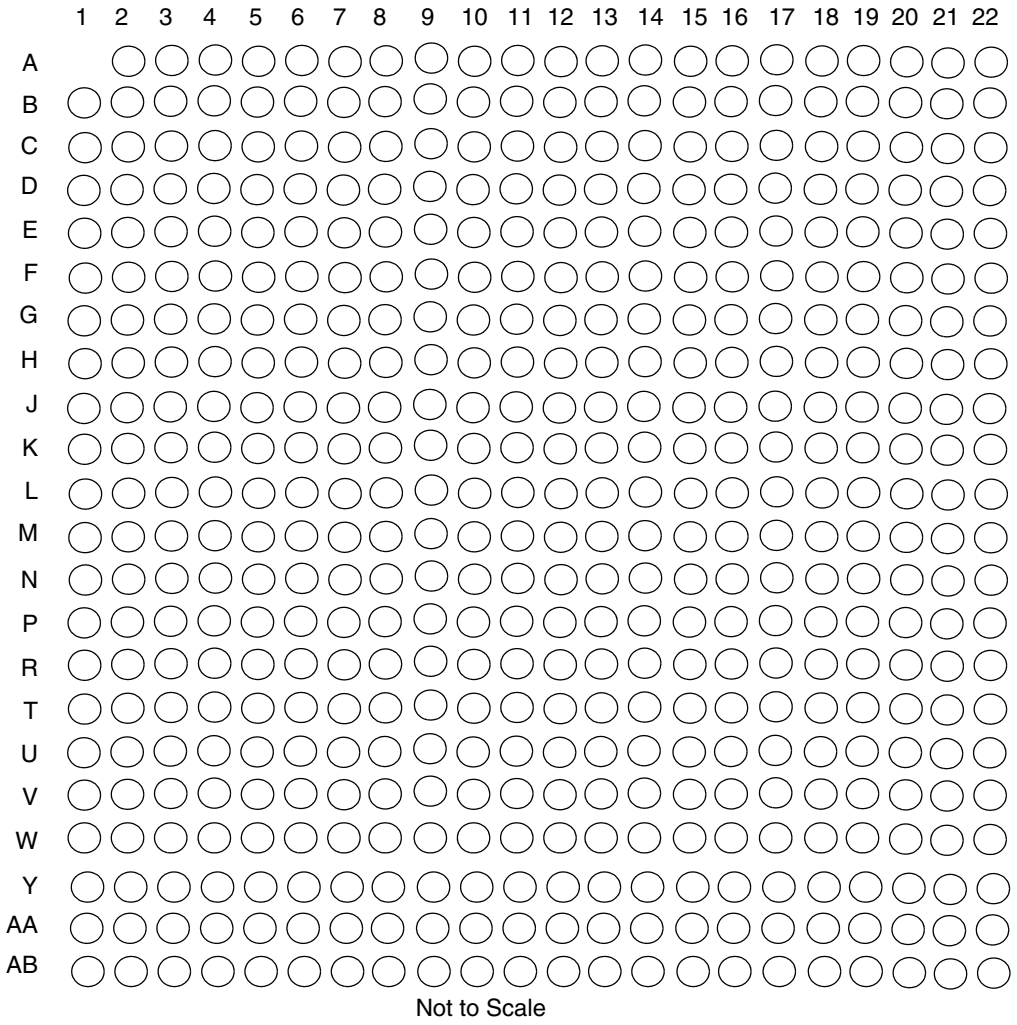
Note:

1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 9. Typical Source Synchronous 4-Mbyte L3 Cache DDR Interface

Figure 19 (Part A) shows the pinout of the MPC7457, 483 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

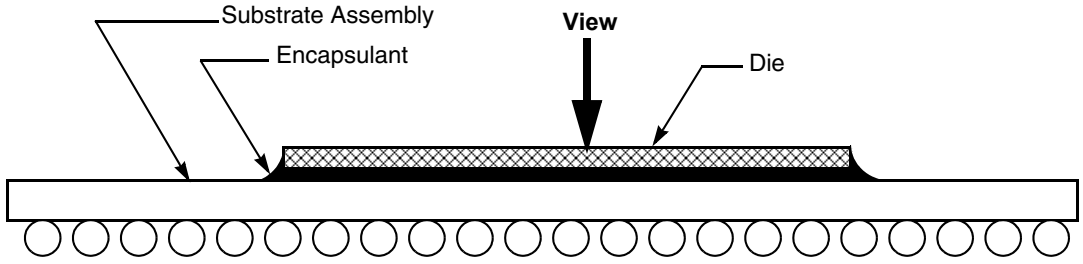


Figure 19. Pinout of the MPC7457, 483 CBGA Package as Viewed from the Top Surface

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
AV_{DD}	B2	—	Input	N/A	
$\overline{BG}$	R3	Low	Input	BVSEL	
$\overline{BMODE0}$	C6	Low	Input	BVSEL	4
$\overline{BMODE1}$	C4	Low	Input	BVSEL	5
$\overline{BR}$	K1	Low	Output	BVSEL	
BVSEL	G6	High	Input	N/A	6, 7
$\overline{CI}$	R1	Low	Output	BVSEL	
$\overline{CKSTP\_IN}$	F3	Low	Input	BVSEL	
$\overline{CKSTP\_OUT}$	K6	Low	Output	BVSEL	
CLK_OUT	N1	High	Output	BVSEL	
D[0:63]	AB15, T14, R14, AB13, V14, U14, AB14, W16, AA11, Y11, U12, W13, Y14, U13, T12, W12, AB12, R12, AA13, AB11, Y12, V11, T11, R11, W10, T10, W11, V10, R10, U10, AA10, U9, V7, T8, AB4, Y6, AB7, AA6, Y8, AA7, W8, AB10, AA16, AB16, AB17, Y18, AB18, Y16, AA18, W14, R13, W15, AA14, V16, W6, AA12, V6, AB9, AB6, R7, R9, AA9, AB8, W9	High	I/O	BVSEL	
$\overline{DBG}$	V1	Low	Input	BVSEL	
DP[0:7]	AA2, AB3, AB2, AA8, R8, W5, U8, AB5	High	I/O	BVSEL	
$\overline{DRDY}$	T6	Low	Output	BVSEL	8
DTI[0:3])	P2, T5, U3, P6	High	Input	BVSEL	9
EXT_QUAL	B9	High	Input	BVSEL	10
$\overline{GBL}$	M4	Low	I/O	BVSEL	
GND	A22, B1, B5, B12, B14, B16, B18, B20, C3, C9, C21, D7, D13, D15, D17, D19, E2, E5, E21, F10, F12, F14, F16, F19, G4, G7, G17, G21, H13, H15, H19, H5, J3, J10, J12, J14, J17, J21, K5, K9, K11, K13, K15, K19, L10, L12, L14, L17, L21, M3, M6, M9, M11, M13, M19, N10, N12, N14, N17, N21, P3, P9, P11, P13, P15, P19, R17, R21, T13, T15, T19, T4, T7, T9, U17, U21, V2, V5, V8, V12, V15, V19, W7, W17, W21, Y3, Y9, Y13, Y15, Y20, AA5, AA17, AB1, AB22	—	—	N/A	
GV_{DD}	B13, B15, B17, B19, B21, D12, D14, D16, D18, D21, E19, F13, F15, F17, F21, G19, H12, H14, H17, H21, J19, K17, K21, L19, M17, M21, N19, P17, P21, R15, R19, T17, T21, U19, V17, V21, W19, Y21	—	—	N/A	11
$\overline{HIT}$	K2	Low	Output	BVSEL	8
$\overline{HRESET}$	A3	Low	Input	BVSEL	
$\overline{INT}$	J6	Low	Input	BVSEL	

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

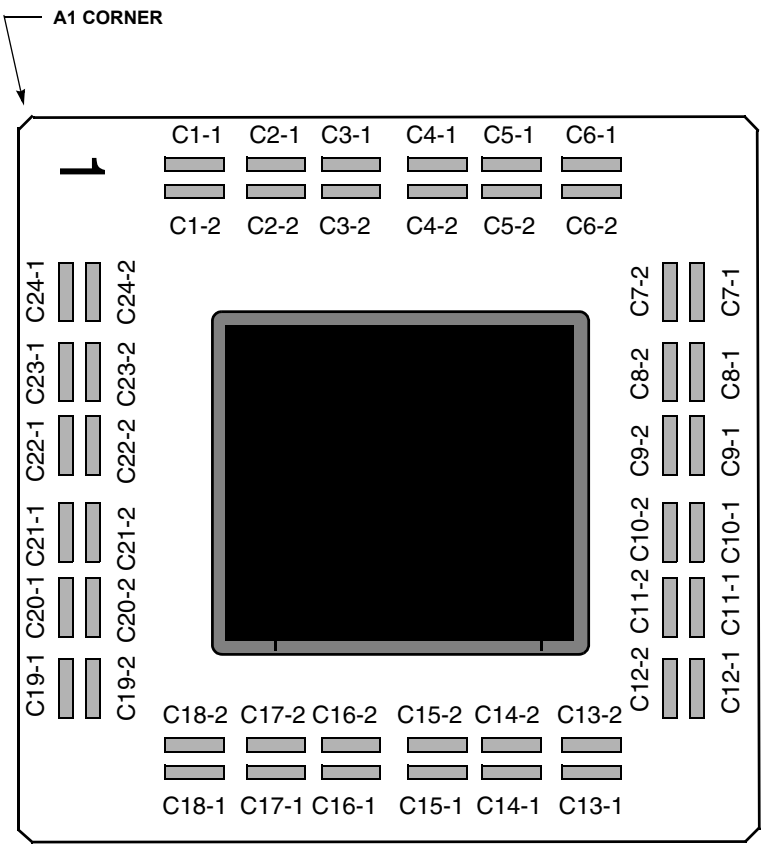
Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
TDI	E4	High	Input	BVSEL	7
TDO	H1	High	Output	BVSEL	
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL	
TEST[0:5]	B10, H6, H10, D8, F9, F8	—	Input	BVSEL	13
TEST[6]	A9	—	Input	BVSEL	10
TMS	K4	High	Input	BVSEL	7
$\overline{\text{TRST}}$	C1	Low	Input	BVSEL	7, 16
$\overline{\text{TS}}$	P5	Low	I/O	BVSEL	3
TSIZ[0:2]	L1,H3,D1	High	Output	BVSEL	
TT[0:4]	F1, F4, K8, A5, E1	High	I/O	BVSEL	
$\overline{\text{WT}}$	L2	Low	Output	BVSEL	
V_{DD}	J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14	—	—	N/A	
VDD_SENSE[0:1]	G11, J8	—	—	N/A	17

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); GV_{DD} supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals $\overline{\text{L3\_CNTL}}$[0:1]; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). For actual recommended value of V_{in} or supply voltages, see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. See Table 3 for bus voltage configuration information. If used, pull-down resistors should be less than 250 Ω.
7. Internal pull up on die.
8. Ignored in 60x bus mode.
9. These signals must be pulled down to GND if unused or if the MPC7457 is in 60x bus mode.
10. These input signals for factory use only and must be pulled down to GND for normal machine operation.
11. Power must be supplied to GV_{DD}, even when the L3 interface is disabled or unused.
12. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
14. These signals are for factory use only and must be left unconnected for normal machine operation.
15. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
16. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
17. These pins are internally connected to V_{DD}. They are intended to allow an external device to detect the core voltage level present at the processor core. If unused, they must be connected directly to V_{DD} or left unconnected.

8.3 Substrate Capacitors for the MPC7447, 360 CBGA

Figure 21 shows the connectivity of the substrate capacitor pads for the MPC7447, 360 CBGA. All capacitors are 100 nF.

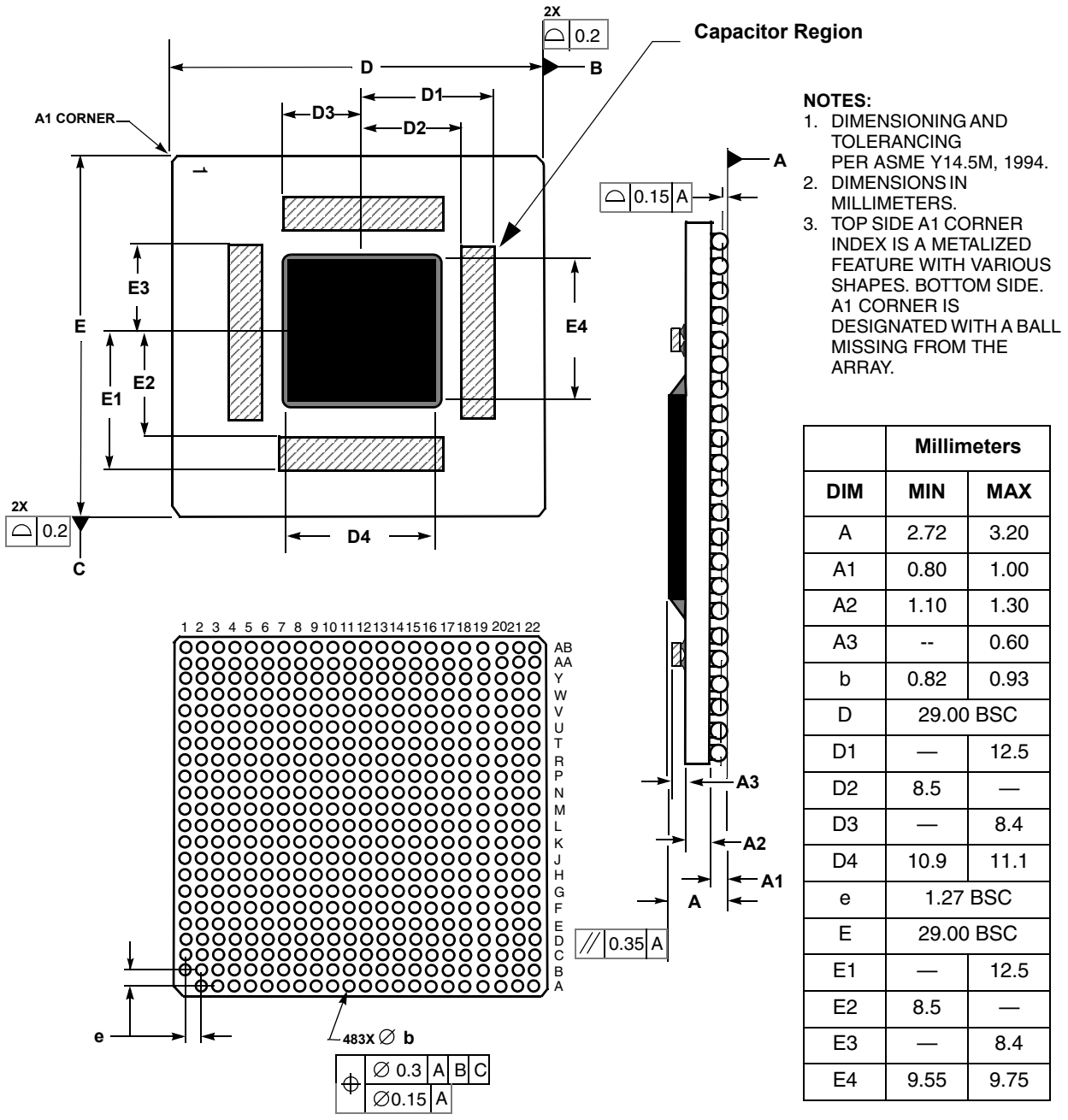


Capacitor	Pad Number	
	-1	-2
C1	GND	V_{DD}
C2	GND	V_{DD}
C3	GND	OV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	V_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	OV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	V_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

Figure 21. Substrate Bypass Capacitors for the MPC7447, 360 CBGA

8.5 Mechanical Dimensions for the MPC7457, 483 CBGA or RoHS BGA

Figure 22 provides the mechanical dimensions and bottom surface nomenclature for the MPC7457, 483 CBGA package.



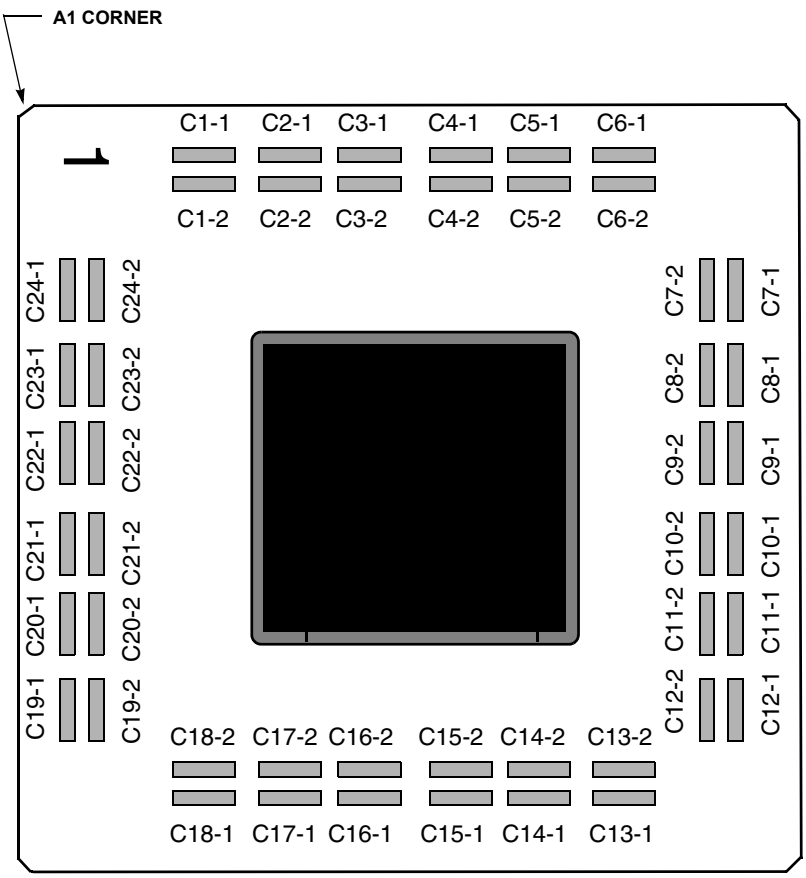
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE. A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1.00
A2	1.10	1.30
A3	--	0.60
b	0.82	0.93
D	29.00 BSC	
D1	—	12.5
D2	8.5	—
D3	—	8.4
D4	10.9	11.1
e	1.27 BSC	
E	29.00 BSC	
E1	—	12.5
E2	8.5	—
E3	—	8.4
E4	9.55	9.75

Figure 22. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7457, 483 CBGA or RoHS BGA Package

8.6 Substrate Capacitors for the MPC7457, 483 CBGA or RoHS BGA

Figure 23 shows the connectivity of the substrate capacitor pads for the MPC7457, 483 CBGA or RoHS BGA. All capacitors are 100 nF.



Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

Figure 23. Substrate Bypass Capacitors for the MPC7457, 483 CBGA or RoHS BGA

Table 18. MPC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts (continued)

PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
01111	9x	2x			600 (1200)	675 (1350)	747 (1494)	900 (1800)	1197 (2394)	
01110	9.5x	2x			633 (1266)	712 (1524)	789 (1578)	950 (1900)	1264 (2528)	
10101	10x	2x			667 (1333)	750 (1500)	830 (1660)	1000 (2000)		
10001	10.5x	2x			700 (1400)	938 (1876)	872 (1744)	1050 (2100)		
10011	11x	2x			733 (1466)	825 (1650)	913 (1826)	1100 (2200)		
00000	11.5x	2x			766 (532)	863 (1726)	955 (1910)	1150 (2300)		
10111	12x	2x		600 (1200)	800 (1600)	900 (1800)	996 (1992)	1200 (2400)		
11111	12.5x	2x		600 (1200)	833 (1666)	938 (1876)	1038 (2076)	1250 (2500)		
01011	13x	2x		650 (1300)	865 (1730)	975 (1950)	1079 (2158)			
11100	13.5x	2x		675 (1350)	900 (1800)	1013 (2026)	1121 (2242)			
11001	14x	2x		700 (1400)	933 (1866)	1050 (2100)	1162 (2324)			
00011	15x	2x		750 (1500)	1000 (2000)	1125 (2250)	1245 (2490)			
11011	16x	2x		800 (1600)	1066 (2132)	1200 (2400)				
00001	17x	2x		850 (1900)	1132 (2264)					
00101	18x	2x	600 (1200)	900 (1800)	1200 (2400)					
00111	20x	2x	667 (1334)	1000 (2000)						
01001	21x	2x	700 (1400)	1050 (2100)						
01101	24x	2x	800 (1600)	1200 (2400)						
11101	28x	2x	933 (1866)							
00110	PLL bypass		PLL off, SYSCLK clocks core circuitry directly							

Table 18. MPC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts (continued)

PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
11110	PLL off		PLL off, no core clocking occurs							

Notes:
1. PLL_CFG[0:4] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7455; see Section 5.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result is that the processor bus frequency is one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7455 regardless of the SYSCLK input.

9.1.2 L3 Clocks

The MPC7457 generates the clock for the external L3 synchronous data SRAMs by dividing the core clock frequency of the MPC7457. The core-to-L3 frequency divisor for the L3 PLL is selected through the L3_CLK bits of the L3CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC7457 core, and timing analysis of the circuit board routing. Table 19 shows various example L3 clock frequencies that can be obtained for a given set of core frequencies.

Table 19. Sample Core-to-L3 Frequencies [1]

Core Frequency (MHz) [2]	÷2	÷2.5	÷3	÷3.5	÷4	÷4.5	÷5	÷5.5	÷6	÷6.5	÷7	÷7.5	÷8
500	250	200	167	143	125	111	100	91	83	77	71	67	63
533	266	213	178	152	133	118	107	97	89	82	76	71	67
550	275	220	183	157	138	122	110	100	92	85	79	73	69
600	300	240	200	171	150	133	120	109	100	92	86	80	75
650	325	260	217	186	163	144	130	118	108	100	93	87	81
666	333	266	222	190	167	148	133	121	111	102	95	89	83
700	350	280	233	200	175	156	140	127	117	108	100	93	88
733	367	293	244	209	183	163	147	133	122	113	105	98	92
800	400	320	266	230	200	178	160	145	133	123	114	107	100
866	433	347	289	248	217	192	173	157	145	133	124	115	108
933	467	373	311	266	233	207	187	170	156	144	133	124	117
1000	500	400	333	285	250	222	200	182	166	154	143	133	125

Table 19. Sample Core-to-L3 Frequencies [1] (continued)

Core Frequency (MHz) [2]	÷2	÷2.5	÷3	÷3.5	÷4	÷4.5	÷5	÷5.5	÷6	÷6.5	÷7	÷7.5	÷8
1050	525	420	350	300	263	233	191	191	175	162	150	140	131
1100	550	440	367	314	275	244	200	200	183	169	157	147	138
1150	575	460	383	329	288	256	209	209	192	177	164	153	144
1200	600	480	400	343	300	267	218	218	200	185	171	160	150
1250	638	500	417	357	313	278	227	227	208	192	179	167	156
1300	650	520	433	371	325	289	236	236	217	200	186	173	163

Notes:
1. The core and L3 frequencies are for reference only. Note that maximum L3 frequency is design dependent. Some examples may represent core or L3 frequencies which are not useful, not supported, or not tested for the MPC7457; see Section 5.2.3, "L3 Clock AC Specifications," for valid L3_CLK frequencies and for more information regarding the maximum L3 frequency.
2. Not all core frequencies are supported by all speed grades; see Table 8 for minimum and maximum core frequency specifications.

9.1.3 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC7457 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7457 is compatible with spread spectrum sources if the recommendations listed in Table 20 are observed.

Table 20. Spread Specturm Clock Source Recommendations

At recommended operating conditions. See Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

Table 21. Impedance Characteristics
V_{DD} = 1.5 V, OV_{DD} = 1.8 V ± 5%, T_j = 5°–85°C

Impedance		Processor Bus	L3 Bus	Unit
Z_0	Typical	33–42	34–42	Ω
	Maximum	31–51	32–44	Ω

9.6 Pull-Up/Pull-Down Resistor Requirements

The MPC7457 requires high-resistive (weak: 4.7-kΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being for factory test must be pulled up to OV_{DD} or down to GND to ensure proper device operation. For the MPC7447, 360 BGA, the pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. For the MPC7457, 483 BGA, the pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:5]; the pins that must be pulled down are: L1_TSTCLK and TEST[6]. The $\overline{\text{CKSTP\_IN}}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 kΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7457 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 kΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

If pull-down resistors are used to configure BVSEL or L3VSEL, the resistors should be less than 250 Ω (see Table 16). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7457 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7457 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information about this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7457 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If extended addressing is not used, A[0:3] are unused and must be pulled low to GND through weak pull-down resistors. If the MPC7457 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].

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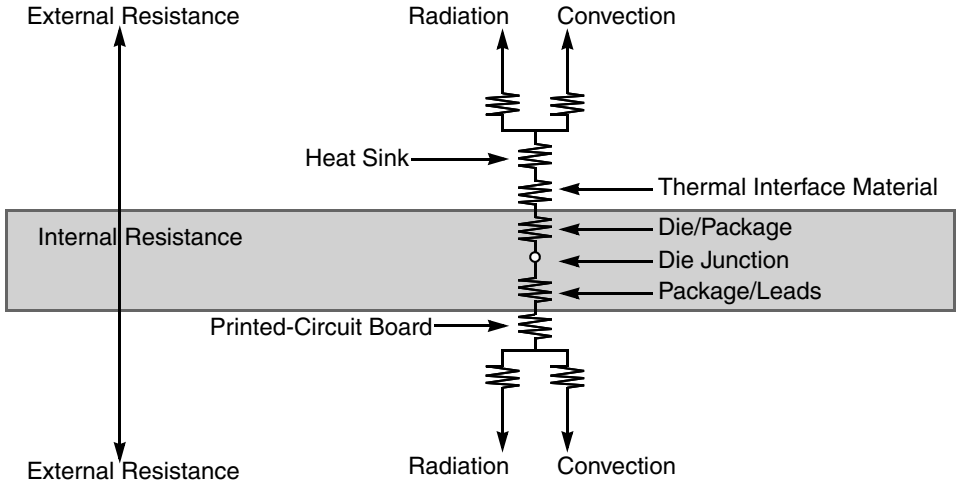
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

9.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (actually top-of-die since silicon die is exposed) thermal resistance
- The die junction-to-ball thermal resistance

Figure 28 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance.)

Figure 28. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

Table 22. Part Numbering Nomenclature

MC	74*x*7	*xx*	*nnnn*	L	*x*

Product Code	Part Identifier	Package	Processor Frequency [1]	Application Modifier	Revision Level
PPC [2] MC	7457 7447	RX = CBGA	867 1000 1200 1267	L: 1.3 V ± 50 mV 0° to 105°C	B: 1.1; PVR = 8002 0101
MC	7457	RX = CBGA VG = RoHS BGA	867 1000 1200 1267		C: 1.2; PVR = 8002 0102

Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by a hardware specification addendum may support other maximum core frequencies.
2. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

10.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed are described in a separate addendum, which supplement and supersede this hardware specification. As such parts are released, these specifications will be listed in this section.

Table 23. Part Numbers Addressed by MPC74x7RX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS01AD)

MC	74*x*7	*xx*	*nnnn*	N	*x*

Product Code	Part Identifier	Package	Processor Frequency	Application Modifier	Revision Level
PPC	7457	RX = CBGA	1000 867 733 600	N: 1.1 V ± 50 mV 0° to 105°C	B: 1.1; PVR = 8002 0101
	7447		1000 867		
MC	7447		1000 867 733 600		B: 1.1; PVR = 8002 0101
	7457	RX = CBGA VG = RoHS BGA	1000 867 733 600		C: 1.2; PVR = 8002 0102

Table 24. Part Numbers Addressed by MPC7457TRX*nnnn*LB Series Hardware Specifications Addendum (Document Order No. MPC7457ECS02AD)

MC	7457	T	RX	*nnnn*	L	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7457	T = Extended Temperature Device	RX = CBGA	1000 1267	L: 1.3 V ± 50 mV –40° to 105°C	C: 1.2; PVR = 8002 0102

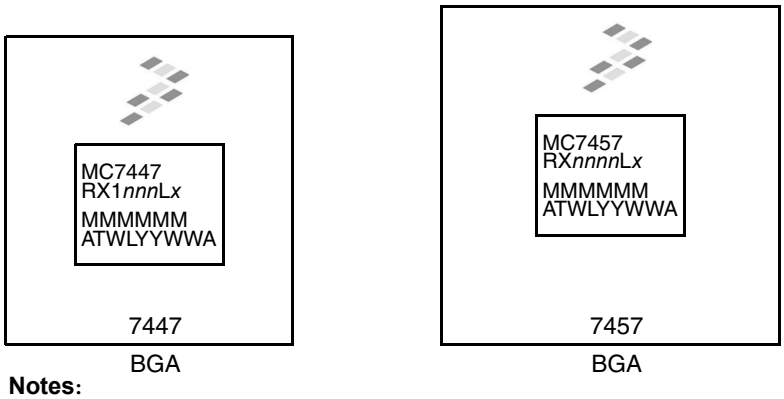
Table 25. Part Numbers Addressed by MPC7457TRX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS03AD)

MC	74*x*7	T	RX	*nnnn*	N	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7447	T = Extended Temperature Device	RX = CBGA	733 1000	N: 1.1 V ± 50 mV –40° to 105°C	B: 1.1; PVR = 8002 0101
	7457					C: 1.2; PVR = 8002 0102

10.3 Part Marking

Parts are marked as the examples shown in Figure 31.



Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.

Figure 31. Part Marking for BGA Device