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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7457vg1000nc

1 Overview

The MPC7457 is the fourth implementation of the fourth generation (G4) microprocessors from Freescale. The MPC7457 implements the full PowerPC 32-bit architecture and is targeted at networking and computing systems applications. The MPC7457 consists of a processor core, a 512-Kbyte L2, and an internal L3 tag and controller that support a glueless backside L3 cache through a dedicated high-bandwidth interface. The MPC7447 is identical to the MPC7457 except that it does not support the L3 cache interface.

Figure 1 shows a block diagram of the MPC7457. The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit.

The memory storage subsystem supports the MPX bus protocol and a subset of the 60x bus protocol to main memory and other system resources. The L3 interface supports 1, 2, or 4 Mbytes of external SRAM for L3 cache and/or private memory data. For systems implementing 4 Mbytes of SRAM, a maximum of 2 Mbytes may be used as cache; the remaining 2 Mbytes must be private memory.

Note that the MPC7457 is a footprint-compatible, drop-in replacement in a MPC7455 application if the core power supply is 1.3 V.

2 Features

This section summarizes features of the MPC7457 implementation of the PowerPC architecture.

Major features of the MPC7457 are as follows:

- High-performance, superscalar microprocessor
  - As many as four instructions can be fetched from the instruction cache at a time.
  - As many as three instructions can be dispatched to the issue queues at a time.
  - As many as 12 instructions can be in the instruction queue (IQ).
  - As many as 16 instructions can be at some stage of execution simultaneously.
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history (BHT) with 2 bits per entry for 4 levels of prediction—not-taken, strongly not-taken, taken, and strongly taken
    - Up to three outstanding speculative branches

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Minimum misprediction penalty	6	6	6
Execution Unit Timings (Latency-Throughput)			
Aligned load (integer, float, vector)	3-1, 4-1, 3-1	3-1, 4-1, 3-1	3-1, 4-1, 3-1
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2	4-2, 5-2, 4-2	4-2, 5-2, 4-2
L1 miss, L2 hit latency	9 data/13 instruction	9 data/13 instruction	9 data/13 instruction
SFX (aDd Sub, Shift, Rot, Cmp, logicals)	1-1	1-1	1-1
Integer multiply (32 × 8, 32 × 16, 32 × 32)	3-1, 3-1, 4-2	3-1, 3-1, 4-2	3-1, 3-1, 4-2
Scalar float	5-1	5-1	5-1
VSFX (vector simple)	1-1	1-1	1-1
VCFX (vector complex)	4-1	4-1	4-1
VFPU (vector float)	4-1	4-1	4-1
VPER (vector permute)	2-1	2-1	2-1
MMUs			
TLBs (instruction and data)	128-entry, 2-way	128-entry, 2-way	128-entry, 2-way
Tablewalk mechanism	Hardware + software	Hardware + software	Hardware + software
Instruction BATs/data BATs	8/8	8/8	4/4
L1 I Cache/D Cache Features			
Size	32K/32K	32K/32K	32K/32K
Associativity	8-way	8-way	8-way
Locking granularity	Way	Way	Way
Parity on I cache	Word	Word	Word
Parity on D cache	Byte	Byte	Byte
Number of D cache misses (load/store)	5/1	5/1	5/1
Data stream touch engines	4 streams	4 streams	4 streams
On-Chip Cache Features			
Cache level	L2	L2	L2
Size/associativity	512-Kbyte/8-way	256-Kbyte/8-way	256-Kbyte/8-way
Access width	256 bits	256 bits	256 bits
Number of 32-byte sectors/line	2	2	2
Parity	Byte	Byte	Byte
Off-Chip Cache Support [1]			

5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7457. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 1.5.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency; see Section 1.11, "Ordering Information."

5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 6 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 8 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the MPC7457 will be a function of the AC timings of the MPC7457, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8. For information regarding the use of spread spectrum clock generators, see Section 9.1.3, "System Bus Clock (SYSCLK) and Spread Spectrum Sources." PLL configuration and bus-to-core multiplier information is found in Section 9.1.1, "Core Clocks and PLL Configuration."

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		867 MHz		1000 MHz		1200 MHz		1267 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	600	867	600	1000	600	1200	600	1267	MHz	1
VCO frequency	f_{VCO}	1200	1733	1200	2000	1200	2400	1200	2534	MHz	1
SYSCLK frequency	f_{SYSCLK}	33	167	33	167	33	167	33	167	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	6.0	30	6.0	30	6.0	30	6.0	30	ns	2
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	1.0	—	1.0	—	1.0	—	1.0	ns	3
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter		—	150	—	150	—	150	—	150	ps	5, 6

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		867 MHz		1000 MHz		1200 MHz		1267 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Internal PLL relock time		—	100	—	100	—	100	—	100	µs	7

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.9.1, “PLL Configuration,” for valid PLL_CFG[0:4] settings.
2. Assumes lightly-loaded, single-processor system; see Section 5.2.1, “Clock AC Specifications” for more information.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver’s closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

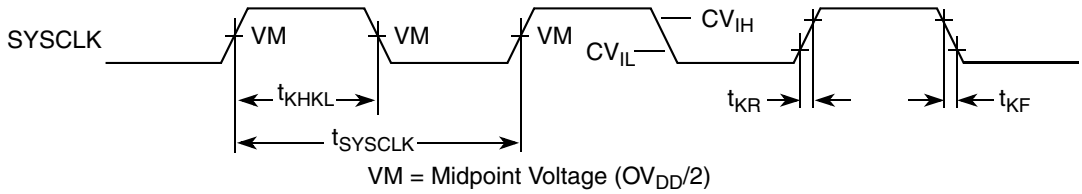


Figure 3. SYSCLK Input Timing Diagram

5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 as defined in Figure 4 and Figure 5. Timing specifications for the L3 bus are provided in Section 5.2.3, “L3 Clock AC Specifications.”

5.2.3 L3 Clock AC Specifications

The L3_CLK frequency is programmed by the L3 configuration register core-to-L3 divisor ratio. See Table 18 for example core and L3 frequencies at various divisors. Table 10 provides the potential range of L3_CLK output AC timing specifications as defined in Figure 7.

The maximum L3_CLK frequency is the core frequency divided by two. Given the high core frequencies available in the MPC7457, however, most SRAM designs will be not be able to operate in this mode using current technology and, as a result, will select a greater core-to-L3 divisor to provide a longer L3_CLK period for read and write access to the L3 SRAMs. Therefore, the typical L3_CLK frequency shown in Table 10 is considered to be the practical maximum in a typical system. The maximum L3_CLK frequency for any application of the MPC7457 will be a function of the AC timings of the MPC7457, the AC timings for the SRAM, bus loading, and printed-circuit board trace length, and may be greater or less than the value given in Table 10. Note that SYSCLK input jitter and L3_CLK[0:1] output jitter are already comprehended in the L3 bus AC timing specifications and do not need to be separately accounted for in an L3 AC timing analysis. Clock skews, where applicable, do need to be accounted for in an AC timing analysis.

Freescale is similarly limited by system constraints and cannot perform tests of the L3 interface on a socketed part on a functional tester at the maximum frequencies of Table 10. Therefore, functional operation and AC timing information are tested at core-to-L3 divisors which result in L3 frequencies at 250 MHz or lower.

Table 10. L3_CLK Output AC Timing Specifications

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [6]						Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)			Rev 1.2 (1.8-, 2.5-V I/O Modes)				
		Min	Typ	Max	Min	Typ	Max		
L3 clock frequency	f_{L3_CLK}	—	200	—	—	250	—	MHz	1
L3 clock cycle time	t_{L3_CLK}	—	5.0	—	—	4.0	—	ns	1
L3 clock duty cycle	t_{CHCL}/t_{L3_CLK}	—	50	—	—	50	—	%	2
L3 clock output-to-output skew (L3_CLK0 to L3_CLK1)	$t_{L3CSKW1}$	—	—	100	—	—	100	ps	3
L3 clock output-to-output skew (L3_CLK[0:1] to L3_ECHO_CLK[1,3])	$t_{L3CSKW2}$	—	—	100	—	—	100	ps	4

5.2.4 L3 Bus AC Specifications

The MPC7457 L3 interface supports three different types of SRAM: source-synchronous, double data rate (DDR) MSUG2 SRAM, Late Write SRAMs, and pipeline burst (PB2) SRAMs. Each requires a different protocol on the L3 interface and a different routing of the L3 clock signals. The type of SRAM is programmed in L3CR[22:23] and the MPC7457 then follows the appropriate protocol for that type. The designer must connect and route the L3 signals appropriately for each type of SRAM. Following are some observations about the L3 interface.

- The routing for the point-to-point signals (L3_CLK[0:1], L3DATA[0:63], L3DP[0:7], and L3_ECHO_CLK[0:3]) to a particular SRAM must be delay matched.
- For 1-Mbyte of SRAM, use L3_ADDR[16:0] (L3_ADDR[0] is LSB)
- For 2-Mbyte of SRAM, use L3_ADDR[17:0] (L3_ADDR[0] is LSB)
- For 4-Mbyte of SRAM, use L3_ADDR[18:0] (L3_ADDR[0] is LSB)
- No pull-up resistors are required for the L3 interface
- For high-speed operations, L3 interface address and control signals should be a ‘T’ with minimal stubs to the two loads; data and clock signals should be point-to-point to their single load. Figure 8 shows the AC test load for the L3 interface.

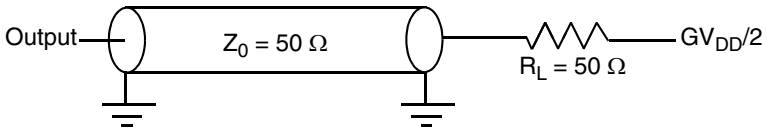


Figure 8. AC Test Load for the L3 Interface

In general, if routing is short, delay-matched, and designed for incident wave reception and minimal reflection, there is a high probability that the AC timing of the MPC7457 L3 interface will meet the maximum frequency operation of appropriately chosen SRAMs. This is despite the pessimistic, guard-banded AC specifications (see Table 12, Table 13, and Table 14), the limitations of functional testers described in Section 5.2.3, “L3 Clock AC Specifications,” and the uncertainty of clocks and signals which inevitably make worst-case critical path timing analysis pessimistic.

More specifically, certain signals within groups should be delay-matched with others in the same group while intergroup routing is less critical. Only the address and control signals are common to both SRAMs and additional timing margin is available for these signals. The double-clocked data signals are grouped with individual clocks as shown in Figure 9 or Figure 11, depending on the type of SRAM. For example, for the MSUG2 DDR SRAM (see Figure 9); L3DATA[0:31], L3DP[0:3], and L3_CLK[0] form a closely coupled group of outputs from the MPC7457; while L3DATA[0:15], L3DP[0:1], and L3_ECHO_CLK[0] form a closely coupled group of inputs.

The *MPC7450 RISC Microprocessor Family User’s Manual* refers to logical settings called ‘sample points’ used in the synchronization of reads from the receive FIFO. The computation of the correct value for this setting is system-dependent and is described in the *MPC7450 RISC Microprocessor Family User’s Manual*. Three specifications are used in this calculation and are given in Table 11. It is essential that all three specifications are included in the calculations to determine the sample points, as incorrect settings can result in errors and unpredictable behavior. For more information, see the *MPC7450 RISC Microprocessor Family User’s Manual.*

window at the internal receiving latches. This delayed clock is used to capture the data into these latches which comprise the receive FIFO. This clock is asynchronous to all other processor clocks. This latched data is subsequently read out of the FIFO synchronously to the processor clock. The time between writing and reading the data is set by the using the sample point settings defined in the L3CR register.

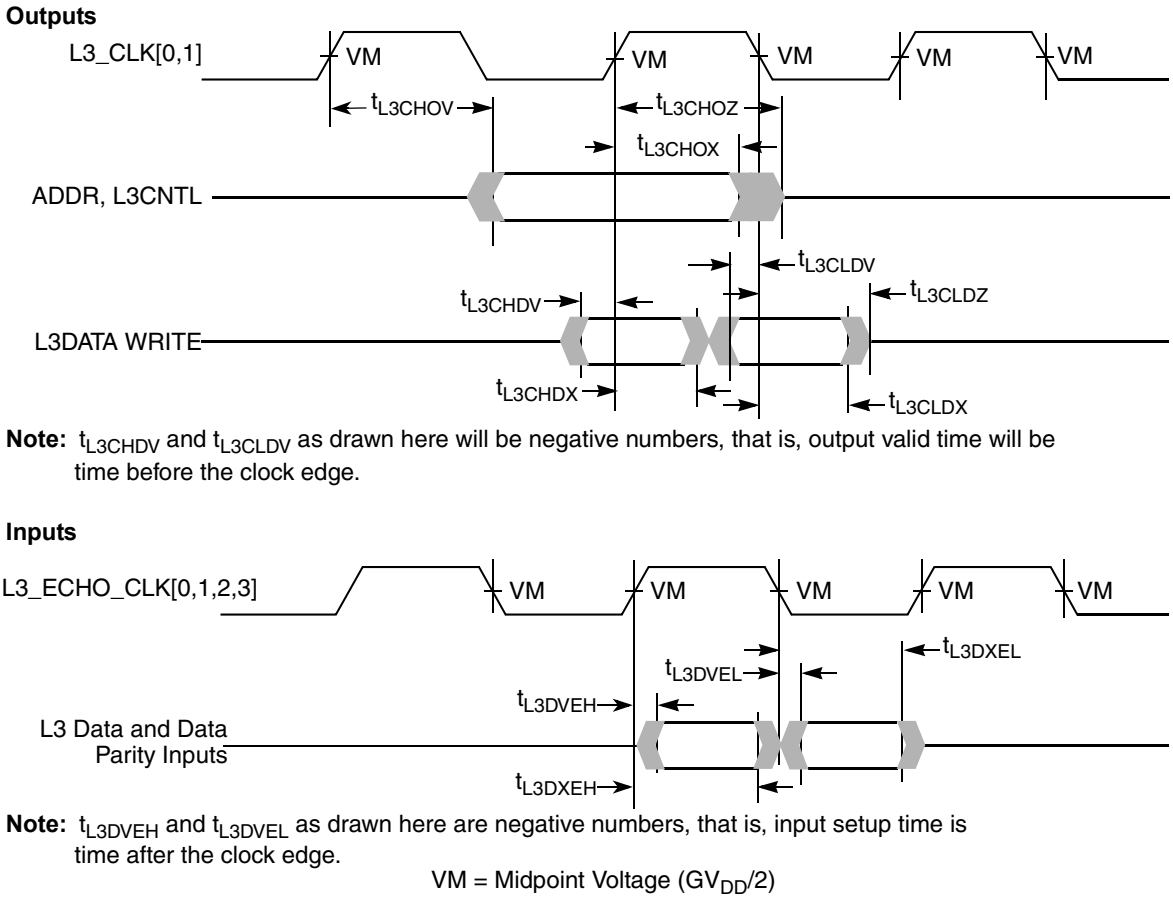
Table 13 provides the L3 bus interface AC timing specifications for the configuration as shown in Figure 9, assuming the timing relationships shown in Figure 10 and the loading shown in Figure 8.

Table 13. L3 Bus Interface AC Timing Specifications for MSUG2

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [9]				Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)		Rev 1.2 (1.8-, 2.5-V I/O Modes)			
		Min	Max	Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	0.75	—	0.75	ns	1
Setup times: Data and parity	t_{L3DVEH}, t_{L3DVEL}	$(-t_{L3CLK}/4) + 0.90$	—	$(-t_{L3CLK}/4) + 0.70$	—	ns	2, 3, 4
Input hold times: Data and parity	t_{L3DXEH}, t_{L3DXEL}	$(t_{L3CLK}/4) + 0.85$	—	$(t_{L3CLK}/4) + 0.70$	—	ns	2, 4
Valid times: Data and parity	t_{L3CHDV}, t_{L3CLDV}	—	$(-t_{L3CLK}/4) + 0.60$	—	$(-t_{L3CLK}/4) + 0.50$	ns	5, 6, 7, 8
Valid times: All other outputs	t_{L3CHOV}	—	$(t_{L3CLK}/4) + 0.65$	—	$(t_{L3CLK}/4) + 0.65$	ns	5, 7, 8
Output hold times: Data and parity	t_{L3CHDX}, t_{L3CLDX},	$(t_{L3CLK}/4) - 0.60$	—	$(t_{L3CLK}/4) - 0.50$	—	ns	5, 6, 7, 8
Output hold times: All other outputs	t_{L3CHOX}	$(t_{L3CLK}/4) - 0.50$	—	$(t_{L3CLK}/4) - 0.50$	—	ns	5, 7, 8
L3_CLK to high impedance: Data and parity	t_{L3CLDZ}	—	$(-t_{L3CLK}/4) + 0.60$	—	$(-t_{L3CLK}/4) + 0.60$	ns	

Figure 10 shows the L3 bus timing diagrams for the MPC7457 interfaced to MSUG2 SRAMs.



Note: t_{L3CHDV} and t_{L3CLDV} as drawn here will be negative numbers, that is, output valid time will be time before the clock edge.

Note: t_{L3DVEH} and t_{L3DVEL} as drawn here are negative numbers, that is, input setup time is time after the clock edge.

VM = Midpoint Voltage ($GV_{DD}/2$)

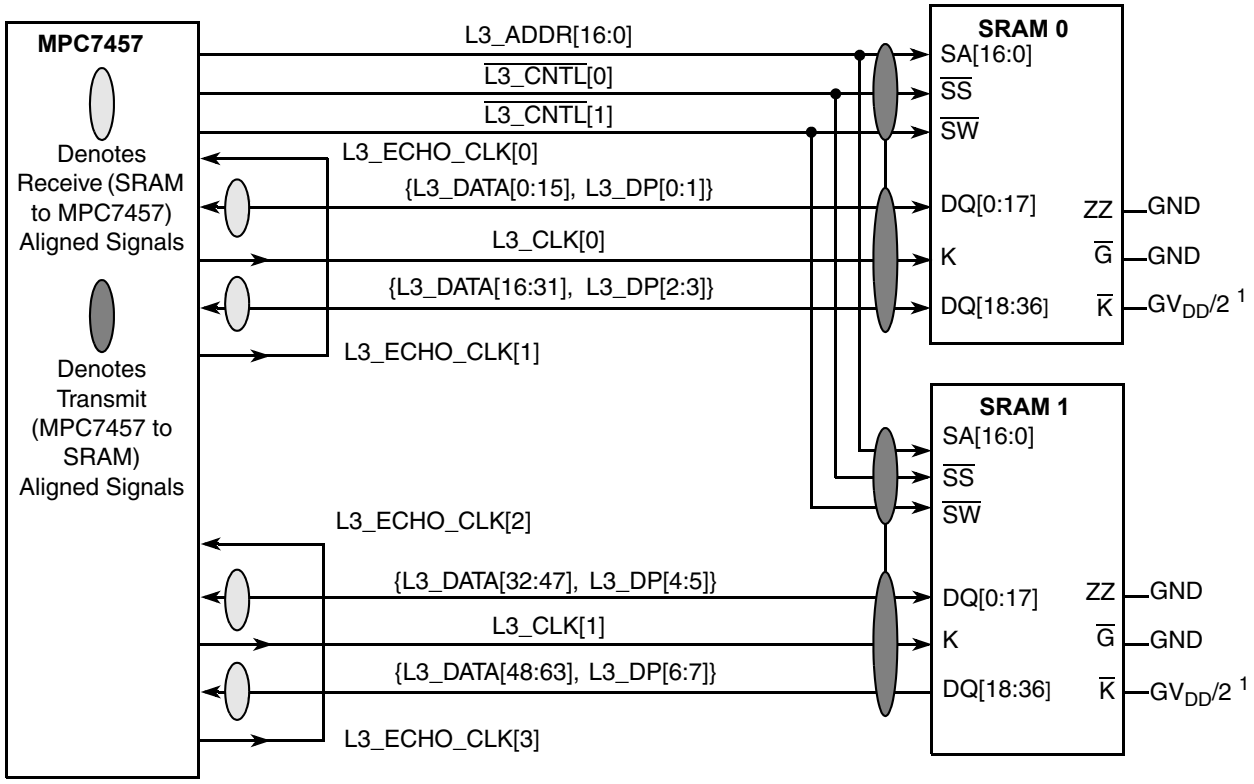
Figure 10. L3 Bus Timing Diagrams for L3 Cache DDR SRAMs

5.2.4.3 L3 Bus AC Specifications for PB2 and Late Write SRAMs

When using PB2 or Late Write SRAMs at the L3 interface, the parts should be connected as shown in Figure 11. These SRAMs are synchronous to the MPC7457; one L3_CLK*n* signal is output to each SRAM to latch address, control, and write data. Read data is launched by the SRAM synchronous to the delayed L3_CLK*n* signal it received. The MPC7457 needs a copy of that delayed clock which launched the SRAM read data to know when the returning data will be valid. Therefore, L3_ECHO_CLK1 and L3_ECHO_CLK3 must be routed halfway to the SRAMs and returned to the MPC7457 inputs L3_ECHO_CLK0 and L3_ECHO_CLK2, respectively. Thus, L3_ECHO_CLK0 and L3_ECHO_CLK2 are phase-aligned with the input clock received at the SRAMs. The MPC7457 will latch the incoming data on the rising edge of L3_ECHO_CLK0 and L3_ECHO_CLK2.

Table 14 provides the L3 bus interface AC timing specifications for the configuration shown in Figure 11, assuming the timing relationships of Figure 12 and the loading of Figure 8.

Figure 11 shows the typical connection diagram for the MPC7457 interfaced to PB2 SRAMs or Late Write SRAMs.



Note:
1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 11. Typical Synchronous 1-MByte L3 Cache Late Write or PB2 Interface

Figure 16 provides the boundary-scan timing diagram.

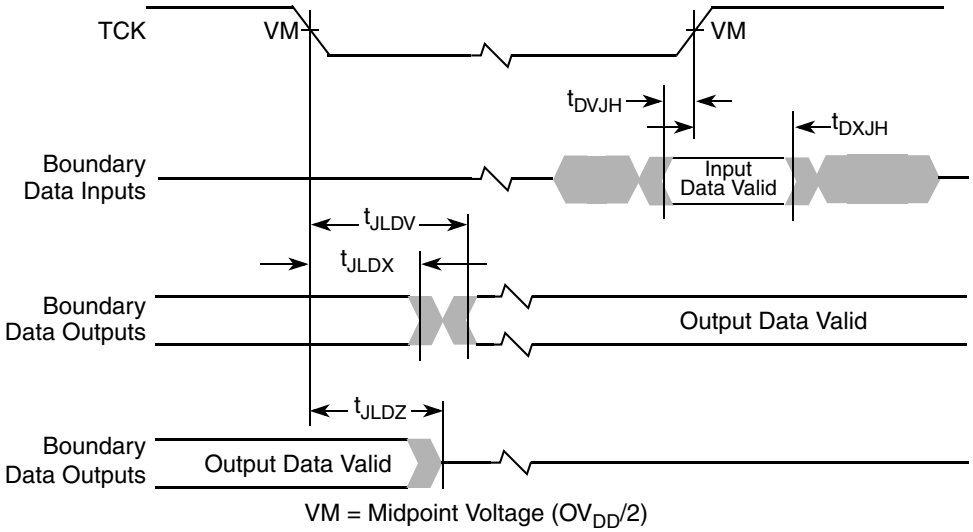


Figure 16. Boundary-Scan Timing Diagram

Figure 17 provides the test access port timing diagram.

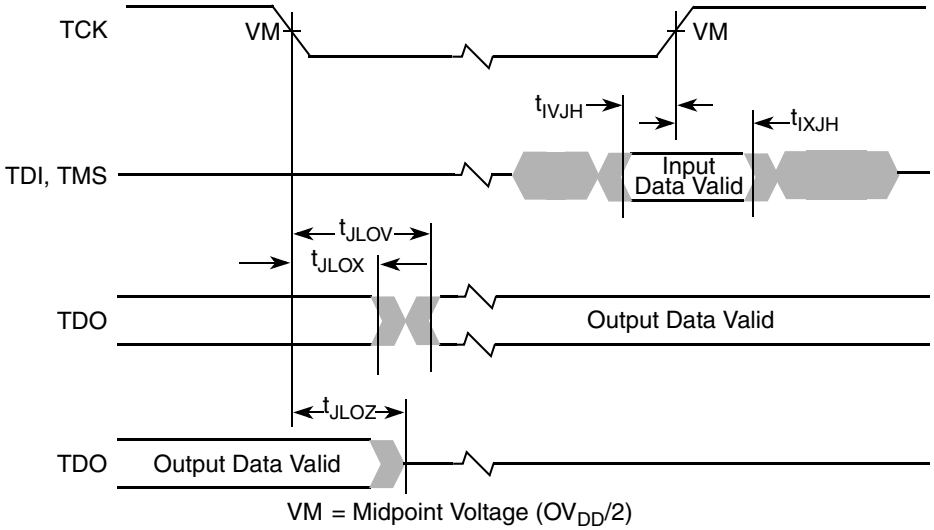
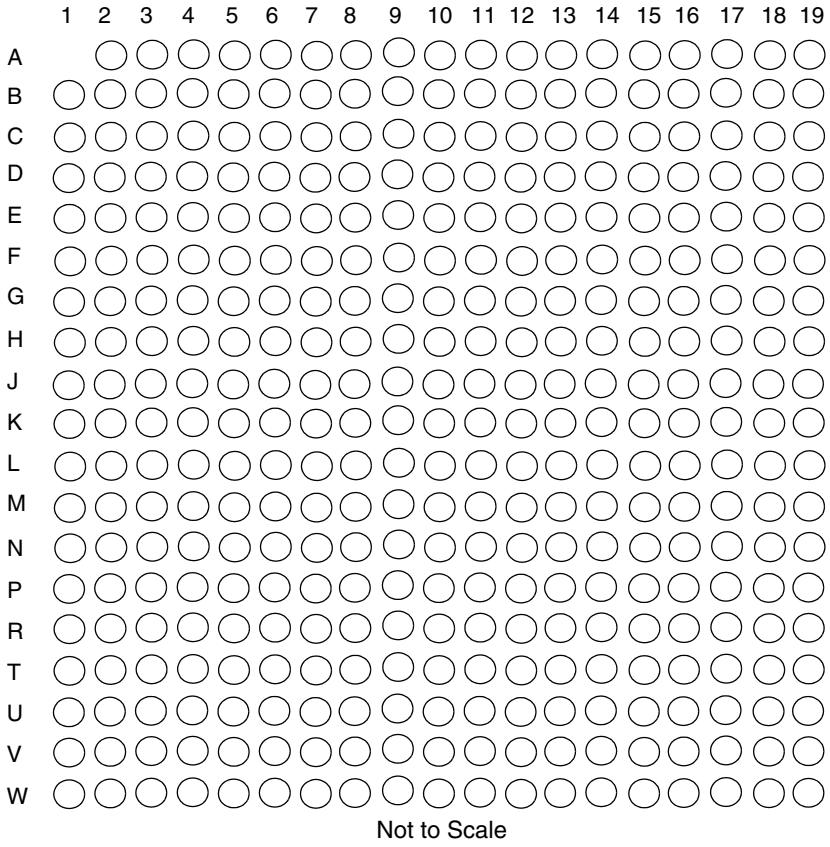


Figure 17. Test Access Port Timing Diagram

6 Pin Assignments

Figure 18 (Part A) shows the pinout of the MPC7447, 360 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

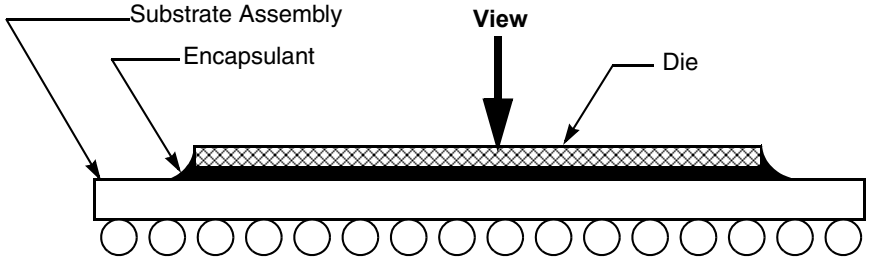
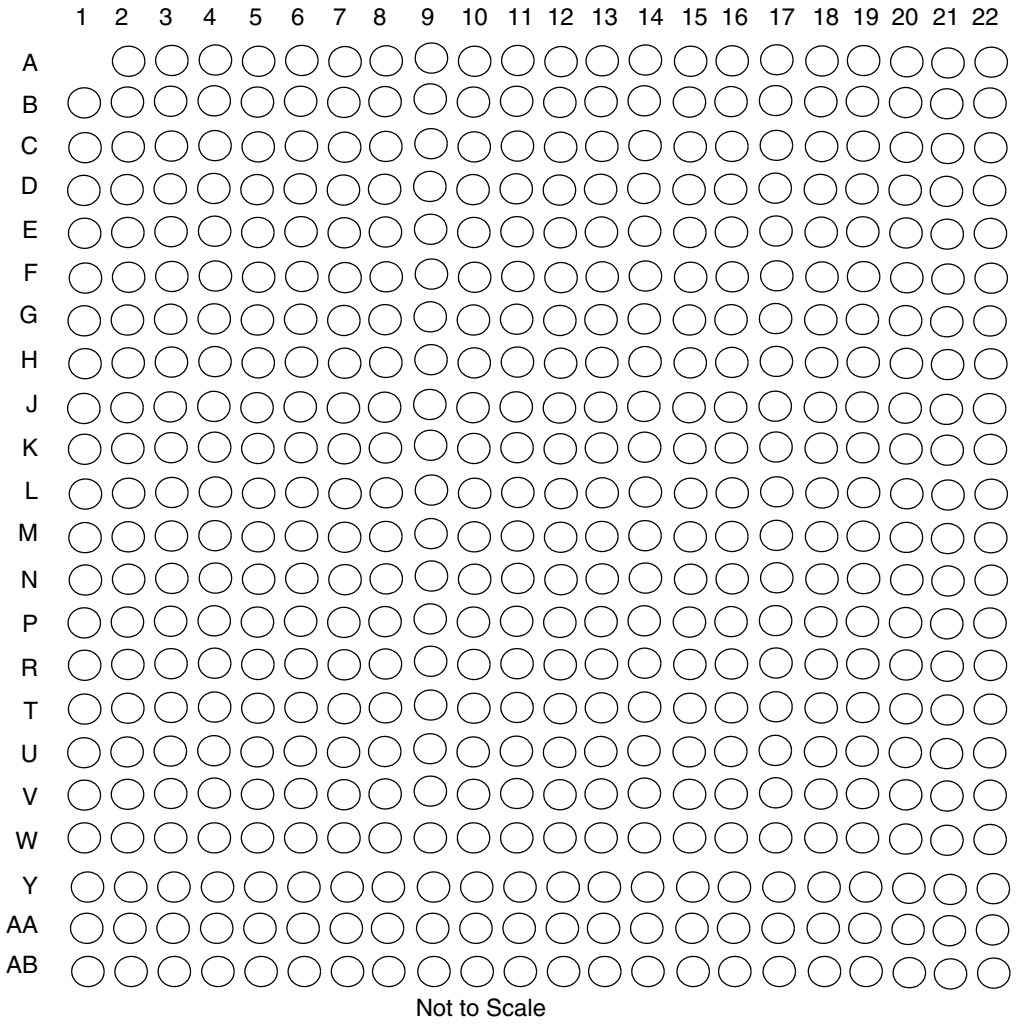


Figure 18. Pinout of the MPC7447, 360 CBGA Package as Viewed from the Top Surface

Figure 19 (Part A) shows the pinout of the MPC7457, 483 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

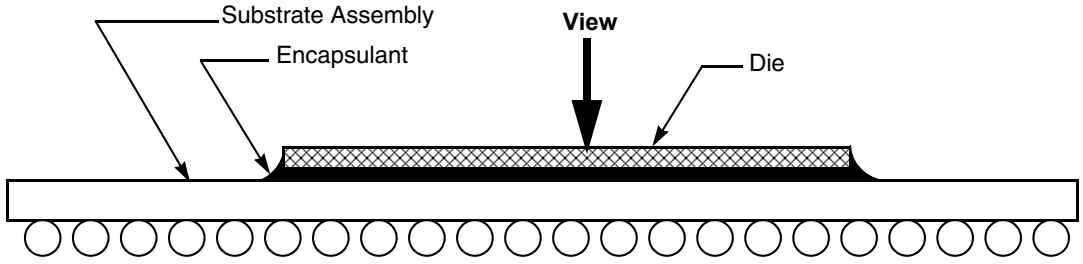


Figure 19. Pinout of the MPC7457, 483 CBGA Package as Viewed from the Top Surface

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
AV_{DD}	B2	—	Input	N/A	
$\overline{BG}$	R3	Low	Input	BVSEL	
$\overline{BMODE0}$	C6	Low	Input	BVSEL	4
$\overline{BMODE1}$	C4	Low	Input	BVSEL	5
$\overline{BR}$	K1	Low	Output	BVSEL	
BVSEL	G6	High	Input	N/A	6, 7
$\overline{CI}$	R1	Low	Output	BVSEL	
$\overline{CKSTP\_IN}$	F3	Low	Input	BVSEL	
$\overline{CKSTP\_OUT}$	K6	Low	Output	BVSEL	
CLK_OUT	N1	High	Output	BVSEL	
D[0:63]	AB15, T14, R14, AB13, V14, U14, AB14, W16, AA11, Y11, U12, W13, Y14, U13, T12, W12, AB12, R12, AA13, AB11, Y12, V11, T11, R11, W10, T10, W11, V10, R10, U10, AA10, U9, V7, T8, AB4, Y6, AB7, AA6, Y8, AA7, W8, AB10, AA16, AB16, AB17, Y18, AB18, Y16, AA18, W14, R13, W15, AA14, V16, W6, AA12, V6, AB9, AB6, R7, R9, AA9, AB8, W9	High	I/O	BVSEL	
$\overline{DBG}$	V1	Low	Input	BVSEL	
DP[0:7]	AA2, AB3, AB2, AA8, R8, W5, U8, AB5	High	I/O	BVSEL	
$\overline{DRDY}$	T6	Low	Output	BVSEL	8
DTI[0:3])	P2, T5, U3, P6	High	Input	BVSEL	9
EXT_QUAL	B9	High	Input	BVSEL	10
$\overline{GBL}$	M4	Low	I/O	BVSEL	
GND	A22, B1, B5, B12, B14, B16, B18, B20, C3, C9, C21, D7, D13, D15, D17, D19, E2, E5, E21, F10, F12, F14, F16, F19, G4, G7, G17, G21, H13, H15, H19, H5, J3, J10, J12, J14, J17, J21, K5, K9, K11, K13, K15, K19, L10, L12, L14, L17, L21, M3, M6, M9, M11, M13, M19, N10, N12, N14, N17, N21, P3, P9, P11, P13, P15, P19, R17, R21, T13, T15, T19, T4, T7, T9, U17, U21, V2, V5, V8, V12, V15, V19, W7, W17, W21, Y3, Y9, Y13, Y15, Y20, AA5, AA17, AB1, AB22	—	—	N/A	
GV_{DD}	B13, B15, B17, B19, B21, D12, D14, D16, D18, D21, E19, F13, F15, F17, F21, G19, H12, H14, H17, H21, J19, K17, K21, L19, M17, M21, N19, P17, P21, R15, R19, T17, T21, U19, V17, V21, W19, Y21	—	—	N/A	11
$\overline{HIT}$	K2	Low	Output	BVSEL	8
$\overline{HRESET}$	A3	Low	Input	BVSEL	
$\overline{INT}$	J6	Low	Input	BVSEL	

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the CBGA package.

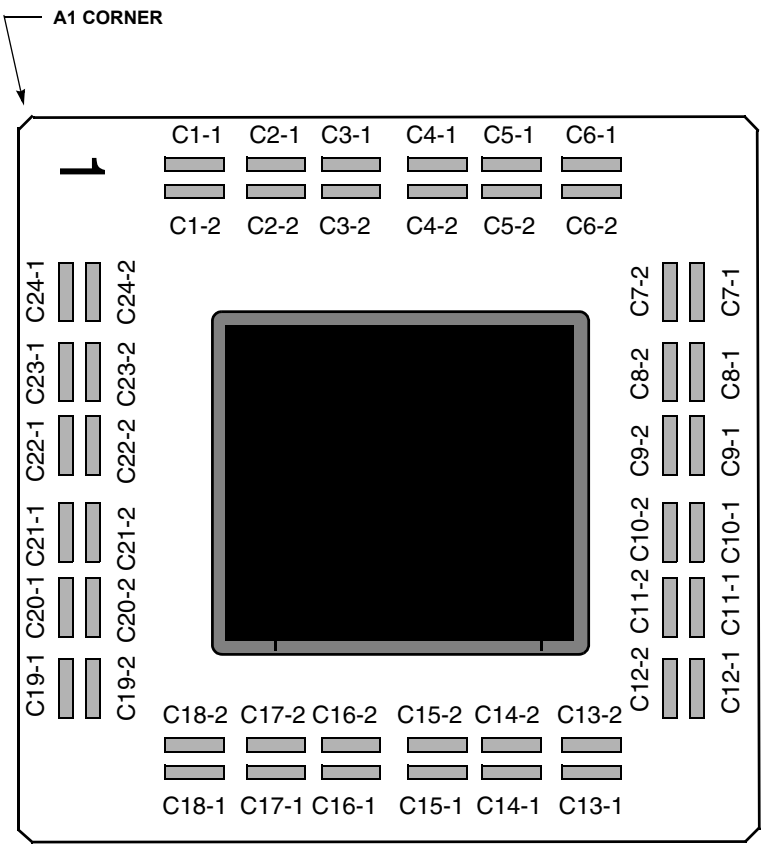
8.1 Package Parameters for the MPC7447, 360 CBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.24 mm
Ball diameter	0.89 mm (35 mil)

8.3 Substrate Capacitors for the MPC7447, 360 CBGA

Figure 21 shows the connectivity of the substrate capacitor pads for the MPC7447, 360 CBGA. All capacitors are 100 nF.

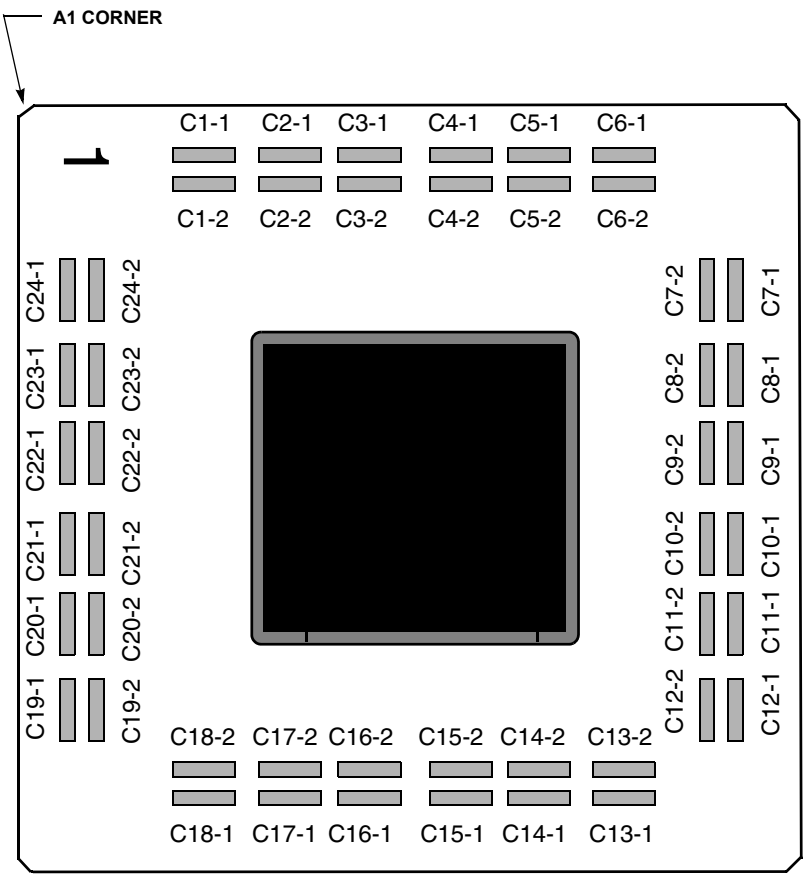


Capacitor	Pad Number	
	-1	-2
C1	GND	V_{DD}
C2	GND	V_{DD}
C3	GND	OV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	V_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	OV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	V_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

Figure 21. Substrate Bypass Capacitors for the MPC7447, 360 CBGA

8.6 Substrate Capacitors for the MPC7457, 483 CBGA or RoHS BGA

Figure 23 shows the connectivity of the substrate capacitor pads for the MPC7457, 483 CBGA or RoHS BGA. All capacitors are 100 nF.



Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

Figure 23. Substrate Bypass Capacitors for the MPC7457, 483 CBGA or RoHS BGA

9 System Design Information

This section provides system and thermal design recommendations for successful application of the MPC7457.

9.1 Clocks

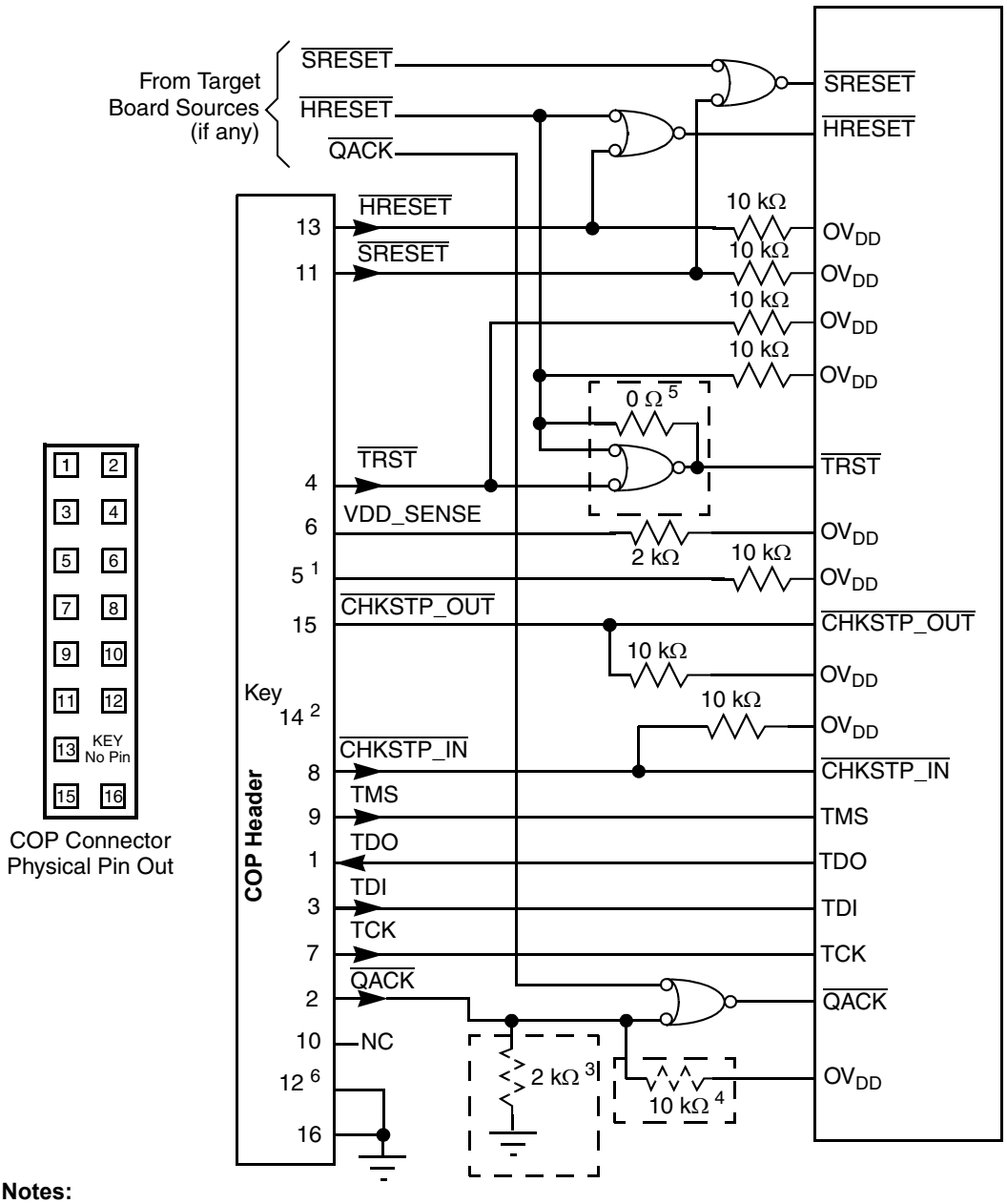
The following sections provide more detailed information regarding the clocking of the MPC7457.

9.1.1 Core Clocks and PLL Configuration

The MPC7457 PLL is configured by the PLL_CFG[0:4] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7457 is shown in Table 18 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 1-GHz column in Table 8. Note that these configurations were different in some earlier MPC7450-family devices and care should be taken when upgrading to the MPC7457 to verify the correct PLL settings for an application.

Table 18. MPC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts

PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
01000	2x	2x								
10000	3x	2x								
10100	4x	2x								667 (1333)
10110	5x	2x							667 (1333)	835 (1670)
10010	5.5x	2x							733 (1466)	919 (1837)
11010	6x	2x						600 (1200)	800 (1600)	1002 (2004)
01010	6.5x	2x						650 (1300)	866 (1730)	1086 (2171)
00100	7x	2x						700 (1400)	931 (1862)	1169 (2338)
00010	7.5x	2x					623 (1245)	750 (1500)	1000 (2000)	1253 (2505)
11000	8x	2x				600 (1200)	664 (1328)	800 (1600)	1064 (2128)	
01100	8.5x	2x				638 (1276)	706 (1412)	850 (1700)	1131 (2261)	



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7457. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. Though defined as a No-Connect, it is a common and recommended practice to use pin 12 as an additional GND pin for improved signal integrity.

Figure 26. JTAG Interface Connection

9.8 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 27); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. If a spring clip is used, the spring force should not exceed 10 pounds.

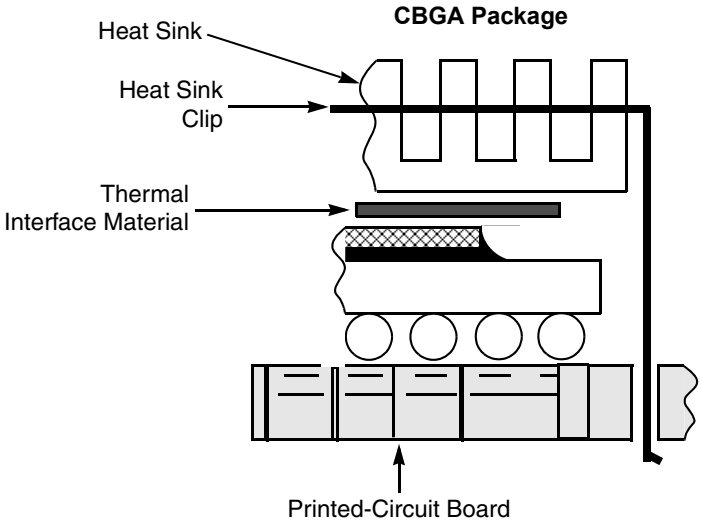


Figure 27. Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the MPC7457. There are several commercially available heat sinks for the MPC7457 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
Calgreg Thermal Solutions 60 Alhambra Road Warwick, RI 02886 Internet: www.calgregthermalsolutions.com	401-732-8100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277

9.8.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 29 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 27). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure and is recommended due to the high power dissipation of the MPC7457. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

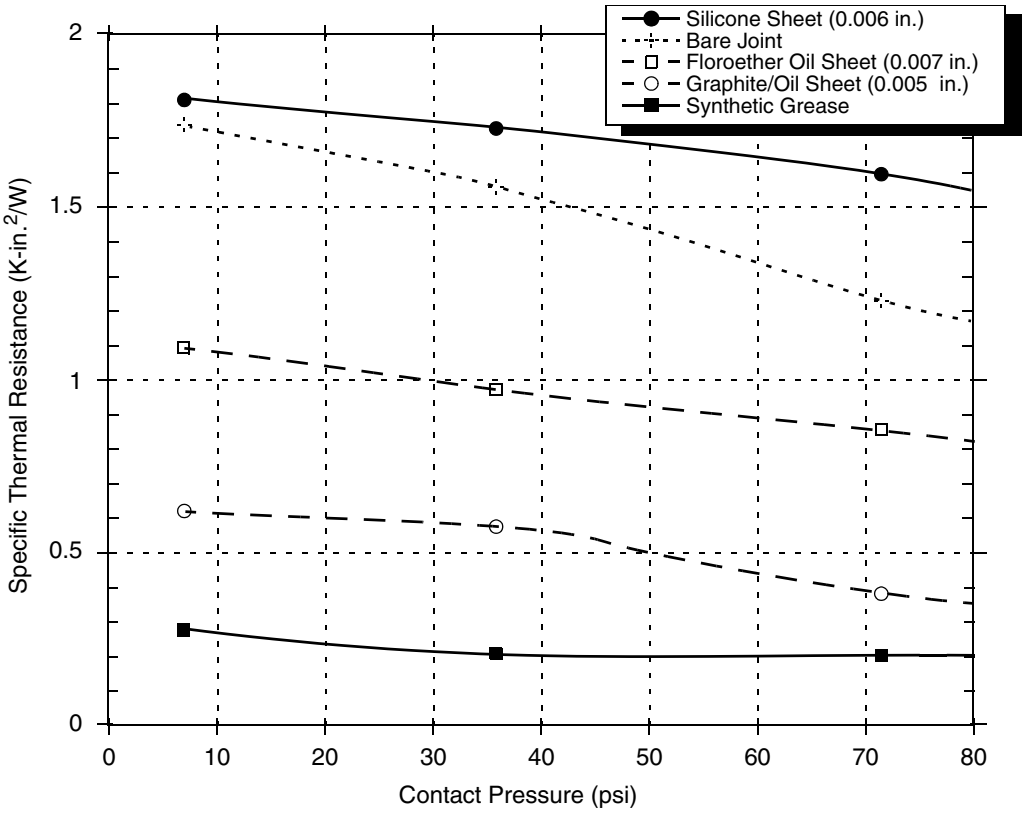


Figure 29. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors: