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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

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Graphics Acceleration	-
Display & Interface Controllers	-
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1 Overview

The MPC7457 is the fourth implementation of the fourth generation (G4) microprocessors from Freescale. The MPC7457 implements the full PowerPC 32-bit architecture and is targeted at networking and computing systems applications. The MPC7457 consists of a processor core, a 512-Kbyte L2, and an internal L3 tag and controller that support a glueless backside L3 cache through a dedicated high-bandwidth interface. The MPC7447 is identical to the MPC7457 except that it does not support the L3 cache interface.

Figure 1 shows a block diagram of the MPC7457. The core is a high-performance superscalar design supporting a double-precision floating-point unit and a SIMD multimedia unit.

The memory storage subsystem supports the MPX bus protocol and a subset of the 60x bus protocol to main memory and other system resources. The L3 interface supports 1, 2, or 4 Mbytes of external SRAM for L3 cache and/or private memory data. For systems implementing 4 Mbytes of SRAM, a maximum of 2 Mbytes may be used as cache; the remaining 2 Mbytes must be private memory.

Note that the MPC7457 is a footprint-compatible, drop-in replacement in a MPC7455 application if the core power supply is 1.3 V.

2 Features

This section summarizes features of the MPC7457 implementation of the PowerPC architecture.

Major features of the MPC7457 are as follows:

- High-performance, superscalar microprocessor
  - As many as four instructions can be fetched from the instruction cache at a time.
  - As many as three instructions can be dispatched to the issue queues at a time.
  - As many as 12 instructions can be in the instruction queue (IQ).
  - As many as 16 instructions can be at some stage of execution simultaneously.
  - Single-cycle execution for most instructions
  - One instruction per clock cycle throughput for most instructions
  - Seven-stage pipeline control
- Eleven independent execution units and three register files
  - Branch processing unit (BPU) features static and dynamic branch prediction
    - 128-entry (32-set, four-way set associative) branch target instruction cache (BTIC), a cache of branch instructions that have been encountered in branch/loop code sequences. If a target instruction is in the BTIC, it is fetched into the instruction queue a cycle sooner than it can be made available from the instruction cache. Typically, a fetch that hits the BTIC provides the first four instructions in the target stream.
    - 2048-entry branch history (BHT) with 2 bits per entry for 4 levels of prediction—not-taken, strongly not-taken, taken, and strongly taken
    - Up to three outstanding speculative branches

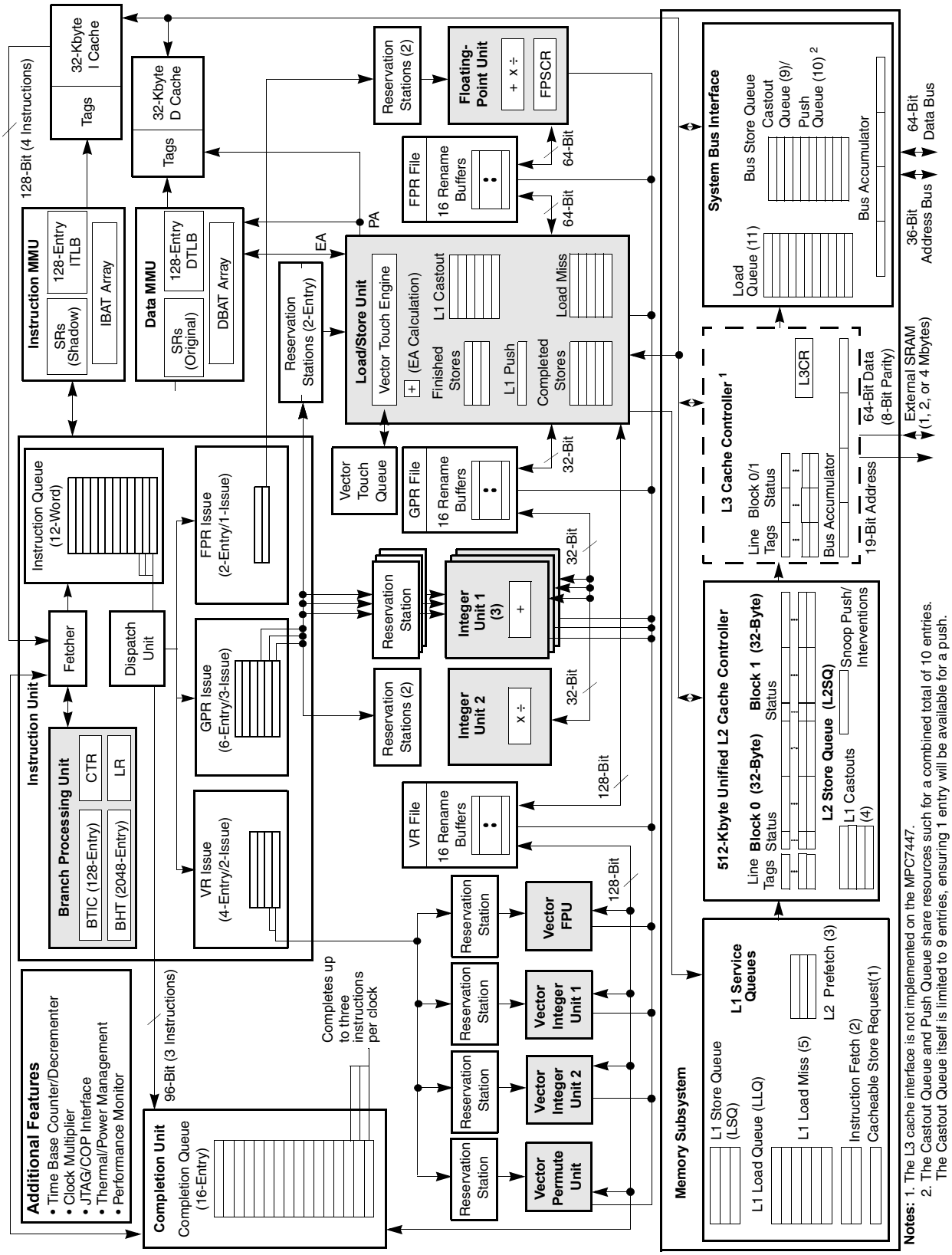


Figure 1. MPC7457 Block Diagram

- Four integer units (IUs) that share 32 GPRs for integer operands
  - Three identical IUs (IU1a, IU1b, and IU1c) can execute all integer instructions except multiply, divide, and move to/from special-purpose register instructions
  - IU2 executes miscellaneous instructions including the CR logical operations, integer multiplication and division instructions, and move to/from special-purpose register instructions
- Five-stage FPU and a 32-entry FPR file
  - Fully IEEE 754-1985 compliant FPU for both single- and double-precision operations
  - Supports non-IEEE mode for time-critical operations
  - Hardware support for denormalized numbers
  - Thirty-two 64-bit FPRs for single- or double-precision operands
- Four vector units and 32-entry vector register file (VRs)
  - Vector permute unit (VPU)
  - Vector integer unit 1 (VIU1) handles short-latency AltiVec™ integer instructions, such as vector add instructions (for example, **vaddsbs**, **vaddshs**, and **vaddsws**)
  - Vector integer unit 2 (VIU2) handles longer-latency AltiVec integer instructions, such as vector multiply add instructions (for example, **vmhaddshs**, **vmhraddshs**, and **vmladduhm**)
  - Vector floating-point unit (VFPU)
- Three-stage load/store unit (LSU)
  - Supports integer, floating-point, and vector instruction load/store traffic
  - Four-entry vector touch queue (VTQ) supports all four architected AltiVec data stream operations
  - Three-cycle GPR and AltiVec load latency (byte, half-word, word, vector) with one-cycle throughput
  - Four-cycle FPR load latency (single, double) with one-cycle throughput
  - No additional delay for misaligned access within double-word boundary
  - Dedicated adder calculates effective addresses (EAs)
  - Supports store gathering
  - Performs alignment, normalization, and precision conversion for floating-point data
  - Executes cache control and TLB instructions
  - Performs alignment, zero padding, and sign extension for integer data
  - Supports hits under misses (multiple outstanding misses)
  - Supports both big- and little-endian modes, including misaligned little-endian accesses

- Three issue queues FIQ, VIQ, and GIQ can accept as many as one, two, and three instructions, respectively, in a cycle. Instruction dispatch requires the following:
  - Instructions can be dispatched only from the three lowest IQ entries—IQ0, IQ1, and IQ2
  - A maximum of three instructions can be dispatched to the issue queues per clock cycle

3 Comparison with the MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441

Table 1 compares the key features of the MPC7457 with the key features of the earlier MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441. To achieve a higher frequency, the number of logic levels per cycle is reduced. Also, to achieve this higher frequency, the pipeline of the MPC7457 is extended (compared to the MPC7400), while maintaining the same level of performance as measured by the number of instructions executed per cycle (IPC).

Table 1. Microarchitecture Comparison

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Basic Pipeline Functions			
Logic inversions per cycle	18	18	18
Pipeline stages up to execute	5	5	5
Total pipeline stages (minimum)	7	7	7
Pipeline maximum instruction throughput	3 + Branch	3 + Branch	3 + Branch
Pipeline Resources			
Instruction buffer size	12	12	12
Completion buffer size	16	16	16
Renames (integer, float, vector)	16, 16, 16	16, 16, 16	16, 16, 16
Maximum Execution Throughput			
SFX	3	3	3
Vector	2 (any 2 of 4 units)	2 (any 2 of 4 units)	2 (any 2 of 4 units)
Scalar floating-point	1	1	1
Out-of-Order Window Size in Execution Queues			
SFX integer units	1 entry × 3 queues	1 entry × 3 queues	1 entry × 3 queues
Vector units	In order, 4 queues	In order, 4 queues	In order, 4 queues
Scalar floating-point unit	In order	In order	In order
Branch Processing Resources			
Prediction structures	BTIC, BHT, link stack	BTIC, BHT, link stack	BTIC, BHT, link stack
BTIC size, associativity	128-entry, 4-way	128-entry, 4-way	128-entry, 4-way
BHT size	2K-entry	2K-entry	2K-entry
Link stack depth	8	8	8
Unresolved branches supported	3	3	3
Branch taken penalty (BTIC hit)	1	1	1

Figure 5 provides the mode select input timing diagram for the MPC7457.

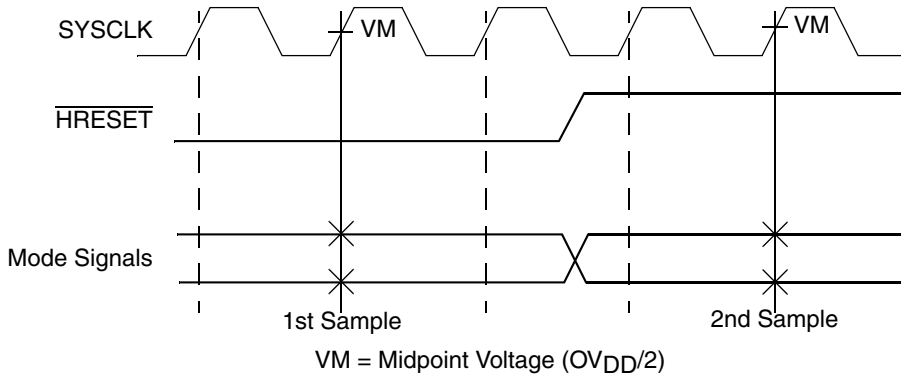


Figure 5. Mode Input Timing Diagram

Figure 6 provides the input/output timing diagram for the MPC7457.

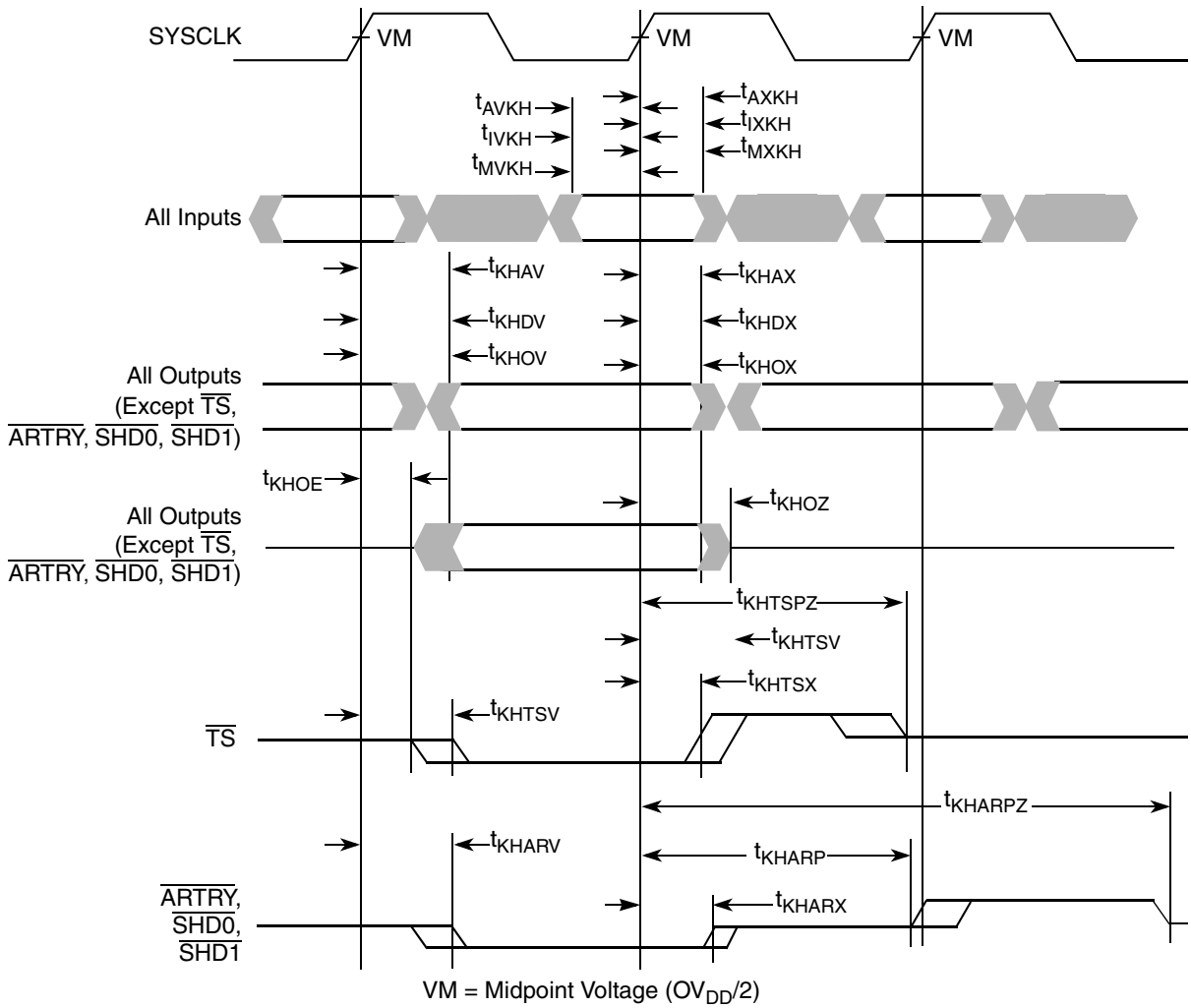


Figure 6. Input/Output Timing Diagram

Table 11. Sample Points Calculation Parameters

Parameter	Symbol	Max	Unit	Notes
Delay from processor clock to internal_L3_CLK	t_{AC}	3/4	t_{L3_CLK}	1
Delay from internal_L3_CLK to L3_CLK[*n*] output pins	t_{CO}	3	ns	2
Delay from L3_ECHO_CLK[*n*] to receive latch	t_{ECI}	3	ns	3

Notes:

1. This specification describes a logical offset between the internal clock edge used to launch the L3 address and control signals (this clock edge is phase-aligned with the processor clock edge) and the internal clock edge used to launch the L3_CLK[*n*] signals. With proper board routing, this offset ensures that the L3_CLK[*n*] edge will arrive at the SRAM within a valid address window and provide adequate setup and hold time. This offset is reflected in the L3 bus interface AC timing specifications, but must also be separately accounted for in the calculation of sample points and, thus, is specified here.
2. This specification is the delay from a rising or falling edge on the internal_L3_CLK signal to the corresponding rising or falling edge at the L3CLK[*n*] pins.
3. This specification is the delay from a rising or falling edge of L3_ECHO_CLK[*n*] to data valid and ready to be sampled from the FIFO.

5.2.4.1 Effects of L3OHCR Settings on L3 Bus AC Specifications

The AC timing of the L3 interface can be adjusted using the L3 Output Hold Control Register (L3OCHR). Each field controls the timing for a group of signals. The AC timing specifications presented herein represent the AC timing when the register contains the default value of 0x0000_0000. Incrementing a field delays the associated signals, increasing the output valid time and hold time of the affected signals. In the special case of delaying an L3_CLK signal, the net effect is to decrease the output valid and output hold times of all signals being latched relative to that clock signal. The amount of delay added is summarized in Table 12. Note that these settings affect output timing parameters only and do not impact input timing parameters of the L3 bus in any way.

Table 12. Effect of L3OHCR Settings on L3 Bus AC Timing

At recommended operating conditions. See Table 4.

Field Name[1]	Affected Signals	Value	Output Valid Time		Output Hold Time		Unit	Notes
			Parameter Symbol [2]	Change [3]	Parameter Symbol [2]	Change [3]		
L3AOH	L3_ADDR[18:0], L3_CNTL[0:1]	0b00	t_{L3CHOV}	0	t_{L3CHOX}	0	ps	4
		0b01		+50		+50		
		0b10		+100		+100		
		0b11		+150		+150		

window at the internal receiving latches. This delayed clock is used to capture the data into these latches which comprise the receive FIFO. This clock is asynchronous to all other processor clocks. This latched data is subsequently read out of the FIFO synchronously to the processor clock. The time between writing and reading the data is set by the using the sample point settings defined in the L3CR register.

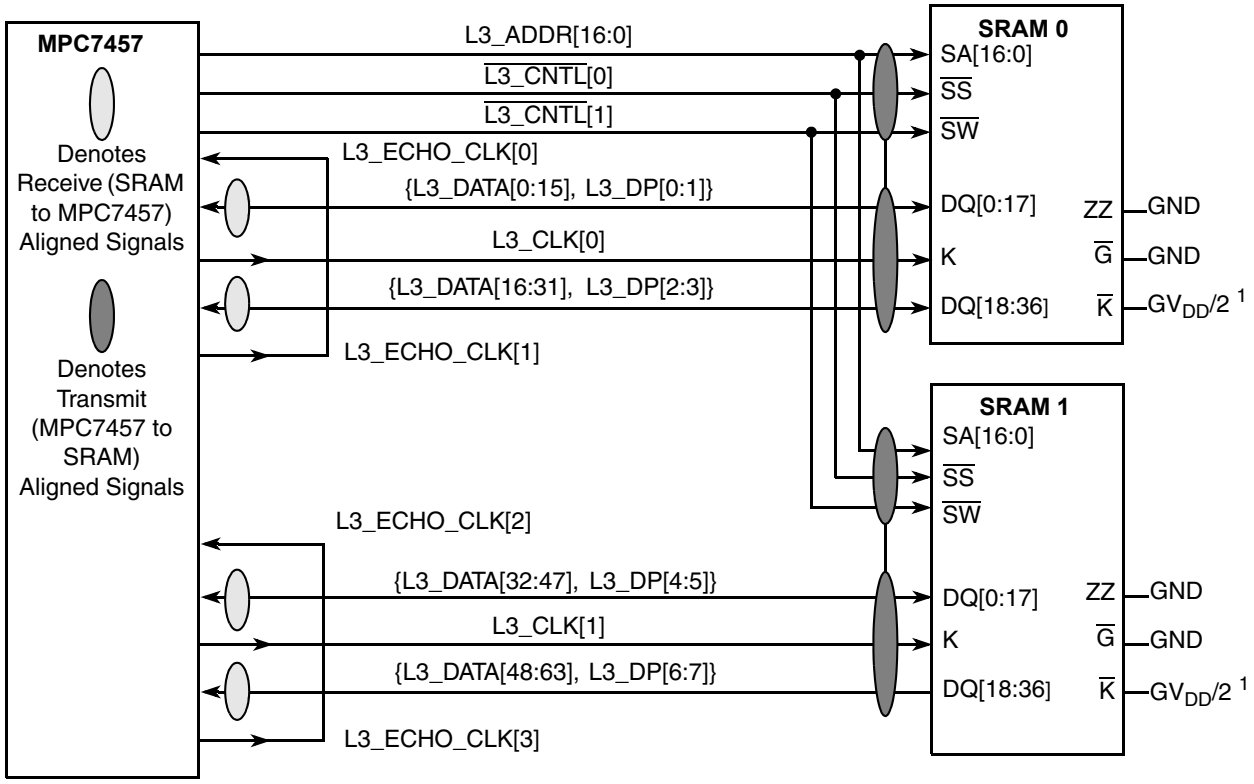
Table 13 provides the L3 bus interface AC timing specifications for the configuration as shown in Figure 9, assuming the timing relationships shown in Figure 10 and the loading shown in Figure 8.

Table 13. L3 Bus Interface AC Timing Specifications for MSUG2

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [9]				Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)		Rev 1.2 (1.8-, 2.5-V I/O Modes)			
		Min	Max	Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	0.75	—	0.75	ns	1
Setup times: Data and parity	t_{L3DVEH}, t_{L3DVEL}	$(-t_{L3CLK}/4) + 0.90$	—	$(-t_{L3CLK}/4) + 0.70$	—	ns	2, 3, 4
Input hold times: Data and parity	t_{L3DXEH}, t_{L3DXEL}	$(t_{L3CLK}/4) + 0.85$	—	$(t_{L3CLK}/4) + 0.70$	—	ns	2, 4
Valid times: Data and parity	t_{L3CHDV}, t_{L3CLDV}	—	$(-t_{L3CLK}/4) + 0.60$	—	$(-t_{L3CLK}/4) + 0.50$	ns	5, 6, 7, 8
Valid times: All other outputs	t_{L3CHOV}	—	$(t_{L3CLK}/4) + 0.65$	—	$(t_{L3CLK}/4) + 0.65$	ns	5, 7, 8
Output hold times: Data and parity	t_{L3CHDX}, t_{L3CLDX},	$(t_{L3CLK}/4) - 0.60$	—	$(t_{L3CLK}/4) - 0.50$	—	ns	5, 6, 7, 8
Output hold times: All other outputs	t_{L3CHOX}	$(t_{L3CLK}/4) - 0.50$	—	$(t_{L3CLK}/4) - 0.50$	—	ns	5, 7, 8
L3_CLK to high impedance: Data and parity	t_{L3CLDZ}	—	$(-t_{L3CLK}/4) + 0.60$	—	$(-t_{L3CLK}/4) + 0.60$	ns	

Figure 11 shows the typical connection diagram for the MPC7457 interfaced to PB2 SRAMs or Late Write SRAMs.



Note:
1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 11. Typical Synchronous 1-MByte L3 Cache Late Write or PB2 Interface

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	 t_{JLDV} t_{JLOV}	 4 4	 20 25	ns	4
Output hold times: Boundary-scan data TDO	 t_{JLDX} t_{JLOX}	 30 30	 — —	ns	4
TCK to output high impedance: Boundary-scan data TDO	 t_{JLDZ} t_{JLOZ}	 3 3	 19 9	ns	4, 5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 13). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 13 provides the AC test load for TDO and the boundary-scan outputs of the MPC7457.

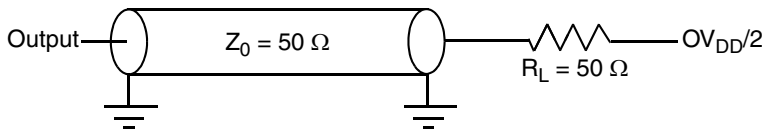


Figure 13. Alternate AC Test Load for the JTAG Interface

Figure 14 provides the JTAG clock input timing diagram.

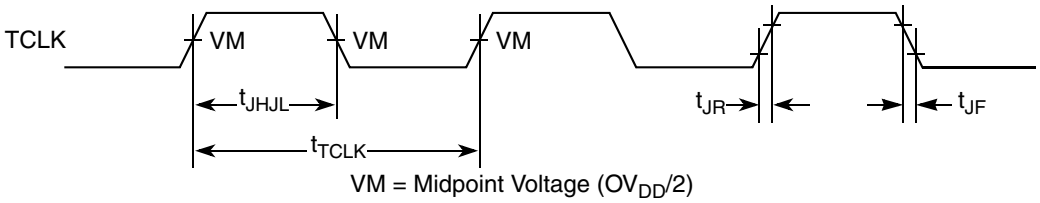


Figure 14. JTAG Clock Input Timing Diagram

Figure 15 provides the $\overline{\text{TRST}}$ timing diagram.

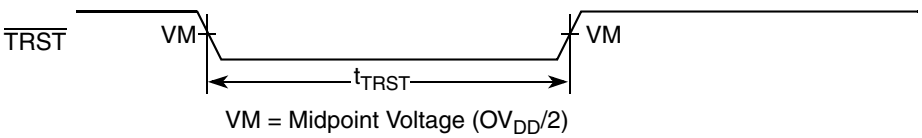


Figure 15. $\overline{\text{TRST}}$ Timing Diagram

Figure 16 provides the boundary-scan timing diagram.

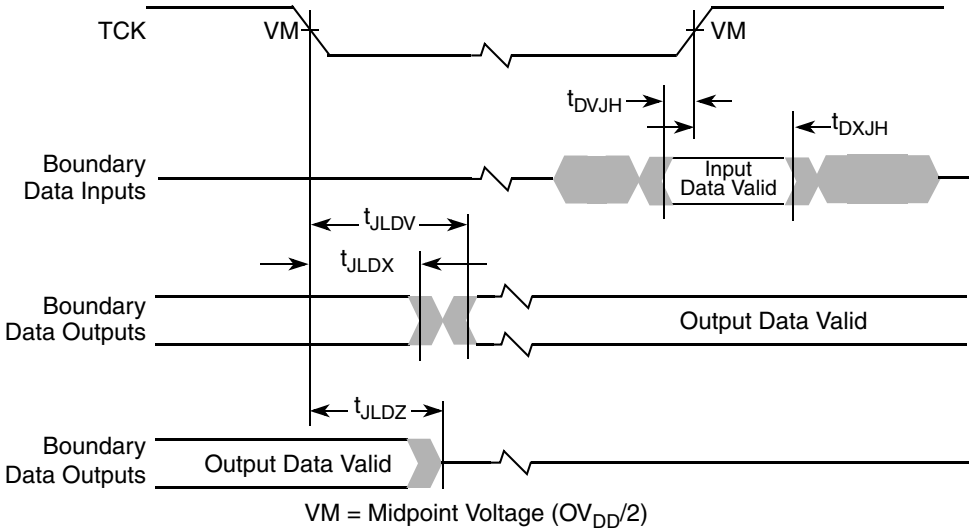


Figure 16. Boundary-Scan Timing Diagram

Figure 17 provides the test access port timing diagram.

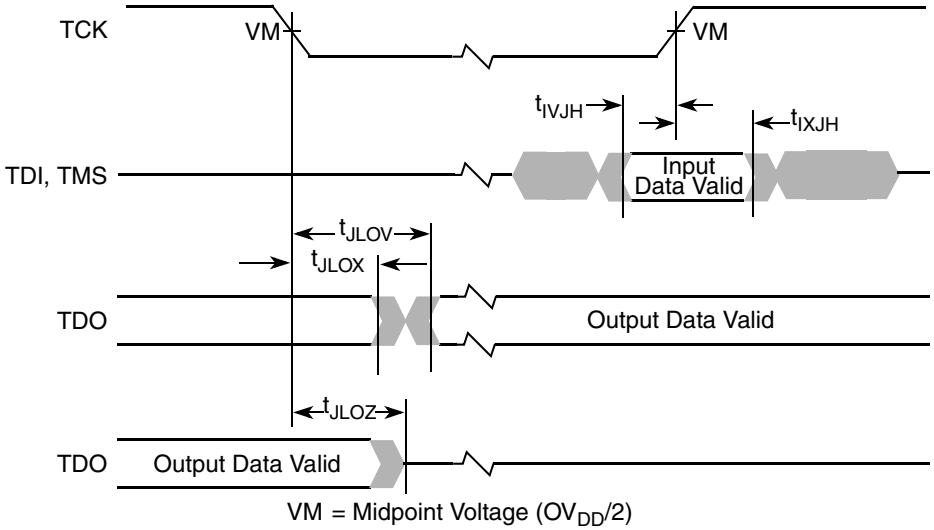
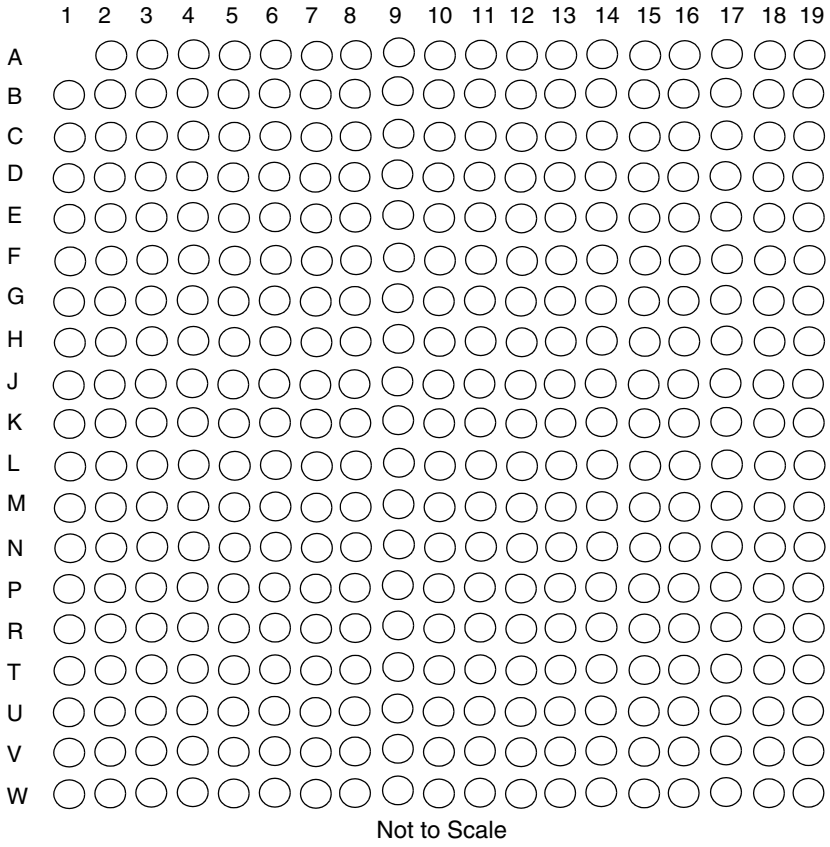


Figure 17. Test Access Port Timing Diagram

6 Pin Assignments

Figure 18 (Part A) shows the pinout of the MPC7447, 360 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

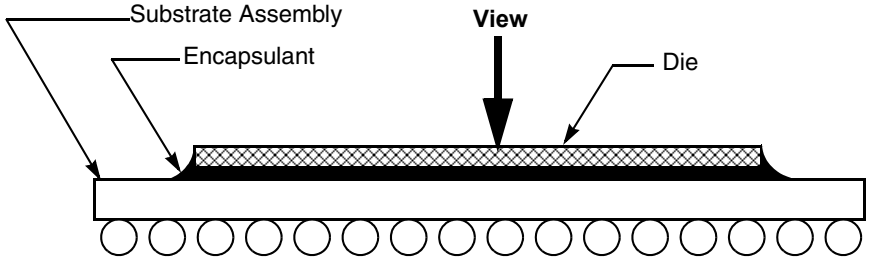
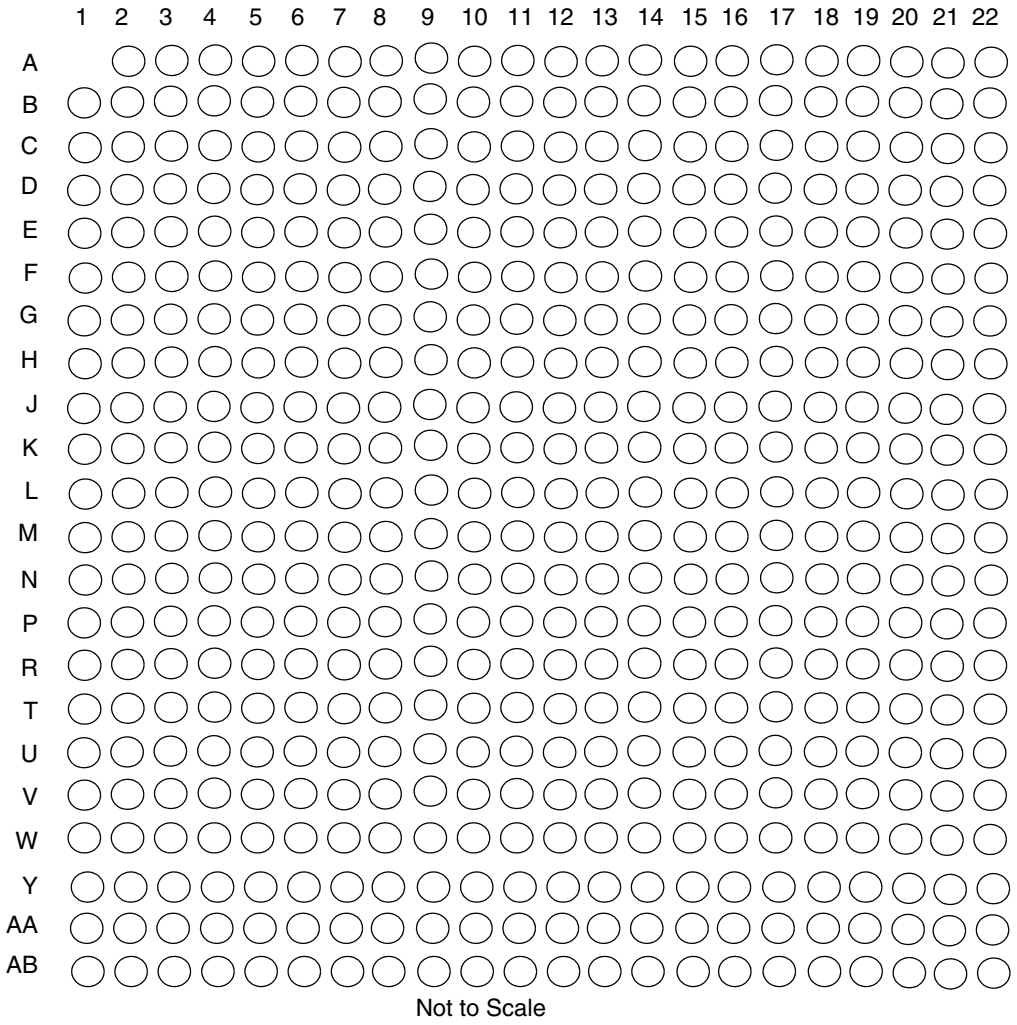


Figure 18. Pinout of the MPC7447, 360 CBGA Package as Viewed from the Top Surface

Figure 19 (Part A) shows the pinout of the MPC7457, 483 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

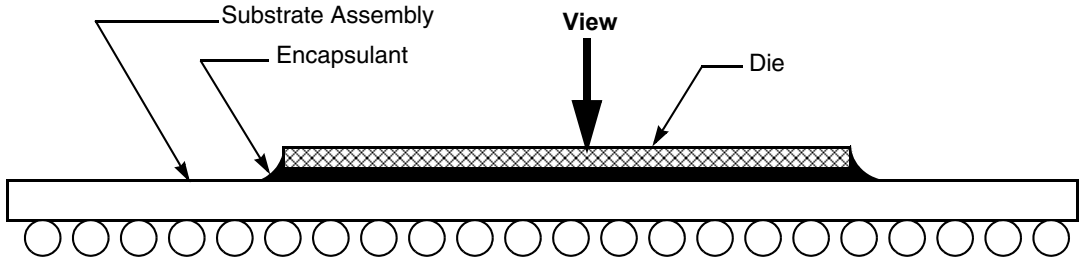


Figure 19. Pinout of the MPC7457, 483 CBGA Package as Viewed from the Top Surface

Table 16. Pinout Listing for the MPC7447, 360 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
$\overline{\text{TEA}}$	L1	Low	Input	BVSEL	
TEST[0:3]	A12, B6, B10, E10	—	Input	BVSEL	12
TEST[4]	D10	—	Input	BVSEL	9
TMS	F1	High	Input	BVSEL	6
$\overline{\text{TRST}}$	A5	Low	Input	BVSEL	6, 14
$\overline{\text{TS}}$	L4	Low	I/O	BVSEL	3
TSIZ[0:2]	G6, F7, E7	High	Output	BVSEL	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	BVSEL	
$\overline{\text{WT}}$	D3	Low	Output	BVSEL	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	N/A	

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). To program the I/O voltage, connect BVSEL to either GND (selects 1.8 V) or to $\overline{\text{HRESET}}$ (selects 2.5 V). If used, the pull-down resistor should be less than 250 Ω. For actual recommended value of V_{in} or supply voltages see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7447 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by $\neg\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7447 is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
A[0:35]	E10, N4, E8, N5, C8, R2, A7, M2, A6, M1, A10, U2, N2, P8, M8, W4, N6, U6, R5, Y4, P1, P4, R6, M7, N7, AA3, U4, W2, W1, W3, V4, AA1, D10, J4, G10, D9	High	I/O	BVSEL	2
$\overline{\text{AACK}}$	U1	Low	Input	BVSEL	
AP[0:4]	L5, L6, J1, H2, G5	High	I/O	BVSEL	
$\overline{\text{ARTRY}}$	T2	Low	I/O	BVSEL	3

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
AV_{DD}	B2	—	Input	N/A	
$\overline{BG}$	R3	Low	Input	BVSEL	
$\overline{BMODE0}$	C6	Low	Input	BVSEL	4
$\overline{BMODE1}$	C4	Low	Input	BVSEL	5
$\overline{BR}$	K1	Low	Output	BVSEL	
BVSEL	G6	High	Input	N/A	6, 7
$\overline{CI}$	R1	Low	Output	BVSEL	
$\overline{CKSTP\_IN}$	F3	Low	Input	BVSEL	
$\overline{CKSTP\_OUT}$	K6	Low	Output	BVSEL	
CLK_OUT	N1	High	Output	BVSEL	
D[0:63]	AB15, T14, R14, AB13, V14, U14, AB14, W16, AA11, Y11, U12, W13, Y14, U13, T12, W12, AB12, R12, AA13, AB11, Y12, V11, T11, R11, W10, T10, W11, V10, R10, U10, AA10, U9, V7, T8, AB4, Y6, AB7, AA6, Y8, AA7, W8, AB10, AA16, AB16, AB17, Y18, AB18, Y16, AA18, W14, R13, W15, AA14, V16, W6, AA12, V6, AB9, AB6, R7, R9, AA9, AB8, W9	High	I/O	BVSEL	
$\overline{DBG}$	V1	Low	Input	BVSEL	
DP[0:7]	AA2, AB3, AB2, AA8, R8, W5, U8, AB5	High	I/O	BVSEL	
$\overline{DRDY}$	T6	Low	Output	BVSEL	8
DTI[0:3])	P2, T5, U3, P6	High	Input	BVSEL	9
EXT_QUAL	B9	High	Input	BVSEL	10
$\overline{GBL}$	M4	Low	I/O	BVSEL	
GND	A22, B1, B5, B12, B14, B16, B18, B20, C3, C9, C21, D7, D13, D15, D17, D19, E2, E5, E21, F10, F12, F14, F16, F19, G4, G7, G17, G21, H13, H15, H19, H5, J3, J10, J12, J14, J17, J21, K5, K9, K11, K13, K15, K19, L10, L12, L14, L17, L21, M3, M6, M9, M11, M13, M19, N10, N12, N14, N17, N21, P3, P9, P11, P13, P15, P19, R17, R21, T13, T15, T19, T4, T7, T9, U17, U21, V2, V5, V8, V12, V15, V19, W7, W17, W21, Y3, Y9, Y13, Y15, Y20, AA5, AA17, AB1, AB22	—	—	N/A	
GV_{DD}	B13, B15, B17, B19, B21, D12, D14, D16, D18, D21, E19, F13, F15, F17, F21, G19, H12, H14, H17, H21, J19, K17, K21, L19, M17, M21, N19, P17, P21, R15, R19, T17, T21, U19, V17, V21, W19, Y21	—	—	N/A	11
$\overline{HIT}$	K2	Low	Output	BVSEL	8
$\overline{HRESET}$	A3	Low	Input	BVSEL	
$\overline{INT}$	J6	Low	Input	BVSEL	

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the CBGA package.

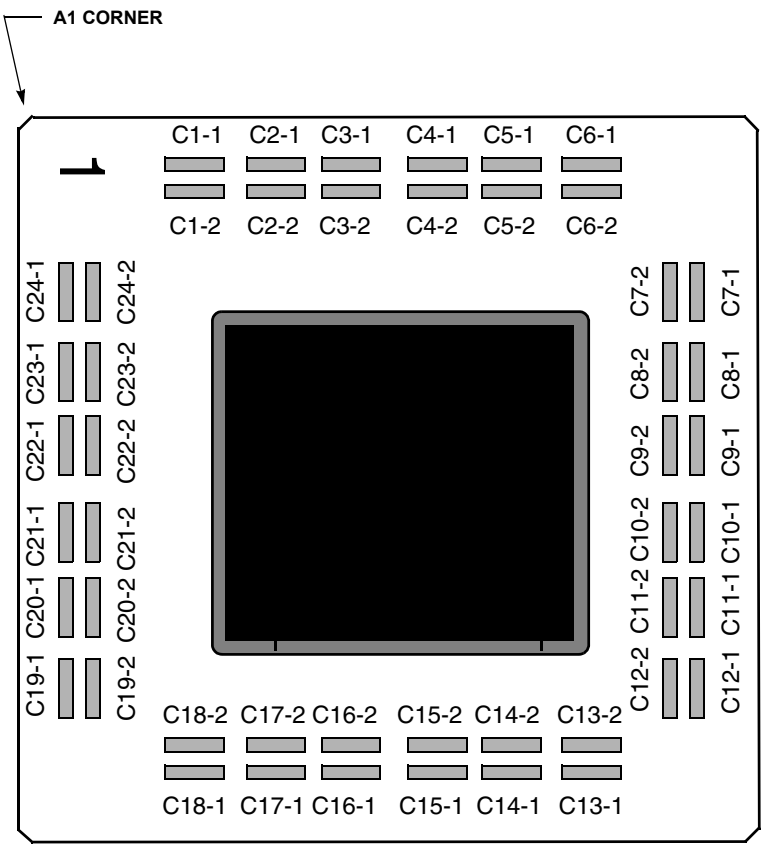
8.1 Package Parameters for the MPC7447, 360 CBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.24 mm
Ball diameter	0.89 mm (35 mil)

8.3 Substrate Capacitors for the MPC7447, 360 CBGA

Figure 21 shows the connectivity of the substrate capacitor pads for the MPC7447, 360 CBGA. All capacitors are 100 nF.



Capacitor	Pad Number	
	-1	-2
C1	GND	V_{DD}
C2	GND	V_{DD}
C3	GND	OV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	V_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	OV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	V_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

Figure 21. Substrate Bypass Capacitors for the MPC7447, 360 CBGA

8.4 Package Parameters for the MPC7457, 483 CBGA or RoHS BGA

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483 ceramic ball grid array (CBGA).

Package outline	29 × 29 mm
Interconnects	483 (22 × 22 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	—
Maximum module height	3.22 mm
Ball diameter	0.89 mm (35 mil)

Table 21. Impedance Characteristics
V_{DD} = 1.5 V, OV_{DD} = 1.8 V ± 5%, T_j = 5°–85°C

Impedance		Processor Bus	L3 Bus	Unit
Z_0	Typical	33–42	34–42	Ω
	Maximum	31–51	32–44	Ω

9.6 Pull-Up/Pull-Down Resistor Requirements

The MPC7457 requires high-resistive (weak: 4.7-kΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being for factory test must be pulled up to OV_{DD} or down to GND to ensure proper device operation. For the MPC7447, 360 BGA, the pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. For the MPC7457, 483 BGA, the pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:5]; the pins that must be pulled down are: L1_TSTCLK and TEST[6]. The $\overline{\text{CKSTP\_IN}}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7–1 kΩ) to prevent erroneous assertions of this signal.

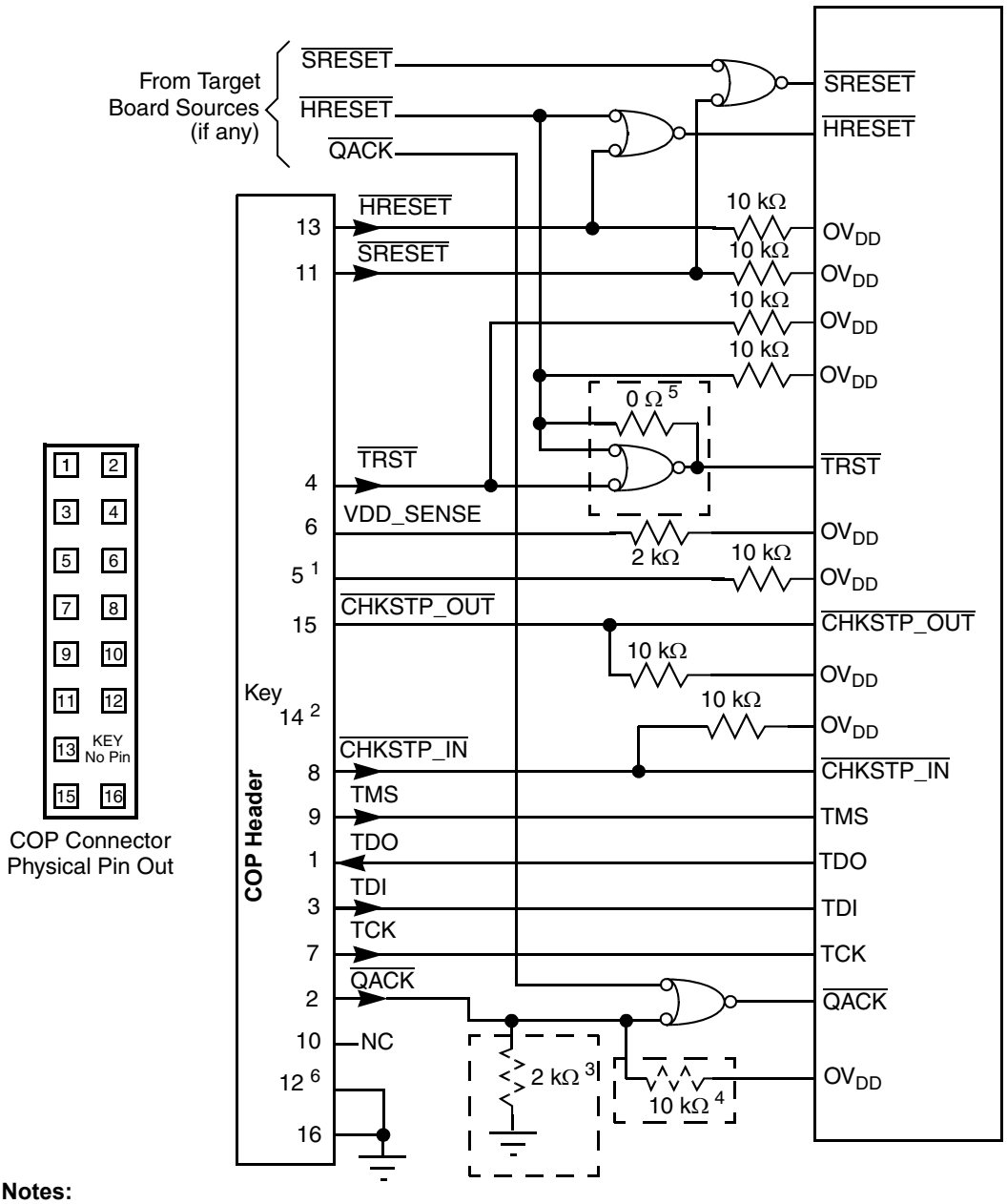
In addition, the MPC7457 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7–1 kΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

If pull-down resistors are used to configure BVSEL or L3VSEL, the resistors should be less than 250 Ω (see Table 16). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the MPC7457 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7457 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system, address bus driven mode enabled (see the *MPC7450 RISC Microprocessor Family Users' Manual* for more information about this mode), or they may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. Preliminary studies have shown the additional power draw by the MPC7457 input receivers to be negligible and, in any event, none of these measures are necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If extended addressing is not used, A[0:3] are unused and must be pulled low to GND through weak pull-down resistors. If the MPC7457 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63] and DP[0:7].



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC7457. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. Though defined as a No-Connect, it is a common and recommended practice to use pin 12 as an additional GND pin for improved signal integrity.

Figure 26. JTAG Interface Connection

Table 24. Part Numbers Addressed by MPC7457TRX*nnnn*LB Series Hardware Specifications Addendum (Document Order No. MPC7457ECS02AD)

MC	7457	T	RX	*nnnn*	L	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7457	T = Extended Temperature Device	RX = CBGA	1000 1267	L: 1.3 V ± 50 mV –40° to 105°C	C: 1.2; PVR = 8002 0102

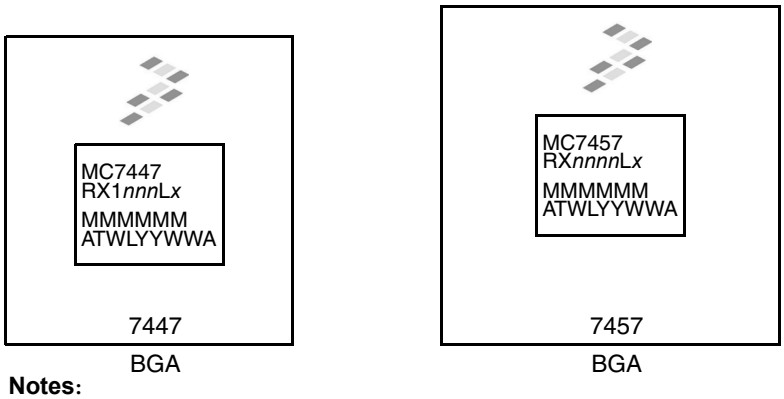
Table 25. Part Numbers Addressed by MPC7457TRX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS03AD)

MC	74*x*7	T	RX	*nnnn*	N	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7447	T = Extended Temperature Device	RX = CBGA	733 1000	N: 1.1 V ± 50 mV –40° to 105°C	B: 1.1; PVR = 8002 0101
	7457					C: 1.2; PVR = 8002 0102

10.3 Part Marking

Parts are marked as the examples shown in Figure 31.



Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.

Figure 31. Part Marking for BGA Device