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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	733MHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.5V, 1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	483-BCBGA, FCCBGA
Supplier Device Package	483-FCCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7457vg733nc

- Branch instructions that do not update the count register (CTR) or link register (LR) are often removed from the instruction stream.
- Eight-entry link register stack to predict the target address of Branch Conditional to Link Register (**bclr**) instructions

  - Space must be available in the CQ for an instruction to dispatch (this includes instructions that are assigned a space in the CQ but not in an issue queue)
- Rename buffers
  - 16 GPR rename buffers
  - 16 FPR rename buffers
  - 16 VR rename buffers
- Dispatch unit
  - Decode/dispatch stage fully decodes each instruction
- Completion unit
  - The completion unit retires an instruction from the 16-entry completion queue (CQ) when all instructions ahead of it have been completed, the instruction has finished execution, and no exceptions are pending.
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
  - 32-Kbyte, eight-way set associative instruction and data caches
  - Pseudo least recently used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software.
  - Caches can be locked in software.
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - L1 cache supports parity generation and checking
  - No snooping of instruction cache except for **icbi** instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 512-Kbyte, eight-way set associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2

  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed).
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.3-V processor core
  - The following three power-saving modes are available to the system:
    - Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and back to nap using a $\overline{\text{QREQ}}$/$\overline{\text{QACK}}$ processor-system handshake protocol.
    - Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled.
    - Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state.
  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and an MPC7457-specific thermal management exception.
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

3 Comparison with the MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441

Table 1 compares the key features of the MPC7457 with the key features of the earlier MPC7455, MPC7445, MPC7450, MPC7451, and MPC7441. To achieve a higher frequency, the number of logic levels per cycle is reduced. Also, to achieve this higher frequency, the pipeline of the MPC7457 is extended (compared to the MPC7400), while maintaining the same level of performance as measured by the number of instructions executed per cycle (IPC).

Table 1. Microarchitecture Comparison

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Basic Pipeline Functions			
Logic inversions per cycle	18	18	18
Pipeline stages up to execute	5	5	5
Total pipeline stages (minimum)	7	7	7
Pipeline maximum instruction throughput	3 + Branch	3 + Branch	3 + Branch
Pipeline Resources			
Instruction buffer size	12	12	12
Completion buffer size	16	16	16
Renames (integer, float, vector)	16, 16, 16	16, 16, 16	16, 16, 16
Maximum Execution Throughput			
SFX	3	3	3
Vector	2 (any 2 of 4 units)	2 (any 2 of 4 units)	2 (any 2 of 4 units)
Scalar floating-point	1	1	1
Out-of-Order Window Size in Execution Queues			
SFX integer units	1 entry × 3 queues	1 entry × 3 queues	1 entry × 3 queues
Vector units	In order, 4 queues	In order, 4 queues	In order, 4 queues
Scalar floating-point unit	In order	In order	In order
Branch Processing Resources			
Prediction structures	BTIC, BHT, link stack	BTIC, BHT, link stack	BTIC, BHT, link stack
BTIC size, associativity	128-entry, 4-way	128-entry, 4-way	128-entry, 4-way
BHT size	2K-entry	2K-entry	2K-entry
Link stack depth	8	8	8
Unresolved branches supported	3	3	3
Branch taken penalty (BTIC hit)	1	1	1

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7457/MPC7447	MPC7455/MPC7445	MPC7450/MPC7451/ MPC7441
Cache level	L3	L3	L3
Total SRAM space supported	1 MB, 2MB, 4 MB [2]	1 MB, 2 MB	1 MB, 2 MB
On-chip tag logical size (cache space)	1 MB, 2 MB	1 MB, 2 MB	1 MB, 2 MB
Associativity	8-way	8-way	8-way
Number of 32-byte sectors/line	2, 4	2, 4	2, 4
Off-Chip data SRAM support	MSUG2 DDR, LW, PB2	MSUG2 DDR, LW, PB2	MSUG2 DDR, LW, PB2
Data path width	64	64	64
Direct mapped SRAM sizes	1 MB, 2 MB, 4 MB	1 MB, 2 MB	1 MB, 2 MB
Parity	Byte	Byte	Byte

Notes:

1. Not implemented on MPC7447, MPC7445, or MPC7441.
2. The MPC7457 supports up to 4 MB of SRAM, of which a maximum of 2 MB can be configured as cache memory; the remaining 2 MB may be unused or configured as private memory.

4 General Parameters

The following list provides a summary of the general parameters of the MPC7457:

Technology	0.13 µm CMOS, nine-layer metal
Die size	9.1 mm × 10.8 mm
Transistor count	58 million
Logic design	Fully-static
Packages	MPC7447: Surface mount 360 ceramic ball grid array (CBGA)
	MPC7457: Surface mount 483 ceramic ball grid array (CBGA)
Core power supply	1.3 V ±50 mV DC nominal
I/O power supply	1.8 V ±5% DC, or
	2.5 V ±5% DC, or
	1.5 V ±5% DC (L3 interface only, not implemented on MPC7447)

5 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7457.

5.1 DC Electrical Characteristics

The tables in this section describe the MPC7457 DC electrical characteristics.Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings [1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.60	V	2
PLL supply voltage		AV_{DD}	–0.3 to 1.60	V	2
Processor bus supply voltage	BVSEL = 0	OV_{DD}	–0.3 to 1.95	V	3, 4
	BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	OV_{DD}	–0.3 to 2.7	V	3, 5
L3 bus supply voltage	L3VSEL = ¬$\overline{\text{HRESET}}$	GV_{DD}	–0.3 to 1.65	V	3, 6
	L3VSEL = 0	GV_{DD}	–0.3 to 1.95	V	3, 7
	L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	GV_{DD}	–0.3 to 2.7	V	3, 8
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3	V	9, 10
	L3 bus	V_{in}	–0.3 to GV_{DD} + 0.3	V	9, 10
	JTAG signals	V_{in}	–0.3 to OV_{DD} + 0.3	V	
Storage temperature range		T_{stg}	–55 to 150	°C	

Notes:
1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{DD}/AV_{DD} must not exceed OV_{DD}/GV_{DD} by more than 1.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution**: OV_{DD}/GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8-V mode.
5. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5-V mode.
6. L3VSEL must be set to ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), such that the bus is in 1.5-V mode.
7. L3VSEL must be set to 0, such that the bus is in 1.8-V mode.
8. L3VSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5-V mode.
9. **Caution**: V_{in} must not exceed OV_{DD} or GV_{DD} by more than 0.3 V at any time including during power-on reset.
10. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Figure 2 shows the undershoot and overshoot voltage on the MPC7457.

Table 5. Package Thermal Characteristics [1] (continued)

Characteristic	Symbol	Value		Unit	Notes
		MPC7447	MPC7457		
Coefficient of thermal expansion		6.8	6.8	ppm/°C	

Notes:
1. Refer to Section 9.8, "Thermal Management Information," for more details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Table 6 provides the DC electrical characteristics for the MPC7457.

Table 6. DC Electrical Specifications

At recommended operating conditions. See Table 4.

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs including SYSCLK)	1.5	V_{IH}	$GV_{DD} \times 0.65$	$GV_{DD} + 0.3$	V	2
	1.8		$OV_{DD}/GV_{DD} \times 0.65$	$OV_{DD}/GV_{DD} + 0.3$	V	
	2.5		1.7	$OV_{DD}/GV_{DD} + 0.3$	V	
Input low voltage (all inputs including SYSCLK)	1.5	V_{IL}	–0.3	$GV_{DD} \times 0.35$	V	2, 6
	1.8		–0.3	$OV_{DD}/GV_{DD} \times 0.35$	V	
	2.5		–0.3	0.7	V	
Input leakage current, $V_{in} = GV_{DD}/OV_{DD}$	—	I_{in}	—	30	µA	2, 3
High-impedance (off-state) leakage current, $V_{in} = GV_{DD}/OV_{DD}$	—	I_{TSI}	—	30	µA	2, 3, 4
Output high voltage, $I_{OH} = –5$ mA	1.5	V_{OH}	$OV_{DD}/GV_{DD} – 0.45$	—	V	6
	1.8		$OV_{DD}/GV_{DD} – 0.45$	—	V	
	2.5		1.8	—	V	
Output low voltage, $I_{OL} = 5$ mA	1.5	V_{OL}	—	0.45	V	6
	1.8		—	0.45	V	
	2.5		—	0.6	V	

5.2.3 L3 Clock AC Specifications

The L3_CLK frequency is programmed by the L3 configuration register core-to-L3 divisor ratio. See Table 18 for example core and L3 frequencies at various divisors. Table 10 provides the potential range of L3_CLK output AC timing specifications as defined in Figure 7.

The maximum L3_CLK frequency is the core frequency divided by two. Given the high core frequencies available in the MPC7457, however, most SRAM designs will be not be able to operate in this mode using current technology and, as a result, will select a greater core-to-L3 divisor to provide a longer L3_CLK period for read and write access to the L3 SRAMs. Therefore, the typical L3_CLK frequency shown in Table 10 is considered to be the practical maximum in a typical system. The maximum L3_CLK frequency for any application of the MPC7457 will be a function of the AC timings of the MPC7457, the AC timings for the SRAM, bus loading, and printed-circuit board trace length, and may be greater or less than the value given in Table 10. Note that SYSCLK input jitter and L3_CLK[0:1] output jitter are already comprehended in the L3 bus AC timing specifications and do not need to be separately accounted for in an L3 AC timing analysis. Clock skews, where applicable, do need to be accounted for in an AC timing analysis.

Freescale is similarly limited by system constraints and cannot perform tests of the L3 interface on a socketed part on a functional tester at the maximum frequencies of Table 10. Therefore, functional operation and AC timing information are tested at core-to-L3 divisors which result in L3 frequencies at 250 MHz or lower.

Table 10. L3_CLK Output AC Timing Specifications

At recommended operating conditions. See Table 4.

Parameter	Symbol	Device Revision (L3 I/O Voltage) [6]						Unit	Notes
		Rev 1.1. (All I/O Modes) Rev 1.2 (1.5-V I/O Mode)			Rev 1.2 (1.8-, 2.5-V I/O Modes)				
		Min	Typ	Max	Min	Typ	Max		
L3 clock frequency	f_{L3_CLK}	—	200	—	—	250	—	MHz	1
L3 clock cycle time	t_{L3_CLK}	—	5.0	—	—	4.0	—	ns	1
L3 clock duty cycle	t_{CHCL}/t_{L3_CLK}	—	50	—	—	50	—	%	2
L3 clock output-to-output skew (L3_CLK0 to L3_CLK1)	$t_{L3CSKW1}$	—	—	100	—	—	100	ps	3
L3 clock output-to-output skew (L3_CLK[0:1] to L3_ECHO_CLK[1,3])	$t_{L3CSKW2}$	—	—	100	—	—	100	ps	4

5.2.4 L3 Bus AC Specifications

The MPC7457 L3 interface supports three different types of SRAM: source-synchronous, double data rate (DDR) MSUG2 SRAM, Late Write SRAMs, and pipeline burst (PB2) SRAMs. Each requires a different protocol on the L3 interface and a different routing of the L3 clock signals. The type of SRAM is programmed in L3CR[22:23] and the MPC7457 then follows the appropriate protocol for that type. The designer must connect and route the L3 signals appropriately for each type of SRAM. Following are some observations about the L3 interface.

- The routing for the point-to-point signals (L3_CLK[0:1], L3DATA[0:63], L3DP[0:7], and L3_ECHO_CLK[0:3]) to a particular SRAM must be delay matched.
- For 1-Mbyte of SRAM, use L3_ADDR[16:0] (L3_ADDR[0] is LSB)
- For 2-Mbyte of SRAM, use L3_ADDR[17:0] (L3_ADDR[0] is LSB)
- For 4-Mbyte of SRAM, use L3_ADDR[18:0] (L3_ADDR[0] is LSB)
- No pull-up resistors are required for the L3 interface
- For high-speed operations, L3 interface address and control signals should be a ‘T’ with minimal stubs to the two loads; data and clock signals should be point-to-point to their single load. Figure 8 shows the AC test load for the L3 interface.

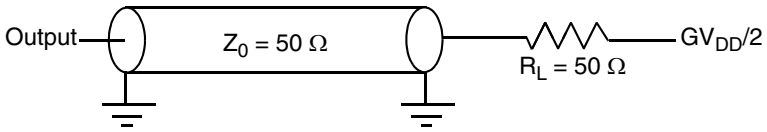


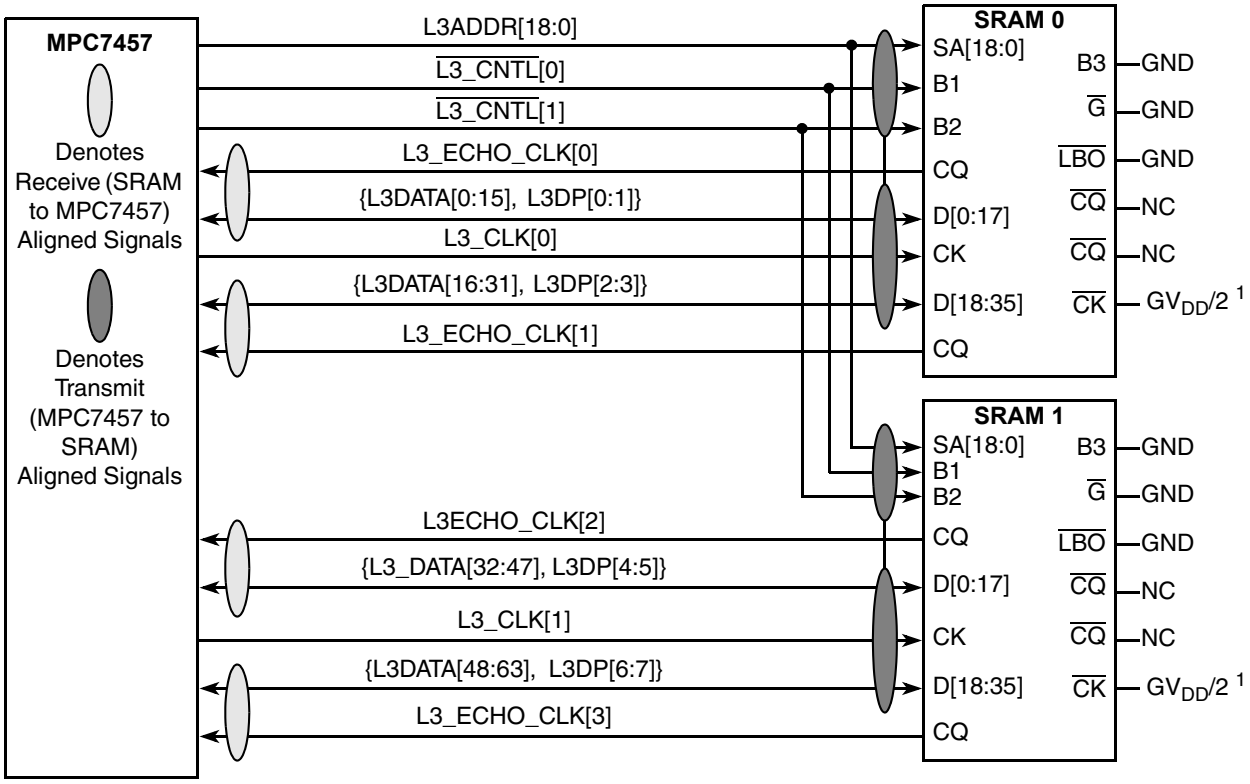
Figure 8. AC Test Load for the L3 Interface

In general, if routing is short, delay-matched, and designed for incident wave reception and minimal reflection, there is a high probability that the AC timing of the MPC7457 L3 interface will meet the maximum frequency operation of appropriately chosen SRAMs. This is despite the pessimistic, guard-banded AC specifications (see Table 12, Table 13, and Table 14), the limitations of functional testers described in Section 5.2.3, “L3 Clock AC Specifications,” and the uncertainty of clocks and signals which inevitably make worst-case critical path timing analysis pessimistic.

More specifically, certain signals within groups should be delay-matched with others in the same group while intergroup routing is less critical. Only the address and control signals are common to both SRAMs and additional timing margin is available for these signals. The double-clocked data signals are grouped with individual clocks as shown in Figure 9 or Figure 11, depending on the type of SRAM. For example, for the MSUG2 DDR SRAM (see Figure 9); L3DATA[0:31], L3DP[0:3], and L3_CLK[0] form a closely coupled group of outputs from the MPC7457; while L3DATA[0:15], L3DP[0:1], and L3_ECHO_CLK[0] form a closely coupled group of inputs.

The *MPC7450 RISC Microprocessor Family User’s Manual* refers to logical settings called ‘sample points’ used in the synchronization of reads from the receive FIFO. The computation of the correct value for this setting is system-dependent and is described in the *MPC7450 RISC Microprocessor Family User’s Manual*. Three specifications are used in this calculation and are given in Table 11. It is essential that all three specifications are included in the calculations to determine the sample points, as incorrect settings can result in errors and unpredictable behavior. For more information, see the *MPC7450 RISC Microprocessor Family User’s Manual.*

Figure 9 shows the typical connection diagram for the MPC7457 interfaced to MSUG2 DDR SRAMs.



Note:

1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 9. Typical Source Synchronous 4-Mbyte L3 Cache DDR Interface

Table 14. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs

At recommended operating conditions. See Table 4.

Parameter	Symbol	All Revisions and L3 I/O Voltage Modes		Unit	Notes
		Min	Max		
L3_CLK rise and fall time	t_{L3CR}, t_{L3CF}	—	0.75	ns	1, 2
Setup times: Data and parity	t_{L3DVEH}	0.1	—	ns	2, 3
Input hold times: Data and parity	t_{L3DXEH}	0.7	—	ns	2, 3
Valid times: Data and parity	t_{L3CHDV}	—	2.5	ns	2, 4, 5
Valid times: All other outputs	t_{L3CHOV}	—	1.8	ns	5
Output hold times: Data and parity	t_{L3CHDX}	1.4	—	ns	2, 4, 5
Output hold times: All other outputs	t_{L3CHOX}	1.0	—	ns	2, 5
L3_CLK to high impedance: Data and parity	t_{L3CHDZ}	—	3.0	ns	2
L3_CLK to high impedance: All other outputs	t_{L3CHOZ}	—	3.0	ns	2

Notes:

1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. Timing behavior and characterization are currently being evaluated.
3. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLK*n* (see Figure 10). Input timings are measured at the pins.
4. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLK*n* to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
5. Assumes default value of L3OHCR. See Section 5.2.4.1, “Effects of L3OHCR Settings on L3 Bus AC Specifications,” for more information.

7 Pinout Listings

Table 16 provides the pinout listing for the MPC7447, 360 CBGA package. Table 17 provides the pinout listing for the MPC7457, 483 CBGA package.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA package.

Table 16. Pinout Listing for the MPC7447, 360 CBGA Package

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	BVSEL	2
$\overline{\text{AACK}}$	R1	Low	Input	BVSEL	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	BVSEL	
$\overline{\text{ARTRY}}$	N2	Low	I/O	BVSEL	3
AV_{DD}	A8	—	Input	N/A	
$\overline{\text{BG}}$	M1	Low	Input	BVSEL	
$\overline{\text{BMODE0}}$	G9	Low	Input	BVSEL	4
$\overline{\text{BMODE1}}$	F8	Low	Input	BVSEL	5
$\overline{\text{BR}}$	D2	Low	Output	BVSEL	
BVSEL	B7	High	Input	BVSEL	1, 6
$\overline{\text{CI}}$	J1	Low	Output	BVSEL	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	BVSEL	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	BVSEL	
CLK_OUT	H2	High	Output	BVSEL	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	BVSEL	
$\overline{\text{DBG}}$	M2	Low	Input	BVSEL	
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	BVSEL	
$\overline{\text{DRDY}}$	R3	Low	Output	BVSEL	7
DTI[0:3]	G1, K1, P1, N1	High	Input	BVSEL	8
EXT_QUAL	A11	High	Input	BVSEL	9
$\overline{\text{GBL}}$	E2	Low	I/O	BVSEL	

Table 17. Pinout Listing for the MPC7457, 483 CBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select [1]	Notes
TDI	E4	High	Input	BVSEL	7
TDO	H1	High	Output	BVSEL	
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL	
TEST[0:5]	B10, H6, H10, D8, F9, F8	—	Input	BVSEL	13
TEST[6]	A9	—	Input	BVSEL	10
TMS	K4	High	Input	BVSEL	7
$\overline{\text{TRST}}$	C1	Low	Input	BVSEL	7, 16
$\overline{\text{TS}}$	P5	Low	I/O	BVSEL	3
TSIZ[0:2]	L1,H3,D1	High	Output	BVSEL	
TT[0:4]	F1, F4, K8, A5, E1	High	I/O	BVSEL	
$\overline{\text{WT}}$	L2	Low	Output	BVSEL	
V_{DD}	J9, J11, J13, J15, K10, K12, K14, L9, L11, L13, L15, M10, M12, M14, N9, N11, N13, N15, P10, P12, P14	—	—	N/A	
VDD_SENSE[0:1]	G11, J8	—	—	N/A	17

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L3 cache controls (L3CTL[0:1]); GV_{DD} supplies power to the L3 cache interface (L3ADDR[0:17], L3DATA[0:63], L3DP[0:7], L3_ECHO_CLK[0:3], and L3_CLK[0:1]) and the L3 control signals $\overline{\text{L3\_CNTL}}$[0:1]; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). For actual recommended value of V_{in} or supply voltages, see Table 4.
2. Unused address pins must be pulled down to GND.
3. These pins require weak pull-up resistors (for example, 4.7 kΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7457 and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull up to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. See Table 3 for bus voltage configuration information. If used, pull-down resistors should be less than 250 Ω.
7. Internal pull up on die.
8. Ignored in 60x bus mode.
9. These signals must be pulled down to GND if unused or if the MPC7457 is in 60x bus mode.
10. These input signals for factory use only and must be pulled down to GND for normal machine operation.
11. Power must be supplied to GV_{DD}, even when the L3 interface is disabled or unused.
12. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
13. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
14. These signals are for factory use only and must be left unconnected for normal machine operation.
15. This pin can externally cause a performance monitor event. Counting of the event is enabled via software.
16. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
17. These pins are internally connected to V_{DD}. They are intended to allow an external device to detect the core voltage level present at the processor core. If unused, they must be connected directly to V_{DD} or left unconnected.

8 Package Description

The following sections provide the package parameters and mechanical dimensions for the CBGA package.

8.1 Package Parameters for the MPC7447, 360 CBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.72 mm
Maximum module height	3.24 mm
Ball diameter	0.89 mm (35 mil)

8.4 Package Parameters for the MPC7457, 483 CBGA or RoHS BGA

The package parameters are as provided in the following list. The package type is 29 × 29 mm, 483 ceramic ball grid array (CBGA).

Package outline	29 × 29 mm
Interconnects	483 (22 × 22 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	—
Maximum module height	3.22 mm
Ball diameter	0.89 mm (35 mil)

Table 18. MPC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts (continued)

PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
11110	PLL off		PLL off, no core clocking occurs							

Notes:
1. PLL_CFG[0:4] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7455; see Section 5.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result is that the processor bus frequency is one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7455 regardless of the SYSCLK input.

9.1.2 L3 Clocks

The MPC7457 generates the clock for the external L3 synchronous data SRAMs by dividing the core clock frequency of the MPC7457. The core-to-L3 frequency divisor for the L3 PLL is selected through the L3_CLK bits of the L3CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC7457 core, and timing analysis of the circuit board routing. Table 19 shows various example L3 clock frequencies that can be obtained for a given set of core frequencies.

Table 19. Sample Core-to-L3 Frequencies [1]

Core Frequency (MHz) [2]	÷2	÷2.5	÷3	÷3.5	÷4	÷4.5	÷5	÷5.5	÷6	÷6.5	÷7	÷7.5	÷8
500	250	200	167	143	125	111	100	91	83	77	71	67	63
533	266	213	178	152	133	118	107	97	89	82	76	71	67
550	275	220	183	157	138	122	110	100	92	85	79	73	69
600	300	240	200	171	150	133	120	109	100	92	86	80	75
650	325	260	217	186	163	144	130	118	108	100	93	87	81
666	333	266	222	190	167	148	133	121	111	102	95	89	83
700	350	280	233	200	175	156	140	127	117	108	100	93	88
733	367	293	244	209	183	163	147	133	122	113	105	98	92
800	400	320	266	230	200	178	160	145	133	123	114	107	100
866	433	347	289	248	217	192	173	157	145	133	124	115	108
933	467	373	311	266	233	207	187	170	156	144	133	124	117
1000	500	400	333	285	250	222	200	182	166	154	143	133	125

9.8.2 Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 29 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 27). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure and is recommended due to the high power dissipation of the MPC7457. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

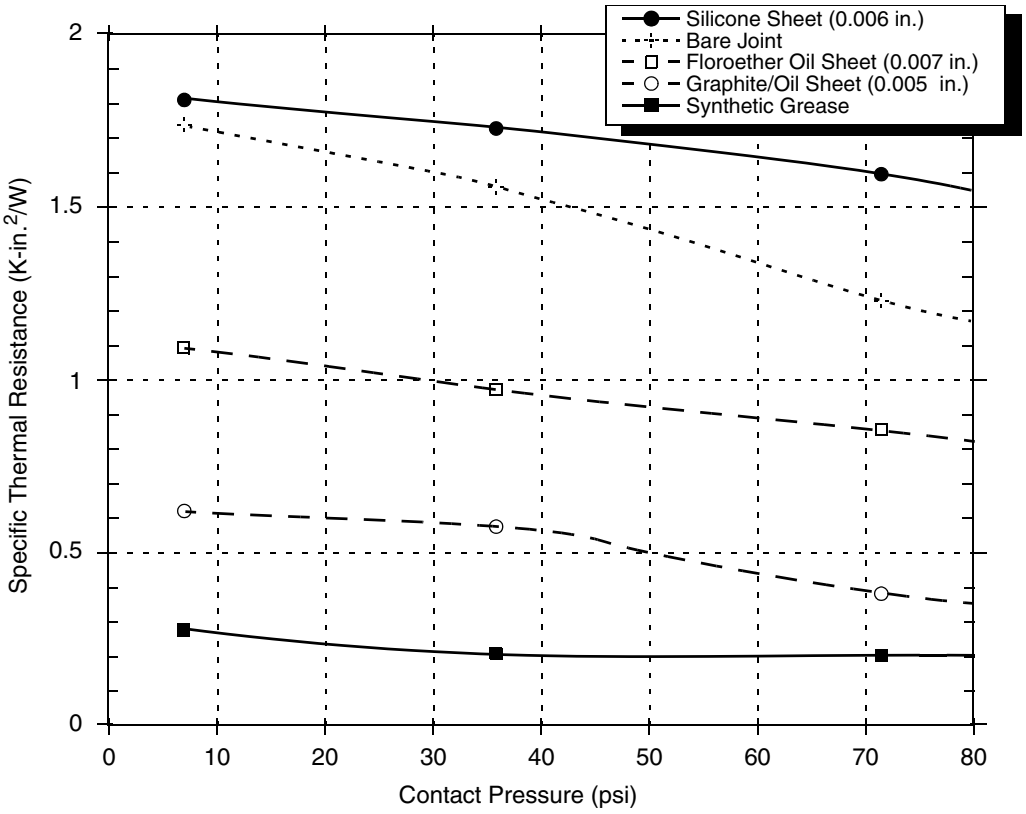


Figure 29. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_I is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5°C/W. For

example, assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 18.7\ W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

For system thermal modeling, the MPC7447 and MPC7457 thermal model is shown in Figure 30. Four volumes will be used to represent this device. Two of the volumes, solder ball, and air and substrate, are modeled using the package outline size of the package. The other two, die, and bump and underfill, have the same size as the die. The silicon die should be modeled 9.64 × 11.0 × 0.74 mm with the heat source applied as a uniform source at the bottom of the volume. The bump and underfill layer is modeled as 9.64 × 11.0 × 0.069 mm (or as a collapsed volume) with orthotropic material properties: 0.6 W/(m • K) in the xy-plane and 2 W/(m • K) in the direction of the z-axis. The substrate volume is 25 × 25 × 1.2 mm (MPC7447) or 29 × 29 × 1.2 mm (MPC7457), and this volume has 18 W/(m • K) isotropic conductivity. The solder ball and air layer is modeled with the same horizontal dimensions as the substrate and is 0.9 mm thick. It can also be modeled as a collapsed volume using orthotropic material properties: 0.034 W/(m • K) in the xy-plane direction and 3.8 W/(m • K) in the direction of the z-axis.

Table 24. Part Numbers Addressed by MPC7457TRX*nnnn*LB Series Hardware Specifications Addendum (Document Order No. MPC7457ECS02AD)

MC	7457	T	RX	*nnnn*	L	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7457	T = Extended Temperature Device	RX = CBGA	1000 1267	L: 1.3 V ± 50 mV –40° to 105°C	C: 1.2; PVR = 8002 0102

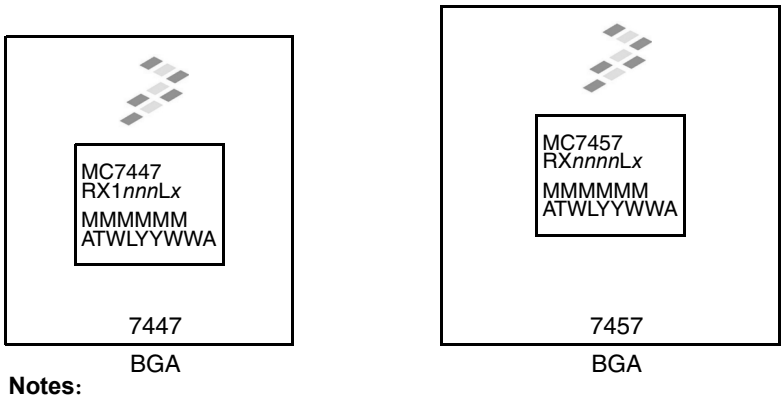
Table 25. Part Numbers Addressed by MPC7457TRX*nnnn*N*x* Series Hardware Specifications Addendum (Document Order No. MPC7457ECS03AD)

MC	74*x*7	T	RX	*nnnn*	N	*x*

Product Code	Part Identifier	Specification Modifier	Package	Processor Frequency	Application Modifier	Revision Level
MC	7447	T = Extended Temperature Device	RX = CBGA	733 1000	N: 1.1 V ± 50 mV –40° to 105°C	B: 1.1; PVR = 8002 0101
	7457					C: 1.2; PVR = 8002 0102

10.3 Part Marking

Parts are marked as the examples shown in Figure 31.



Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.

Figure 31. Part Marking for BGA Device