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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c3012pecr3495

ZiLOG

PRELIMINARY CUSTOMER PROCUREMENT SPECIFICATION

Z86C30/C31/C32/C40

CMOS Z8® CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM (KB)	RAM* (Byte)	Speed (MHz)
Z86C30	4	237	16
Z86C31	2	125	12
Z86C32	2	237	12
Z86C40	4	236	16

* General-Purpose

- 28-Pin DIP, 28-Pin SOIC, 28-Pin PLCC Packages (Z86C3X)
  40-Pin DIP, 44-Pin PLCC/QFP Packages (Z86C40)
- 3.0V to 5.5V Operating Range
- Low-Power Consumption
- –40°C to +105°C Operating Range
- Expanded Register File (ERF)
- 32 Input/Output Lines (C40)
  24 Input/Output Lines (C3X)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer/Power-On Reset
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86C3X/C40 Consumer Controller Processors (CCP) are members of the Z8® single-chip microcontroller family offering a unique register-to-register architecture that avoids accumulator bottlenecks and offers fast execution of code.

Three address spaces (Program Memory, Register File, and Expanded Register File [ERF]), support a wide range of memory configurations. Through the ERF, the designer has access to three additional control registers that provide extra peripheral devices, I/O ports, and register addresses. The rest of the ERF is not physically implemented and is open for future expansion.

For applications demanding powerful I/O capabilities, the Z86C3X/C40's dedicated input and output lines are grouped into three and four ports, respectively, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

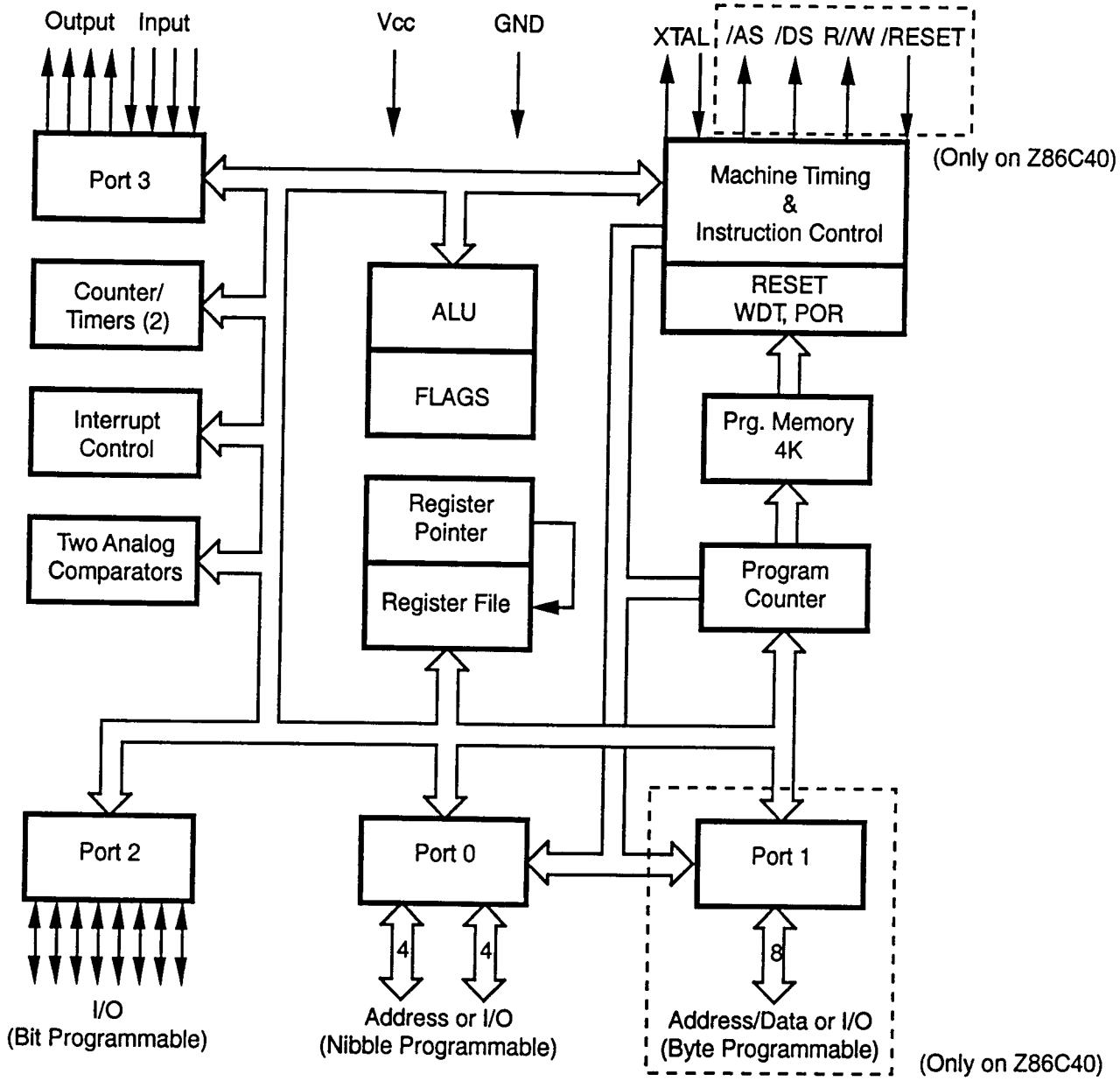
With ROM/ROMless selectivity, the Z86C40 provides both external memory and pre-programmed ROM, which enables these Z8 microcontrollers to be used in high-volume applications, or where code flexibility is required.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

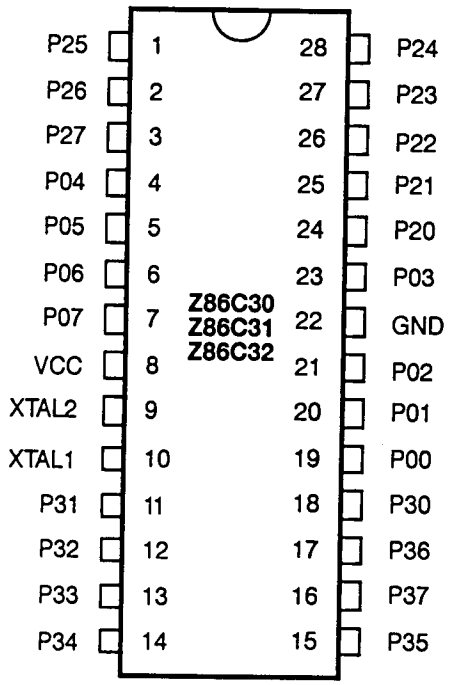
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

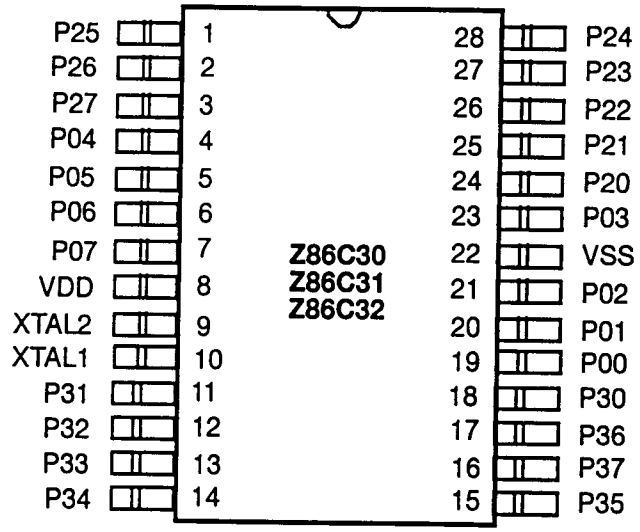
PIN DESCRIPTION



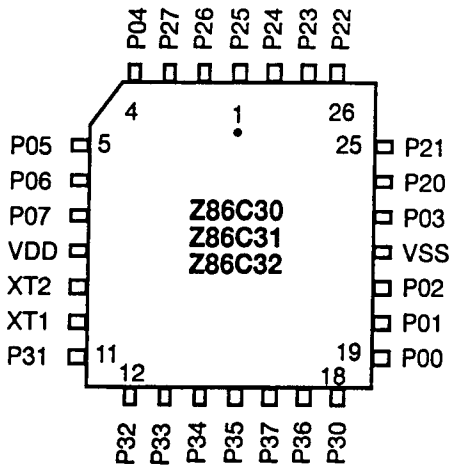
28-Pin DIP Configuration

28-Pin DIP/SOIC/PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-3	P27-25	Port 2, Pins 5,6,7	In/Output
4-7	P07-04	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P33-31	Port 3, Pins 1,2,3	Fixed Input
14-15	P35-4	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P02-00	Port 0, Pins 0,1,2	In/Output
22	GND	Ground, V_{SS}	
23	P03	Port 0, Pin 3	In/Output
24-28	P24-20	Port 2, Pins 0,1,2,3,4	In/Output

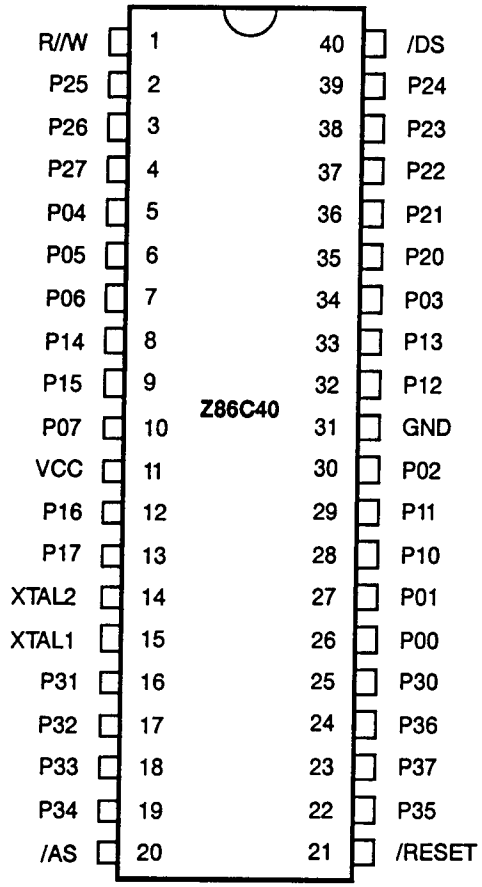


28-Pin SOIC Configuration



28-Pin PLCC Configuration

PIN DESCRIPTION (Continued)

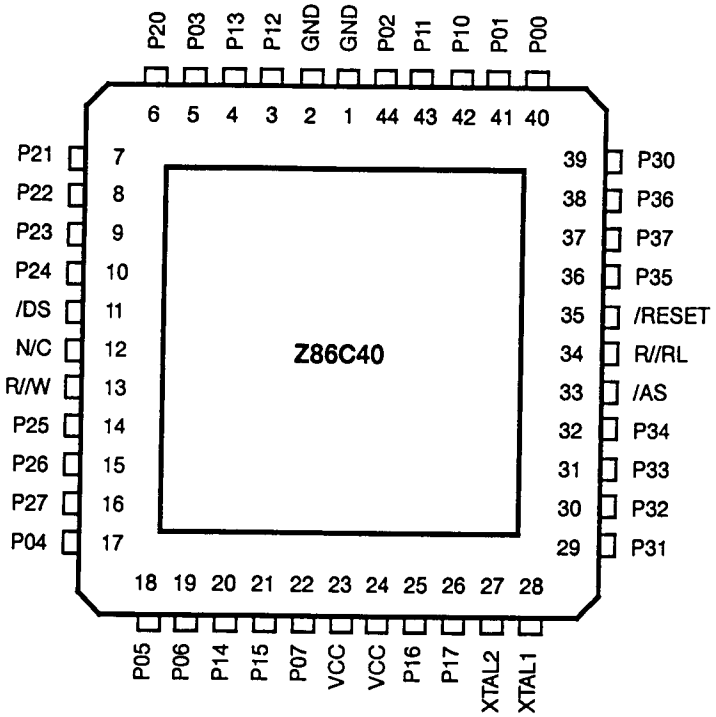


40-Pin DIP Assignments

40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output
2-4	P25-27	Port 2, Pins 5,6,7	In/Output
5-7	P04-06	Port 0, Pins 4,5,6	In/Output
8-9	P14-15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output
15	XTAL1	Crystal, Oscillator Clock	Input
16-18	P31-33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-01	Port 0, Pin 0,1	In/Output
28-29	P10-11	Port 1, Pin 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground, GND	
32-33	P12-13	Port 1, Pin 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-24	Port 2, Pin 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

PIN DESCRIPTION (Continued)

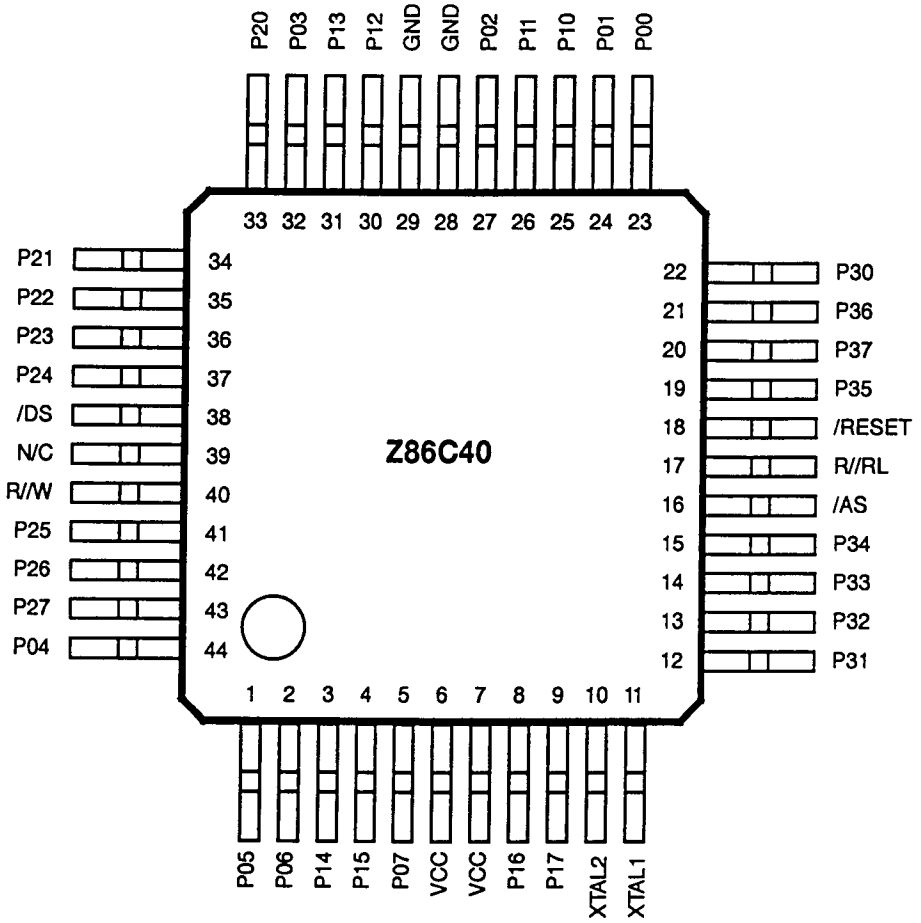


44-Pin PLCC Pin Assignments

44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground, GND	
3-4	P12-13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	N/C	Not Connected	
13	R//W	Read/Write	Output
14-16	P25-27	Port 2, Pins 5,6,7	In/Output
17-19	P04-06	Port 0, Pins 4,5,6	In/Output
20-21	P14-15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23-24	V_{cc}	Power Supply	
25-26	P16-17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal, Oscillator Clock	Output
28	XTAL1	Crystal, Oscillator Clock	Input
29-31	P31-33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless Control	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-01	Port 0, Pins 0,1	In/Output
42-43	P10-11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN DESCRIPTION (Continued)



44-Pin QFP Pin Assignments

44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output
3-4	P14-15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	V_{CC}	Power Supply	
8-9	P16-17	Port 1 Pins 6,7	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output
11	XTAL1	Crystal, Oscillator Clock	Input
12-14	P31-33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless Control	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output

Pin #	Symbol	Function	Direction
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-01	Port 0, Pins 0,1	In/Output
25-26	P10-11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground, GND	
30-31	P12-13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	N/C	Not Connected	
40	R//W	Read/Write	Output
41-43	P25-27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		1.21	W
Maximum Allowable Current out of V_{SS}		220	mA
Maximum Allowable Current into V_{DD}		180	mA
Maximum Allowable Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Allowable Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA

Notes:
[1] This applies to all pins except XTAL pins and where otherwise noted.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes XTAL pins.
[4] Device pin is not at an output Low state.

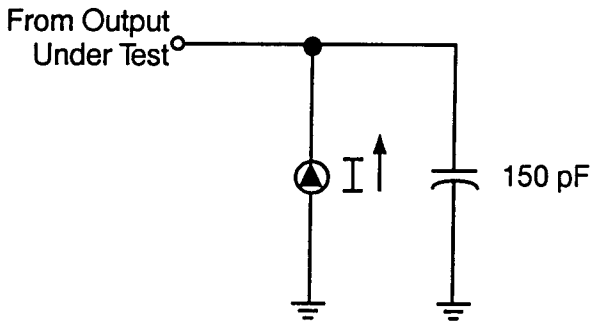
Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH}) \,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH} \,] + \text{sum of } (V_{OL} \times I_{OL})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).



Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltge	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –0.5 mA	
	Low EMI Mode	5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	[8]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	[8]
V_{OL}	Output Low Voltage	3.0V		0.6	0.3	V	I_{OL} = 1.0 mA	
	Low EMI Mode	5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OL} = +4.0 mA	[8]
		5.0V		0.4	0.1	V	I_{OL} = +4.0 mA	[8]
V_{OL2}	Output Low Voltage	3.0V		1.2	0.5	V	I_{OL} = +6 mA	[8]
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	[8]
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	1.5	V		[7]
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		[7]
V_{RL}	Reset Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	1.1			[7]
		5.5V	GND–0.3	0.2 V_{CC}	1.7			[7]
V_{OLR}	Reset Outut Low Voltage	3.0V		0.6	0.3	V	I_{OL} = +1.0 mA	[7]
		5.5V		0.6	0.2	V	I_{OL} = +1.0 mA	[7]
V_{OFFSET}	Comparator Input Offset	3.0V		25	10	mV		
	Voltage	5.5V		25	10	mV		
V_{ICR}	Input Common Mode	3.0V	GND-0.3	V_{CC} –1.0V		V		[10]
	Voltage Range	5.5V	GND-0.3	V_{CC} –1.0V		V		[10]
I_{IL}	Input Leakage	3.0V	–1	2	0.064	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.064	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1	2	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	0.114	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V	–20	–130	–62	µA		
		5.5V	–20	–180	–112	µA		
I_{CC}	Supply Current	3.0V		20	7	mA	@ 16 MHz	[4,5]
		5.5V		25	20	mA	@ 16 MHz	[4,5]
		3.0V		15	5	mA	@ 12 MHz	[4,5]
		5.5V		20	15	mA	@ 12 MHz	[4,5]

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Halt Mode)	3.0V		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		5.5V		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		3.0V		4	1.5	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		5.5V		6	3.2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		3.0V		3.4	1.5	mA	Clock Divide by 16 @ 16 MHz	[4,5]
		5.5V		7.0	2.9	mA	Clock Divide by 16 @ 16 MHz	[4,5]
		3.0V		3	1.2	mA	Clock Divide by 16 @ 12 MHz	[4,5]
		5.5V		5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4,5]
I_{CC2}	Standby Current (Stop Mode)	3.0V		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		5.5V		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		3.0V		500	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	[6,11]
		5.5V		800	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	[6,11]
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	2.4	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V	1.4	15	4.7	µA	$0V < V_{IN} < V_{CC}$	[9]
I_{ALH}	Auto Latch High Current	3.0V	–0.6	–5	–1.8	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V	–1	–8	–3.8	µA	$0V < V_{IN} < V_{CC}$	[9]
T_{POR}	Power On Reset	3.0V	3	24	10	mS		
		5.5V	2.0	13	4	mS		
V_{LV}	Low Voltage Protection		2.05	2.95	2.6	V	6 MHz max INT CLK Freq.	[7]

Note:
[1] Typicals are at V_{CC} = 5.0V and 3.3V.
[2] GND = 0V.
[3] The V_{CC} voltage spec. of 3.0V guarantees 3.3V ± 0.3V and the V_{DD} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1= CL2 = 10 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] Z86C40 only.
[8] STD Mode (not Low-EMI Mode).
[9] Auto Latch (mask option) selected.
[10] For analog comparator inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A=–40°C to 105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –0.5 mA	
	Low EMI Mode	5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage	3.0V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	[8]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	[8]
V_{OL}	Output Low Voltage	3.0V		0.6	0.3	V	I_{OL} = 1.0 mA	
	Low EMI Mode	5.5V		0.4	0.2	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OL} = +4.0 mA	[8]
		5.0V		0.4	0.1	V	I_{OL} = +4.0 mA	[8]
V_{OL2}	Output Low Voltage	3.0V		1.2	0.5	V	I_{OL} = +6 mA	[8]
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	[8]
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	1.5	V		[7]
		5.5V	.8 V_{CC}	V_{CC}	2.1	V		[7]
V_{RL}	Reset Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	1.1			[7]
		5.5V	GND–0.3	0.2 V_{CC}	1.7			[7]
V_{OLR}	Reset Output Low Voltage	3.0V		0.6	0.4	V	I_{OL} = +1.0 mA	[7]
		5.5V		0.6	0.3	V	I_{OL} = +1.0 mA	[7]
V_{OFFSET}	Comparator Input Offset	3.0V		25	10	mV		
	Voltage	5.5V		25	10	mV		
V_{ICR}	Input Common Mode	3.0V	GND–0.3	V_{CC} –1.5V		V		[10]
	Voltage Range	5.5V	GND–0.3	V_{CC} –1.5V		V		[10]
I_{IL}	Input Leakage	3.0V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V	–18	–130	–62	µA		
		5.5V	–18	–180	–112	µA		
I_{CC}	Supply Current	3.0V		20	7	mA	@ 16 MHz	[4,5]
		5.5V		25	20	mA	@ 16 MHz	[4,5]
		3.0V		15	5	mA	@ 12 MHz	[4,5]
		5.5V		20	15	mA	@ 12 MHz	[4,5]

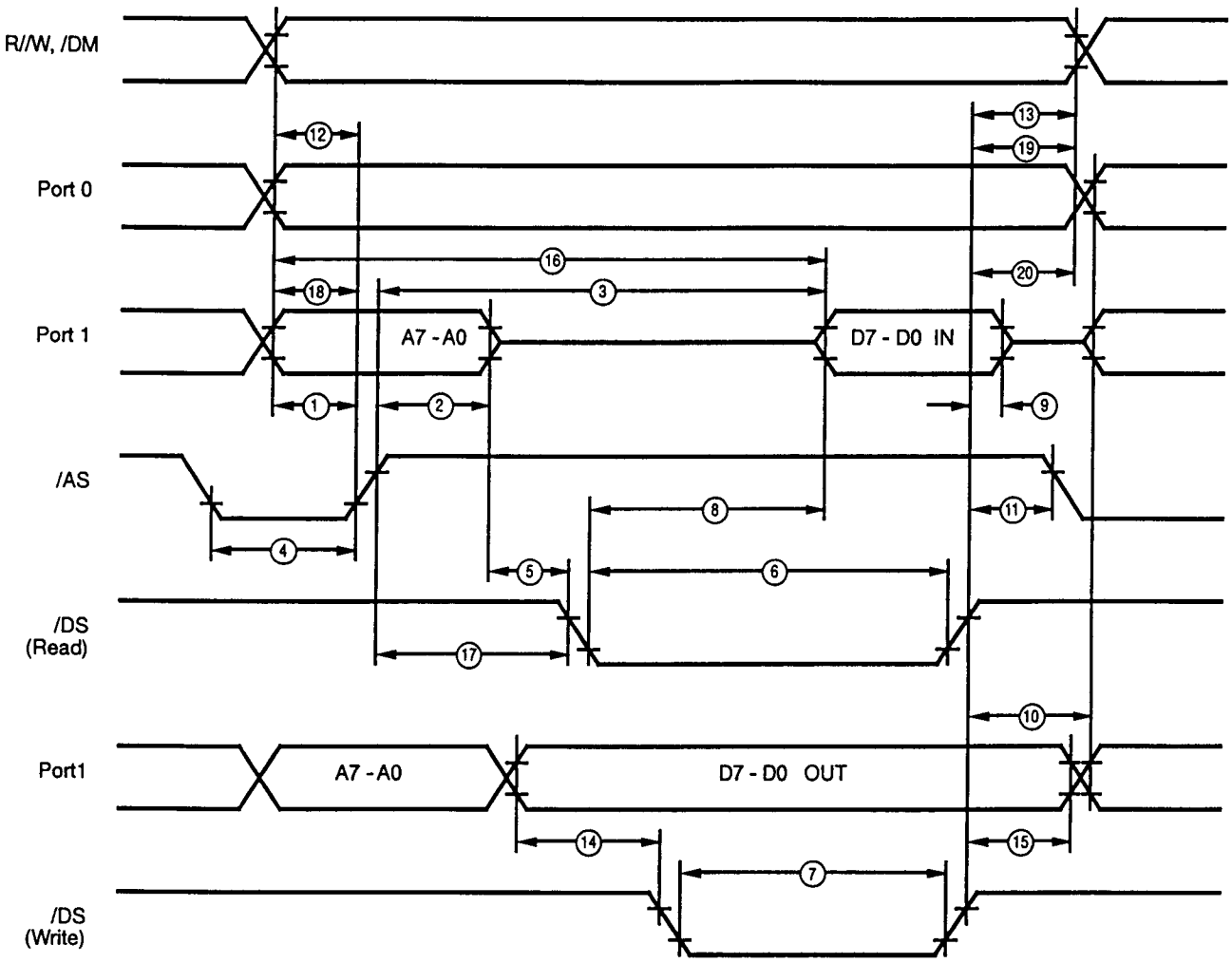
DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} Note [3]	T_A = –40°C to 105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Halt Mode)	3.0V		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		5.5V		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		3.0V		4	1.5	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		5.5V		6	3.2	mA	V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		3.0V		3.4	1.5	mA	Clock Divide by 16 @ 16 MHz	[4,5]
		5.5V		7.0	2.9	mA	Clock Divide by 16 @ 16 MHz	[4,5]
		3.0V		3	1.2	mA	Clock Divide by 16 @ 12 MHz	[4,5]
		5.5V		5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4,5]
I_{CC2}	Standby Current (Stop Mode)	3.0V		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		5.5V		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		3.0V		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	[6,11]
		5.5V		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	[6,11]
I_{ALL}	Auto Latch Low Current	3.0V	0.7	10	2.4	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V	1.4	20	4.7	µA	$0V < V_{IN} < V_{CC}$	[9]
I_{ALH}	Auto Latch High Current	3.0V	–0.6	–7	–1.8	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V	–1.0	–10	–3.8	µA	$0V < V_{IN} < V_{CC}$	[9]
T_{POR}	Power On Reset	3.0V	3.0	25	7	mS		
		5.5V	2.0	14	4	mS		
V_{LV}	Low Voltage Protection		1.8	3.3	2.6	V	4 MHz max INT CLK Freq.	

Note:
[1] Typicals are at V_{CC} = 5.0V and 3.3V.
[2] GND=0V.
[3] The V_{CC} voltage spec. of 3.0V guarantees 3.3V ± 0.3V and the V_{DD} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1= CL2 = 100pF.
[6] Same as note [4] except inputs at V_{CC}.
[[7] Z86C40 only.
[8] STD Mode (not Low EMI Mode).
[9] Auto Latch (mask option) selected.
[10] For analog comparator inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
[7] Z86C40 only.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram (Z86C40 Only)



External I/O or Memory Read/Write Timing
(Z86C40 Only)

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (Z86C40 Only)
(SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3] V_{CC}	T_A=–40°C to 105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A = –40°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		35		25		ns	[2]
			5.5	35		25		35		25		ns	
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		45		35		ns	[2]
			5.5	45		35		45		35		ns	
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	[1,2]
			5.5		250		180		250		180	ns	
4	TwAS	/AS Low Width	3.0	55		40		55		40		ns	[2]
			5.5	55		40		55		40		ns	
5	TdAS(DS)	Address Float to /DS Fall	3.0	0		0		0		0		ns	
			5.5	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.0	200		135		200		135		ns	[1,2]
			5.5	200		135		200		135		ns	
7	TwDSW	/DS (Write) Low Width	3.0	110		80		110		80		ns	[1,2]
			5.5	110		80		110		80		ns	
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	[1,2]
			5.5		150		75		150		75	ns	
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.00	0		0		0		0		ns	[2]
			5.5	0		0		0		0		ns	
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		45		50		ns	[2]
			5.5	55		50		55		50		ns	
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		30		35		ns	[2]
			5.5	45		35		45		55		ns	
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	3.0	45		25		45		25		ns	[2]
			5.5	45		25		45		25		ns	
13	TdDS(R/W)	/DS Rise to R/W Not Valid	3.0	45		35		45		35		ns	[2]
			5.5	45		35		45		35		ns	
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		55		25		ns	[2]
			5.5	55		25		55		25		ns	
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		45		35		ns	[2]
			5.5	45		35		45		35		ns	
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	[1,2]
			5.5		310		230		310		230	ns	
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		65		45		ns	[2]
			5.5	65		45		65		45		ns	
18	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		35		30		ns	[2]
			5.5	35		30		35		30		ns	
19	TdDS(DM)	/DS Rise to DM Valid Delay	3.0	45		35		45		35		ns	
			5.5	45		35		45		35		ns	
20	ThDS(AS)	/DS Valid to Address Valid Hold Time	3.0	45		35		45		35		ns	
			5.5	45		35		45		35		ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

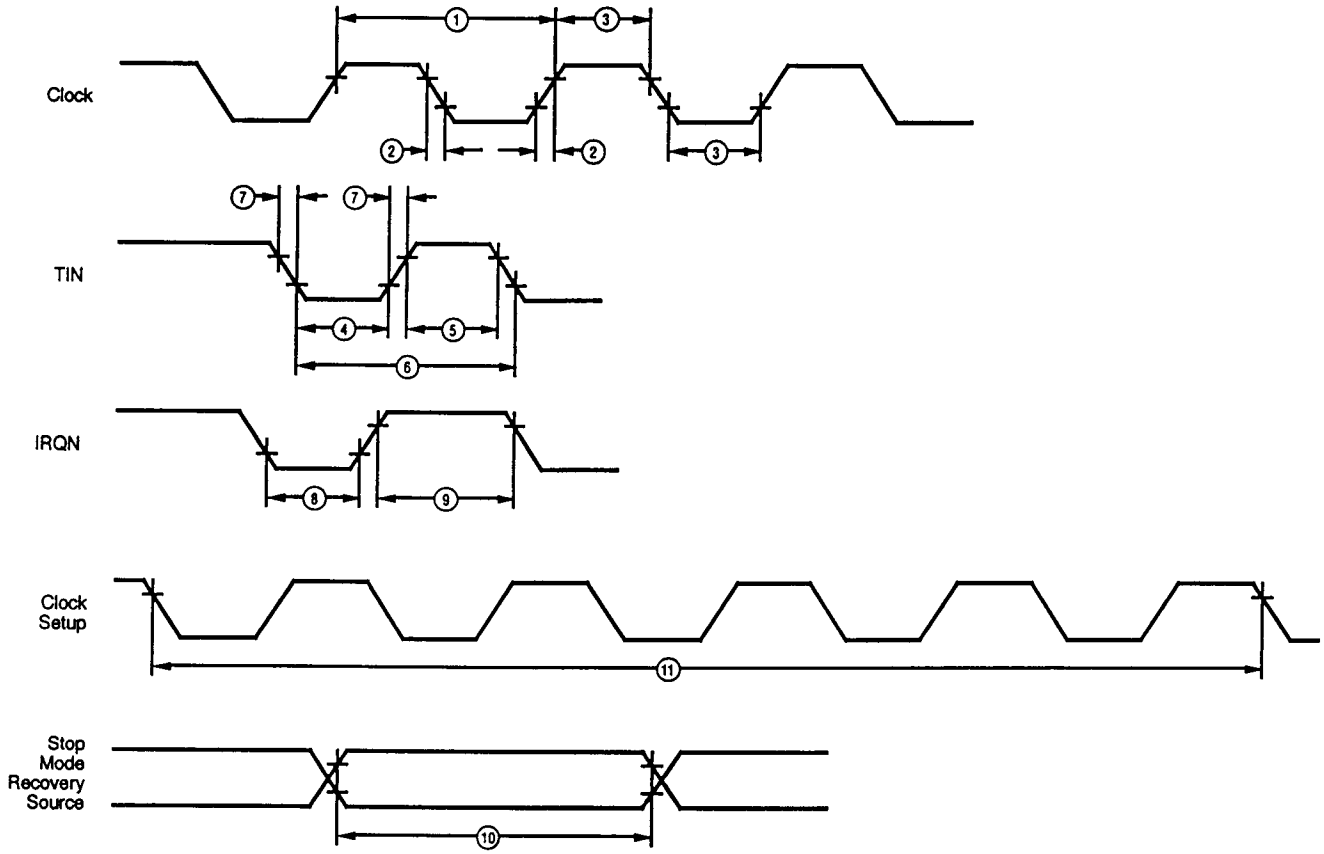
Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode)

				T_A = 0°C to +70°C		T_A = 40°C to +105°C			
			V_{CC}	4 MHz		4 MHz			
No	Symbol	Parameter	Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	100		100		ns	[1,7,8]
			5.5V	100		100		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
			5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC			[1,3,7,8]
			5.5V	5TpC		5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		[4,8,9]
			5.5V		5TpC		5TpC		[4,8,9]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request via Port 3 (P31-P33).

[3] Interrupt request via Port 3 (P30).

[4] SMR-D5 = 1, POR STOP Mode Delay is on.

[5] Reg. WDTMR.

[6] The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

[7] SMR D1 = 0.

[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.

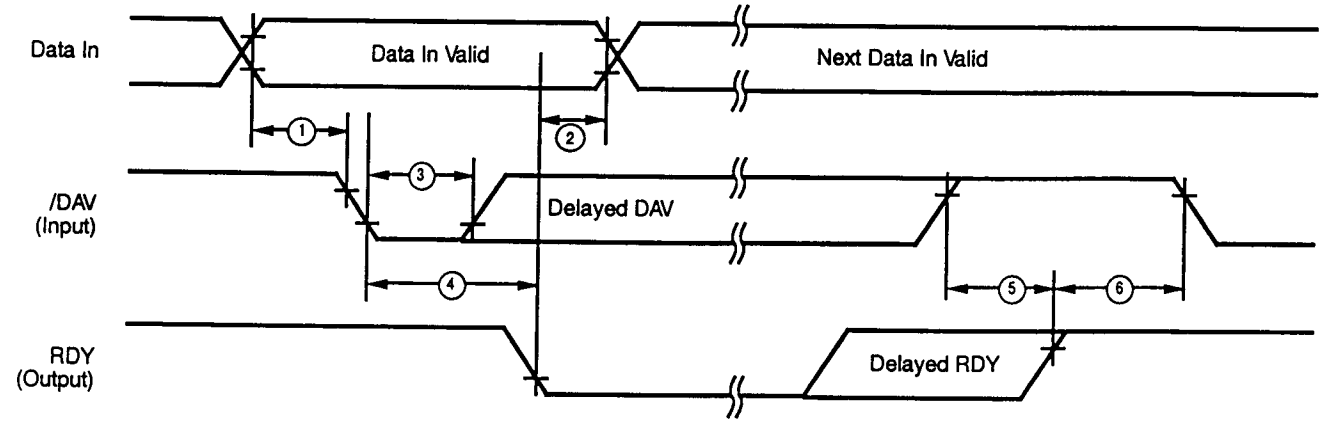
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table

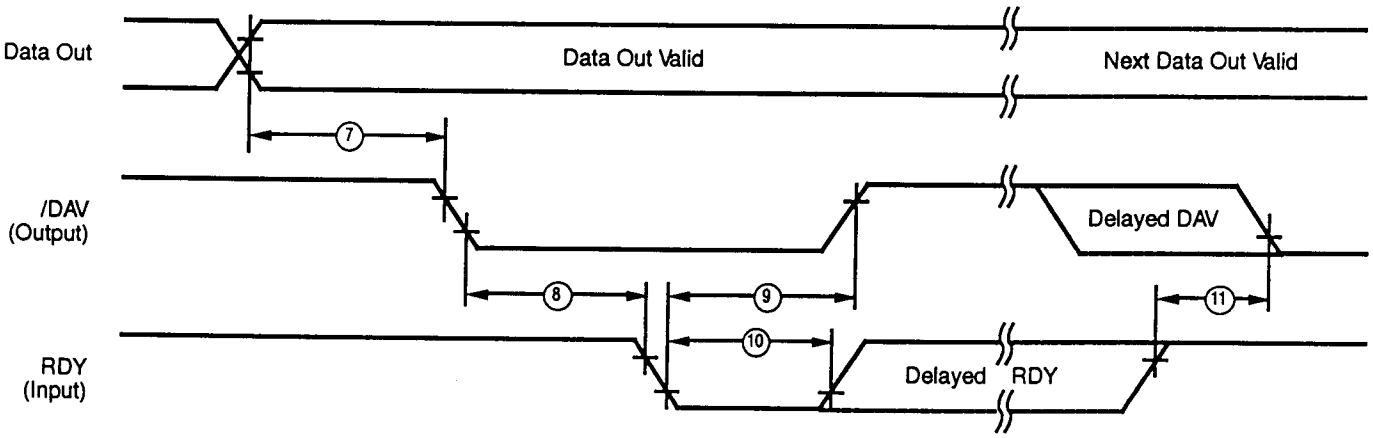
No	Symbol	Parameter	V_{CC} Note [6]	T_A = –40°C to +105°C, T_A = 0°C to +70°C 16 MHz Min	16 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.0V	62.5	DC	83	DC	ns	[1,7,8]
			5.5V	62.5	DC	83	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15	ns	[1,7,8]
			5.5V		15		15	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	31		26		ns	[1,7,8]
			5.5V	31		26		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
			5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC			[1,3,7,8]
			5.5V	5TpC		5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		[4,8]
			5.5V		5TpC		5TpC		[4,8]
12	Twdt	Watch-Dog Timer Delay Time Before Refresh	3.0V	10		10		ms	D0 = 0 [5,11]
			5.5V	5		5.0		ms	D1 = 0 [5,11]
			3.0V	20		20		ms	D0 = 1 [5,11]
			5.5V	10		10		ms	D1 = 0 [5,11]
			3.0V	40		40		ms	D0 = 0 [5,11]
			5.5V	20		20		ms	D1 = 1 [5,11]
			3.0V	160		160		ms	D0 = 1 [5,11]
			5.5V	80		80		ms	D1 = 1 [5,11]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 1, POR STOP Mode Delay is on.
[5] Reg. WDTMR.
[6] The V_{CC} voltage spec. of 3.0V guarantees 3.3V ± 0.3V and the V_{DD} voltage spec. of 5.5V guarantees 5.0V ± 0.5V.
[7] SMR D1 = 0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.
[10] Standard Mode (not Low EMI output ports).
[11] Using internal RC.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

PRECAUTIONS

1. When in ROM Protect Mode, and executing out of *External Program Memory*, instructions LDC, LDCI, LDE, and LDEI *cannot* read Internal Program Memory.

2. When in ROM Protect Mode, and executing out of *Internal Program Memory*, instructions LDC, LDCI, LDE, and LDEI *can* read Internal Program Memory.

3. Low EMI is 25 percent of standard pull-down output driver and 25 percent of standard pull-up output driver.

4. The Port 3 outputs are reset to High State after Reset, except after Stop-Mode Recovery, at which time the outputs remain in the last state.

5. Extended timing is operable.

6. P0/P1/P2/P3 is Low-EMI software programmable.

7. P0/P1/P2 is software programmable for open-drain.

8. Expanded register PCON is Write Only.

9. WDTMR is writeable only within the first 60 system clocks after Reset. Afterward, the WDTMR is write protected.

10. Device functions down to the V_{LV} threshold. At temperatures less than 25°C, the V_{LV} threshold will rise to a maximum V_{DD} of 3.3V.

11. Registers FE Hex (SPH) and FF Hex (SPL) are set to 00 Hex after any reset.

12. When Low EMI OSC is selected (PCON Reg Bit D7=0), the output drive of /DS, /AS, and R/W will also be in low EMI mode.

13. P01M Reg Bit D4,D3 must be set to 00Hex for Z86C30/31/32.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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