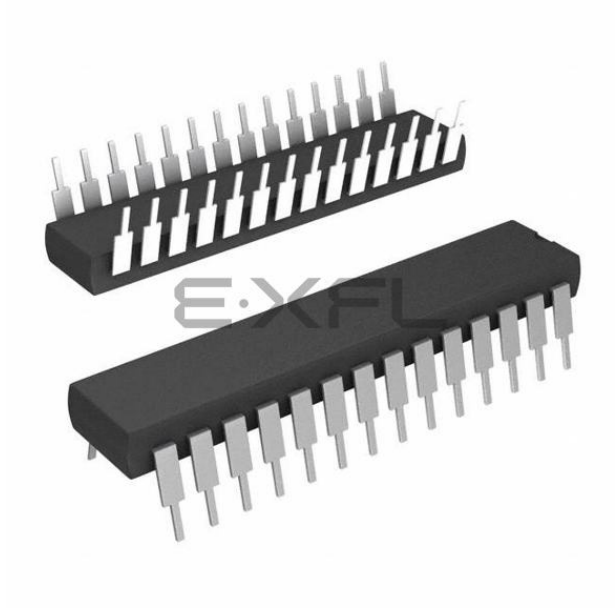

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Table 9 - DRVDEN Mapping

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 10 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

MAIN STATUS REGISTER

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	Reserved	Reserved	DRV1 BUSY	DRV0 BUSY

BIT 0 - 1 DRV x BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DATA REGISTER (FIFO)

Address 3F5 READ/WRITE

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 11 gives several examples of the delays with a FIFO.

The data is based upon the following formula:

$$\text{Threshold \# } x \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 11 - FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps DATA RATE
1 byte	1 x 4 μs - 1.5 μs = 2.5 μs
2 bytes	2 x 4 μs - 1.5 μs = 6.5 μs
8 bytes	8 x 4 μs - 1.5 μs = 30.5 μs
15 bytes	15 x 4 μs - 1.5 μs = 58.5 μs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 μs - 1.5 μs = 6.5 μs
2 bytes	2 x 8 μs - 1.5 μs = 14.5 μs
8 bytes	8 x 8 μs - 1.5 μs = 62.5 μs
15 bytes	15 x 8 μs - 1.5 μs = 118.5 μs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 μs - 1.5 μs = 14.5 μs
2 bytes	2 x 16 μs - 1.5 μs = 30.5 μs
8 bytes	8 x 16 μs - 1.5 μs = 126.5 μs
15 bytes	15 x 16 μs - 1.5 μs = 238.5 μs

DIGITAL INPUT REGISTER (DIR)

Address 3F7 READ ONLY
This register is read-only in all modes.

PC-AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	0	0	0	0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 are read as '0'.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH nDENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 nHIGH DENS
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 - 2 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 - 6 UNDEFINED
Always read as a logic "1"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

Table 14 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 15 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the nPCI_RESET pin, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a nPCI_RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.
On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

nPCI_RESET Pin (Hardware Reset)

The nPCI_RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODES OF OPERATION

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the Interface Mode bits in LD0-CRF0[3,2].

VERIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL/SC ———								
Execution										No data transfer takes place.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

VERSION										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— N ———								Bytes/Sector
	W	——— SC ———								Sectors/Cylinder
	W	——— GPL ———								Gap 3
	W	——— D ———								Filler Byte
Execution for Each Sector Repeat:	W	——— C ———								Input Sector Parameters
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
										FDC formats an entire cylinder
Result	R	——— ST0 ———								Status information after Command execution
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— Undefined ———								
	R	——— Undefined ———								
	R	——— Undefined ———								
	R	——— Undefined ———								

RELATIVE SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———— RCN ————								

DUMPREG									
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	———— PCN-Drive 0 ————								
	R	———— PCN-Drive 1 ————								
	R	———— PCN-Drive 2 ————								
	R	———— PCN-Drive 3 ————								
	R	——— SRT ———				|	—— HUT ——			
	R	———— HLT ————						|	ND
	R	———— SC/EOT ————							
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE
	R	0	EIS	EFIFO	POLL	|	—— FIFOTHR ——		
	R	———— PRETRK ————							

READ ID										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	———— ST0 ————								Status information after Command execution.
	R	———— ST1 ————								Disk status after the Command has completed
	R	———— ST2 ————								
	R	———— C ————								
	R	———— H ————								
	R	———— R ————								
	R	———— N ————								

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	——— Invalid Codes ———								Invalid Command Codes (NoOp - FDC goes into Stand-by State)
Result	R	——— ST0 ———								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

DATA TRANSFER COMMANDS

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it is reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of the TC cycle, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 18). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 18 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 19.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in

Bit 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

Bit 7
This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)
Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5
This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6
This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.
Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
Bit 5 indicates when the XMIT FIFO is empty.
Bit 6 indicates that both the XMIT FIFO and shift register are empty.
Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 30 - Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL[1]	HIGH SPEED BIT[2]
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note[1]: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.
Note [2]: The High Speed bit is located in the Device Configuration Space.

System Interface Pins

Table 49 gives the state of the interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged".

Table 49 – State of System Pins in Auto Powerdown

SYSTEM PINS	STATE IN AUTO POWERDOWN
LAD[3:0]	Unchanged
nLDRQ	Unchanged
nLPCPD	Unchanged
nLFRAME	Unchanged
nPCI_RESET	Unchanged
PCI_CLK	Unchanged
SER_IRQ	Unchanged

FDD Interface Pins

All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED.

Pins used for local logic control or part programming are unaffected. Table 50 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 50 - State of Floppy Disk Drive Interface Pins in Powerdown

FDD PINS	STATE IN AUTO POWERDOWN
INPUT PINS	
nRDATA	Input
nWRTPRT	Input
nTRK0	Input
nINDEX	Input
nDSKCHG	Input
OUTPUT PINS	
nMTR0	Tristated
nDS0	Tristated
nDIR	Active
nSTEP	Active
nWDATA	Tristated
nWGATE	Tristated
nHDSEL	Active
DRVDEN[0:1]	Active

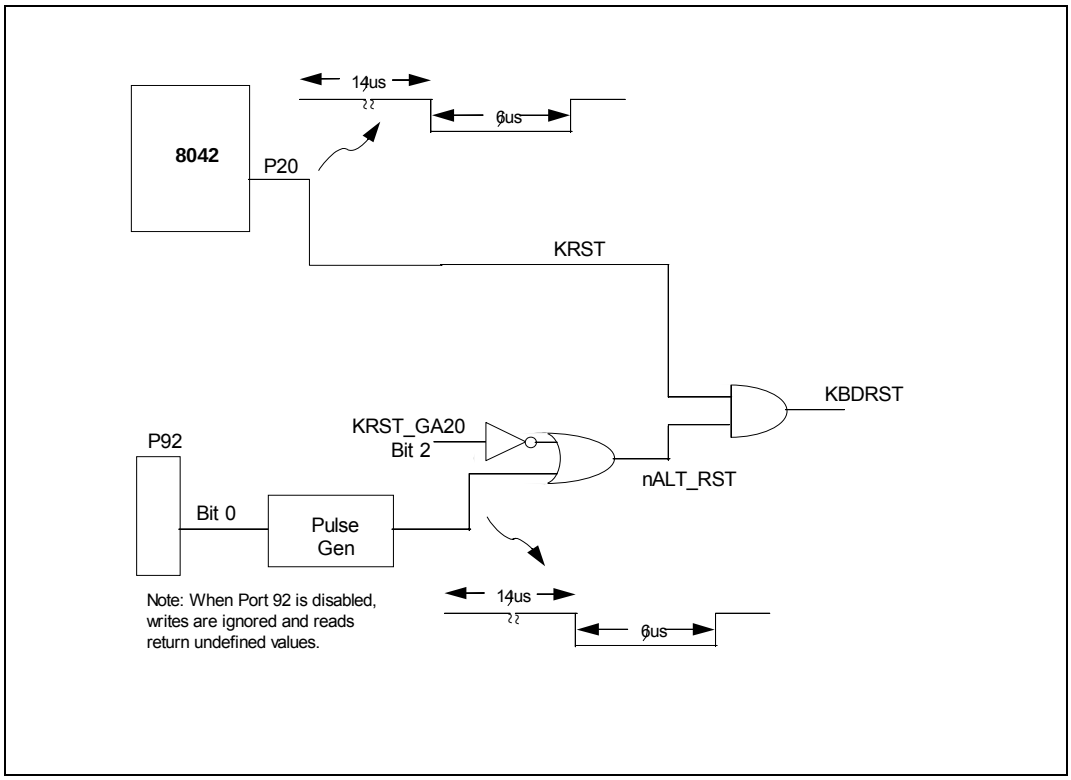
UART Power Management
Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B4 and B5. When set, these bits allow the following auto power management operations:

1. The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2. The receiver enters powerdown when the following conditions are all met:
   A. Receive FIFO is empty
   B. The receiver is waiting for a start bit.

Note: While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

Exit Auto Powerdown
The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.



Bit 1 of Port 92, the ALT_A20 signal, is used to force nA20M to the CPU low for support of real mode compatible software. This signal is externally OR'ed with the A20GATE signal from the keyboard controller and CPURST to control the nA20M input of the CPU. Writing a 0 to bit 1 of the Port 92 Register forces ALT_A20 low. ALT_A20 low drives nA20M to the CPU low, if A20GATE from the keyboard controller is also low. Writing a 1 to bit 1 of the Port 92 Register forces ALT_A20 high. ALT_A20 high drives nA20M to the CPU high, regardless of the state of A20GATE from the keyboard controller. Upon reset, this signal is driven low.

NAME	REG OFFSET (hex)	DESCRIPTION
PME_STS5 Default = 0x00 on VTR POR (Note 6)	08 (R/W)	PME Wake Status Register 5 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
N/A	09 (R)	Reserved – reads return 0
PME_EN1 Default = 0x00 on VTR POR	0A (R/W)	PME Wake Enable Register 1 This register is used to enable individual LPC47M10x PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] Reserved (Note 7) Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] SPEKEY (Wake on specific key) Bit[6] FAN_TACH1 Bit[7] FAN_TACH2 The PME Wake Enable register is not affected by VCC POR, SOFT RESET or HARD RESET.

NAME	REG OFFSET (hex)	DESCRIPTION
GP25 Default = 0x01 on VTR POR	30 (R/W)	General Purpose I/0 bit 2.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=MIDI_IN 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP26 Default = 0x01 on VTR POR	31 (R/W)	General Purpose I/0 bit 2.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=MIDI_OUT 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP27 Default = 0x01 on VTR POR	32 (R/W)	General Purpose I/0 bit 2.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_SMI (Note 5) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP30 Default = 0x01 on VTR POR	33 (R/W)	General Purpose I/0 bit 3.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity :=1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=FAN_TACH2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP31 Default = 0x01 on VTR POR	34 (R/W)	General Purpose I/0 bit 3.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=FAN_TACH1 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

Programming Example

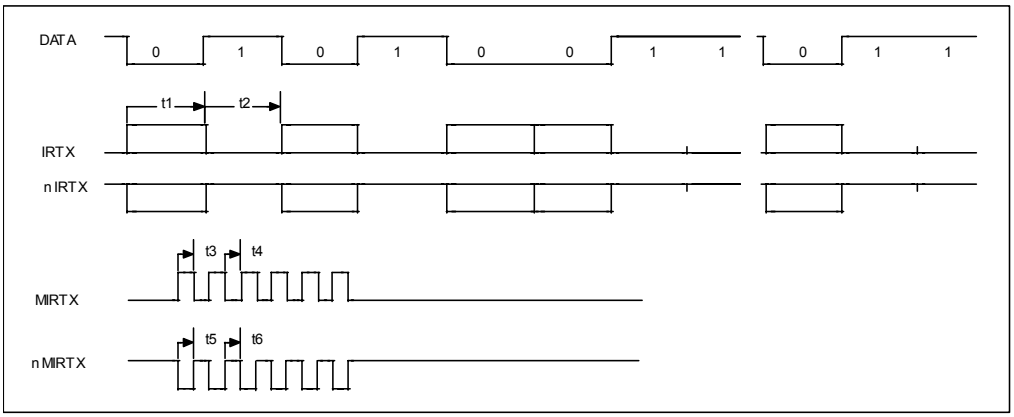
The following is an example of a configuration program in Intel 8086 assembly language.

```
;-----------------------------.
; ENTER CONFIGURATION MODE    |
;-----------------------------'
MOV    DX,02EH
MOV    AX,055H
OUT    DX,AL
;-----------------------------.
; CONFIGURE REGISTER CRE0,    |
; LOGICAL DEVICE 8            |
;-----------------------------'
MOV    DX,02EH
MOV    AL,07H
OUT    DX,AL ;Point to LD# Config Reg
MOV    DX,02FH
MOV    AL, 08H
OUT    DX,AL;Point to Logical Device 8
;
MOV    DX,02EH
MOV    AL,E0H
OUT    DX,AL  ; Point to CRE0
MOV    DX,02fH
MOV    AL,02H
OUT    DX,AL  ; Update CRE0
;-----------------------------.
; EXIT CONFIGURATION MODE     |
;-----------------------------'
MOV    DX,02EH
MOV    AX,0AAH
OUT    DX,AL
```

Notes: HARD RESET: nPCI_RESET pin asserted
SOFT RESET: Bit 0 of Configuration Control register set to one
All host accesses are blocked for 500µs after Vcc POR (see Power-up Timing Diagram)

Table 62 – LPC47M10x Configuration Registers Summary

INDEX	TYPE	HARD RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x59	0x59	0x59	0x59	Device ID - hard wired
0x21	R	0x00	0x00	0x00	0x00	Device Rev - hard wired
0x22	R/W	0x00(Note 1)	0x00(Note 1)	0x00(Note 1)	0x00(Note 1)	Power Control
0x23	R/W	0x00	0x00	0x00	-	Power Mgmt
0x24	R/W	0x44	0x44	0x44	-	OSC
0x26	R/W	Sysopt=0: 0x2E Sysopt=1: 0x4E	Sysopt=0: 0x2E Sysopt=1: 0x4E	-	-	Configuration Port Address Byte 0 (Low Byte)
0x27	R/W	Sysopt=0: 0x00 Sysopt=1: 0x00	Sysopt=0: 0x00 Sysopt=1: 0x00	-	-	Configuration Port Address Byte 1 (High Byte)
0x28	R	-	-	-	-	Reserved
0x2A	R/W	-	0x00	0x00	-	TEST 6
0x2B	R/W	-	0x00	0x00	-	TEST 4



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0
   MIRTX, nMIRTX are the modulated outputs

FIGURE 28 - AMPLITUDE SHIFT KEYED IR TRANSMIT TIMING

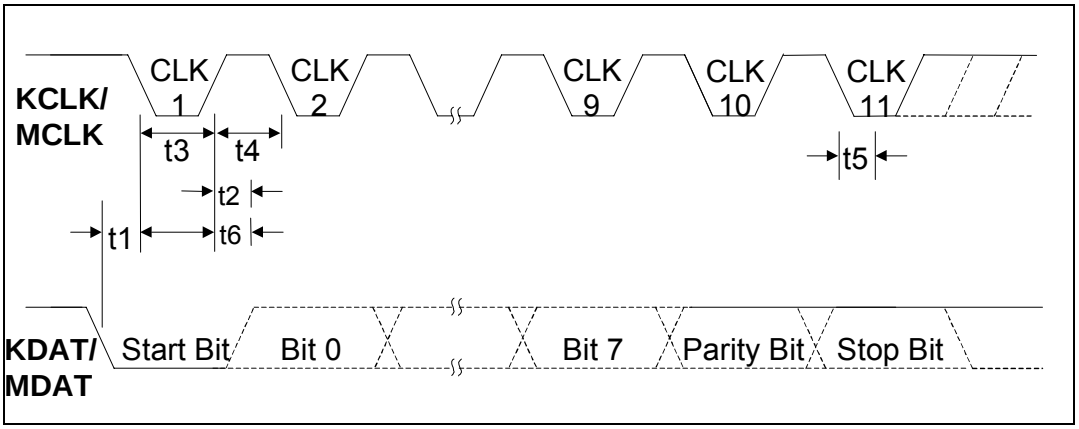


FIGURE 33 – KEYBOARD/MOUSE RECEIVE/SEND DATA TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Time from DATA transition to falling edge of CLOCK (Receive)	5		25	µsec
t2	Time from rising edge of CLOCK to DATA transition (Receive)	5		T4-5	µsec
t3	Duration of CLOCK inactive (Receive/Send)	30		50	µsec
t4	Duration of CLOCK active (Receive/Send)	30		50	µsec
t5	Time to keyboard inhibit after clock 11 to ensure the keyboard does not start another transmission (Receive)	>0		50	µsec
t6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	µsec

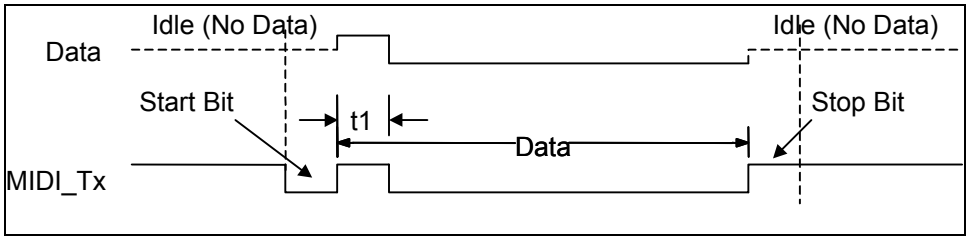


FIGURE 34 – MIDI DATA BYTE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	MIDI Data Bit Time	31.7	32	32.3	µsec

Note: The MIDI bit clock is 31.25kHz +/- 1%

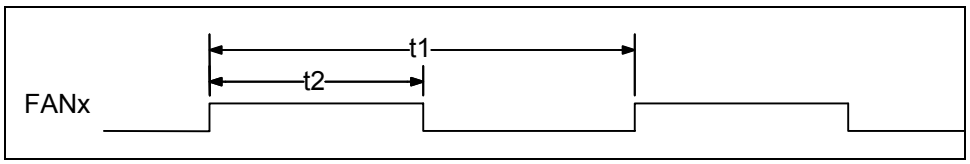


FIGURE 35 – FAN OUTPUT TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PWM Period (Note 1)	0.021		25.5	msec
t2	PWM High Time (Note 2)	0.00033		25.1	msec

Note 1: The period is $1/f_{out}$,where f_{out} is programmed through the FANx and Fan Control registers. The tolerance on f_{out} is +/- 2%.

Note 2: When Bit 0 of the FANx registers is 0, then the duty cycle is programmed through Bits[6:1] of these registers. If Bits[6:1] = “000000” then the FANx pin is low. The duty cycle is programmable through Bits[6:1] to be between 1.56% and 98.44%. When Bit 0 is 1, the FANx pin is high.

TRUTH TABLE 1 - Toggling Inputs In Descending Order

	PIN 100	PIN 99	PIN 98	PIN 97	PIN 96	PIN ...	PIN 1	OUTPUT PIN 52
INITIAL CONFIG	L	L	L	L	L	L	L	L
STEP 1	H	L	L	L	L	L	L	H
STEP 2	H	H	L	L	L	L	L	L
STEP 3	H	H	H	L	L	L	L	H
STEP 4	H	H	H	H	L	L	L	L
STEP 5	H	H	H	H	H	L	L	H
…	…	…	…	…	…	…	…	…
STEP N	H	H	H	H	H	H	L	H
END CONFIG	H	H	H	H	H	H	H	L

TRUTH TABLE 2 - Toggling Inputs In Ascending Order

	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN ...	PIN 100	OUTPUT PIN 52
INITIAL CONFIG	H	H	H	H	H	H	H	L
STEP 1	L	H	H	H	H	H	H	H
STEP 2	L	L	H	H	H	H	H	L
STEP 3	L	L	L	H	H	H	H	H
STEP 4	L	L	L	L	H	H	H	L
STEP 5	L	L	L	L	L	H	H	H
	…	…	…	…	…	…	…	…
STEP N	L	L	L	L	L	L	H	L
END CONFIG	L	L	L	L	L	L	L	L