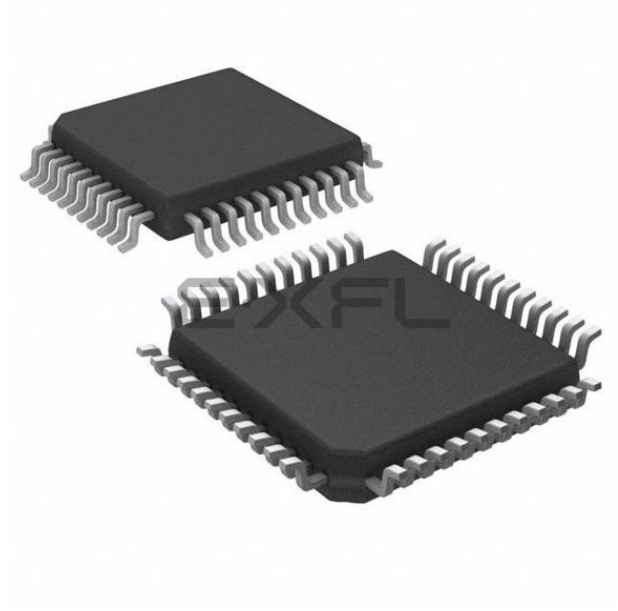

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08gt16cfber

Chapter 2 Pins and Connections

2.1 Introduction

This section describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.

2.2 Device Pin Assignment

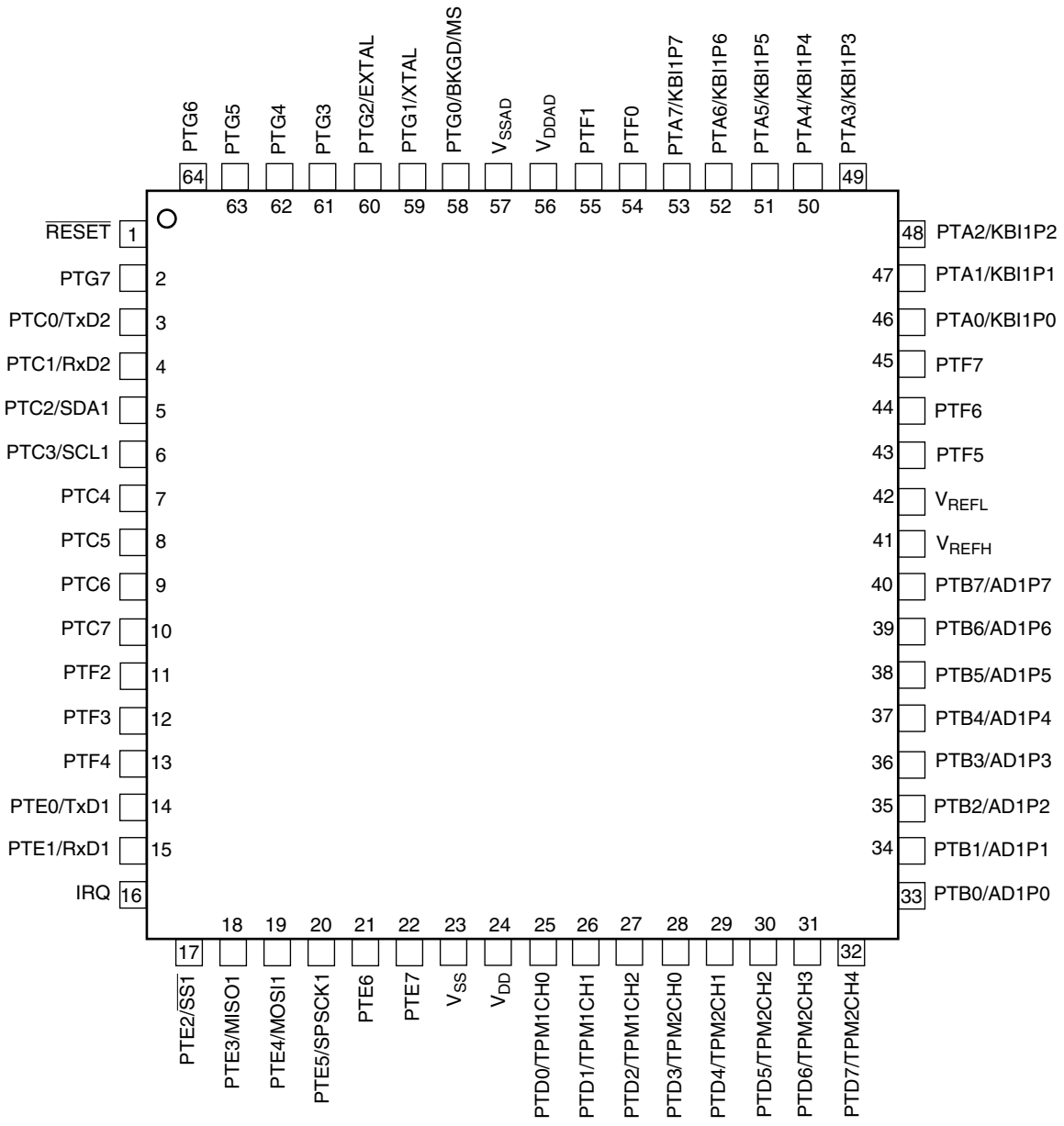


Figure 2-1. MC9S08GBxx in 64-Pin LQFP Package

Table 4-6. FLASH Clock Divider Settings

f_{Bus}	PRDIV8 (Binary)	DIV5:DIV0 (Decimal)	f_{FCLK}	Program/Erase Timing Pulse (5 µs Min, 6.7 µs Max)
20 MHz	1	12	192.3 kHz	5.2 µs
10 MHz	0	49	200 kHz	5 µs
8 MHz	0	39	200 kHz	5 µs
4 MHz	0	19	200 kHz	5 µs
2 MHz	0	9	200 kHz	5 µs
1 MHz	0	4	200 kHz	5 µs
200 kHz	0	0	200 kHz	5 µs
150 kHz	0	0	150 kHz	6.7 µs

4.6.2 FLASH Options Register (FOPT and NVOPT)

During reset, the contents of the nonvolatile location NVOPT are copied from FLASH into FOPT. Bits 5 through 2 are not used and always read 0. This register may be read at any time, but writes have no meaning or effect. To change the value in this register, erase and reprogram the NVOPT location in FLASH memory as usual and then issue a new MCU reset.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	KEYEN	FNORED	0	0	0	0	SEC01	SEC00
Write:								
Reset:	This register is loaded from nonvolatile location NVOPT during reset.							

= Unimplemented or Reserved

Figure 4-5. FLASH Options Register (FOPT)

KEYEN — Backdoor Key Mechanism Enable

When this bit is 0, the backdoor key mechanism cannot be used to disengage security. The backdoor key mechanism is accessible only from user (secured) firmware. BDM commands cannot be used to write key comparison values that would unlock the backdoor key. For more detailed information about the backdoor key mechanism, refer to Section 4.5, "Security."

1 = If user firmware writes an 8-byte value that matches the nonvolatile backdoor key (NVBACKKEY through NVBACKKEY+7, in that order), security is temporarily disengaged until the next MCU reset.

0 = No backdoor key access allowed.

FNORED — Vector Redirection Disable

When this bit is 1, vector redirection is disabled.

1 = Vector redirection disabled.

0 = Vector redirection enabled.

Chapter 5 Resets, Interrupts, and System Configuration

5.1 Introduction

This section discusses basic reset and interrupt mechanisms and the various sources of reset and interrupts in the MC9S08GB/GT. Some interrupt sources from peripheral modules are discussed in greater detail within other sections of this data manual. This section gathers basic information about all reset and interrupt sources in one place for easy reference. A few reset and interrupt sources, including the computer operating properly (COP) watchdog and real-time interrupt (RTI), are not part of on-chip peripheral systems with their own sections but are part of the system control logic.

5.2 Features

Reset and interrupt features include:

- Multiple sources of reset for flexible system configuration and reliable operation:
  - Power-on detection (POR)
  - Low voltage detection (LVD) with enable
  - External $\overline{\text{RESET}}$ pin with enable
  - COP watchdog with enable and two timeout choices
  - Illegal opcode
  - Serial command from a background debug host
- Reset status register (SRS) to indicate source of most recent reset
- Separate interrupt vectors for each module (reduces polling overhead) (see Table 5-1)

5.3 MCU Reset

Resetting the MCU provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector ($FFFE:$FFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with pullup devices disabled. The I bit in the condition code register (CCR) is set to block maskable interrupts so the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to $00FF at reset.

The MC9S08GB/GT has seven sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Computer operating properly (COP) timer
- Illegal opcode detect
- Background debug forced reset
- The reset pin ($\overline{\text{RESET}}$)
- Clock generator loss of lock and loss of clock reset

6.5 Stop Modes

Depending on the stop mode, I/O functions differently as the result of executing a STOP instruction. An explanation of I/O behavior for the various stop modes follows:

- When the MCU enters stop1 mode, all internal registers including general-purpose I/O control and data registers are powered down. All of the general-purpose I/O pins assume their reset state: output buffers and pullups turned off. Upon exit from stop1, all I/O must be initialized as if the MCU had been reset.
- When the MCU enters stop2 mode, the internal registers are powered down as in stop1 but the I/O pin states are latched and held. For example, a port pin that is an output driving low continues to function as an output driving low even though its associated data direction and output data registers are powered down internally. Upon exit from stop2, the pins continue to hold their states until a 1 is written to the PPDACK bit. To avoid discontinuity in the pin state following exit from stop2, the user must restore the port control and data registers to the values they held before entering stop2. These values can be stored in RAM before entering stop2 because the RAM is maintained during stop2.
- In stop3 mode, all I/O is maintained because internal logic circuity stays powered up. Upon recovery, normal I/O function is available to the user.

6.6 Parallel I/O Registers and Control Bits

This section provides information about all registers and control bits associated with the parallel I/O ports.

Refer to tables in Chapter 4, “Memory” for the absolute address assignments for all parallel I/O registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

6.6.1 Port A Registers (PTAD, PTAPE, PTASE, and PTADD)

Port A includes eight pins shared between general-purpose I/O and the KBI module. Port A pins used as general-purpose I/O pins are controlled by the port A data (PTAD), data direction (PTADD), pullup enable (PTAPE), and slew rate control (PTASE) registers.

If the KBI takes control of a port A pin, the corresponding PTASE bit is ignored since the pin functions as an input. As long as PTADD is 0, the PTAPE controls the pullup enable for the KBI function. Reads of PTAD will return the logic value of the corresponding pin, provided PTADD is 0.

PTFPEn — Pullup Enable for Port F Bit n (n = 0–7)

For port F pins that are inputs, these read/write control bits determine whether internal pullup devices are enabled. For port F pins that are configured as outputs, these bits are ignored and the internal pullup devices are disabled.

1 = Internal pullup device enabled.
0 = Internal pullup device disabled.

PTFSEn — Slew Rate Control Enable for Port F Bit n (n = 0–7)

For port F pins that are outputs, these read/write control bits determine whether the slew rate controlled outputs are enabled. For port F pins that are configured as inputs, these bits are ignored.

1 = Slew rate control enabled.
0 = Slew rate control disabled.

PTFDDn — Data Direction for Port F Bit n (n = 0–7)

These read/write bits control the direction of port F pins and what is read for PTFD reads.

1 = Output driver enabled for port F bit n and PTFD reads return the contents of PTFDn.
0 = Input (output driver disabled) and reads return the pin value.

6.6.7 Port G Registers (PTGD, PTGPE, PTGSE, and PTGDD)

Port G includes eight general-purpose I/O pins that are shared with BKGD/MS function and the oscillator or external clock pins. Port G pins used as general-purpose I/O pins are controlled by the port G data (PTGD), data direction (PTGDD), pullup enable (PTGPE), and slew rate control (PTGSE) registers.

Port pin PTG0, while in reset, defaults to the BKGD/MS pin. After the MCU is out of reset, PTG0 can be configured to be a general-purpose output pin. When BKGD/MS takes control of PTG0, the corresponding PTGDD, PTGPE, and PTGPSE bits are ignored.

Port pins PTG1 and PTG2 can be configured to be oscillator or external clock pins. When the oscillator takes control of a port G pin, the corresponding PTGD, PTGDD, PTGSE, and PTGPE bits are ignored.

Reads of PTGD will return the logic value of the corresponding pin, provided PTGDD is 0.

ICGC2 = $30 (%00110000)

Bit 7	LOLRE	0	Generates an interrupt request on loss of lock
Bit 6:4	MFD	011	Sets the MFD multiplication factor to 10
Bit 3	LOCRE	0	Generates an interrupt request on loss of clock
Bit 2:0	RFD	000	Sets the RFD division factor to ÷1

ICGS1 = $xx

This is read only except for clearing interrupt flag

ICGS2 = $xx

This is read only. Should read DCOS before performing any time critical tasks

ICGFLTLU/L = $xx

Not used in this example

ICGTRM

Not used in this example

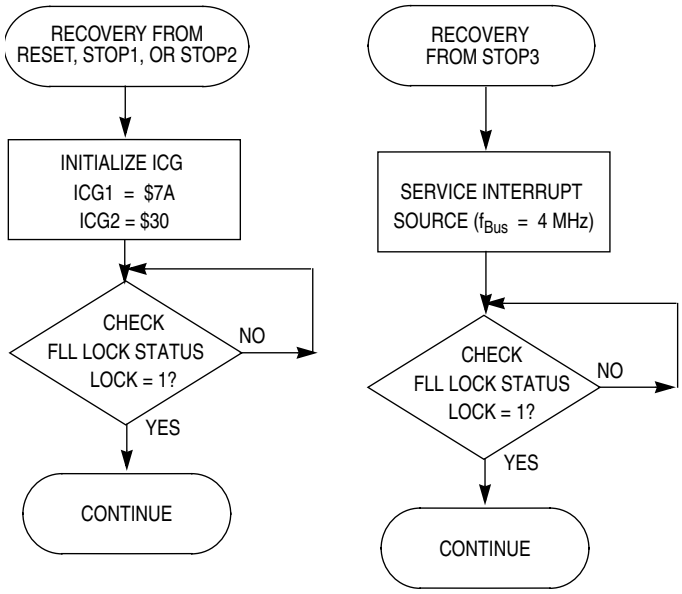


Figure 7-9. ICG Initialization and Stop Recovery for Example #2

7.4.4 Example #3: No External Crystal Connection, 5.4 MHz Bus Frequency

In this example, the FLL will be used (in FEI mode) to multiply the internal 243 kHz (approximate) reference clock up to 10.8 MHz to achieve 5.4 MHz bus frequency. This system will also use the trim function to fine tune the frequency based on an external reference signal.

After the MCU is released from reset, the ICG is in self-clocked mode (SCM) and supplies approximately 8 MHz on ICGOUT which corresponds to a 4 MHz bus frequency (f_{Bus}).

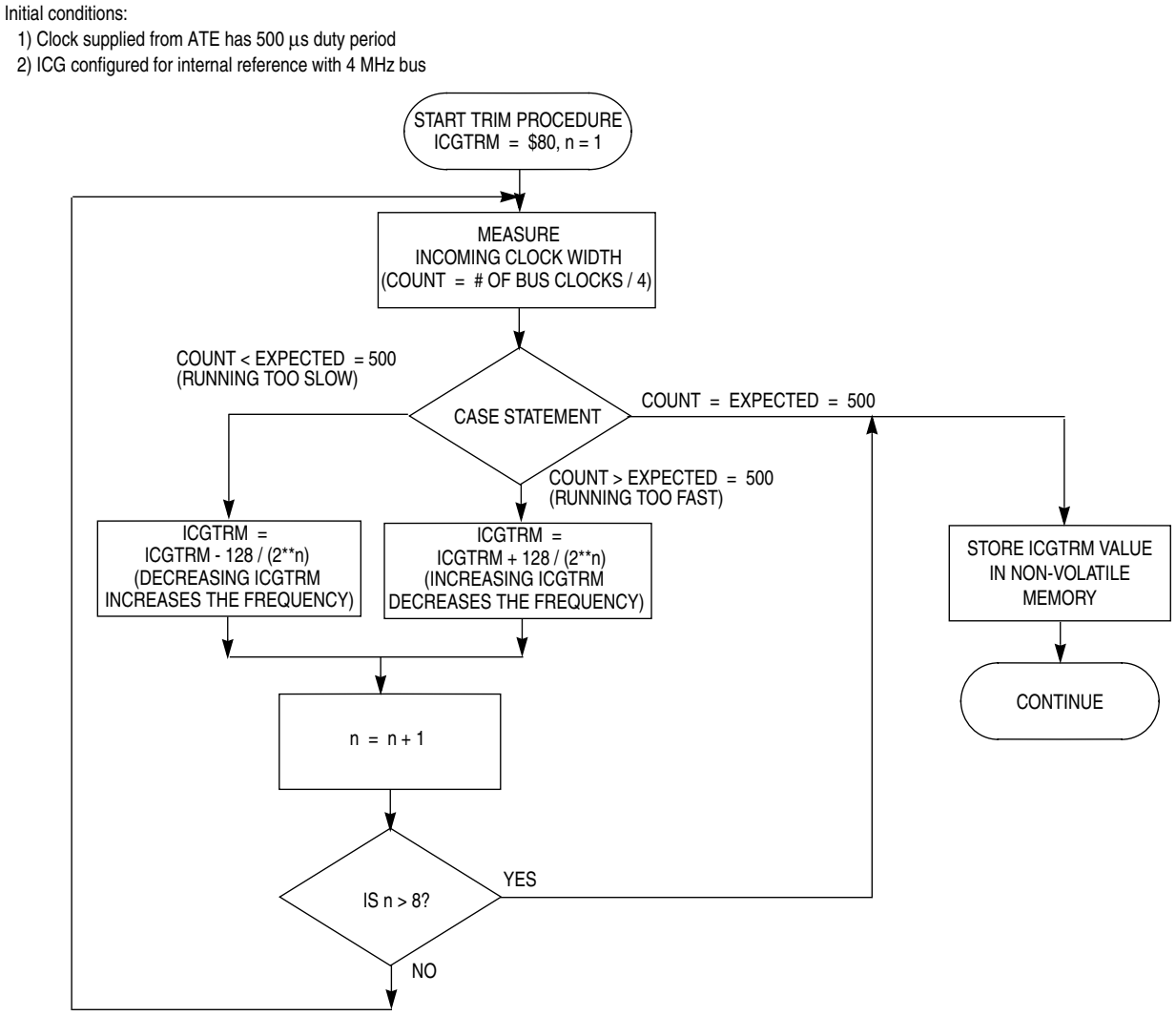


Figure 7-11. Trim Procedure

In this particular case, the MCU has been attached to a PCB and the entire assembly is undergoing final test with automated test equipment. A separate signal or message is provided to the MCU operating under user provided software control. The MCU initiates a trim procedure as outlined in Figure 7-11 while the tester supplies a precision reference signal.

If the intended bus frequency is near the maximum allowed for the device, it is recommended to trim using a reduction divisor (R) twice the final value. Once the trim procedure is complete, the reduction divisor can be restored. This will prevent accidental overshoot of the maximum clock frequency.

7.5 ICG Registers and Control Bits

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all ICG registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

A rising edge is detected when the input signal is seen as a logic 0 during one bus cycle and then a logic 1 during the next cycle.

The KBIMOD control bit can be set to reconfigure the detection logic so that it detects edges and levels. In KBIMOD = 1 mode, the KBF status flag becomes set when an edge is detected (when one or more enabled pins change from the deasserted to the asserted level while all other enabled pins remain at their deasserted levels), but the flag is continuously set (and cannot be cleared) as long as any enabled keyboard input pin remains at the asserted level. When the MCU enters stop mode, the synchronous edge-detection logic is bypassed (because clocks are stopped). In stop mode, KBI inputs act as asynchronous level-sensitive inputs so they can wake the MCU from stop mode.

9.4.3 KBI Interrupt Controls

The KBF status flag becomes set (1) when an edge event has been detected on any KBI input pin. If KBIE = 1 in the KBI1SC register, a hardware interrupt will be requested whenever KBF = 1. The KBF flag is cleared by writing a 1 to the keyboard acknowledge (KBACK) bit.

When KBIMOD = 0 (selecting edge-only operation), KBF is always cleared by writing 1 to KBACK. When KBIMOD = 1 (selecting edge-and-level operation), KBF cannot be cleared as long as any keyboard input is at its asserted level.

9.5 KBI Registers and Control Bits

This section provides information about all registers and control bits associated with the KBI modules.

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all KBI registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

9.5.1 KBI Status and Control Register (KBI1SC)

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	KBEDG7	KBEDG6	KBEDG5	KBEDG4	KBF	0	KBIE	KBIMOD
Write:						KBACK		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-4. KBI Status and Control Register (KBI1SC)

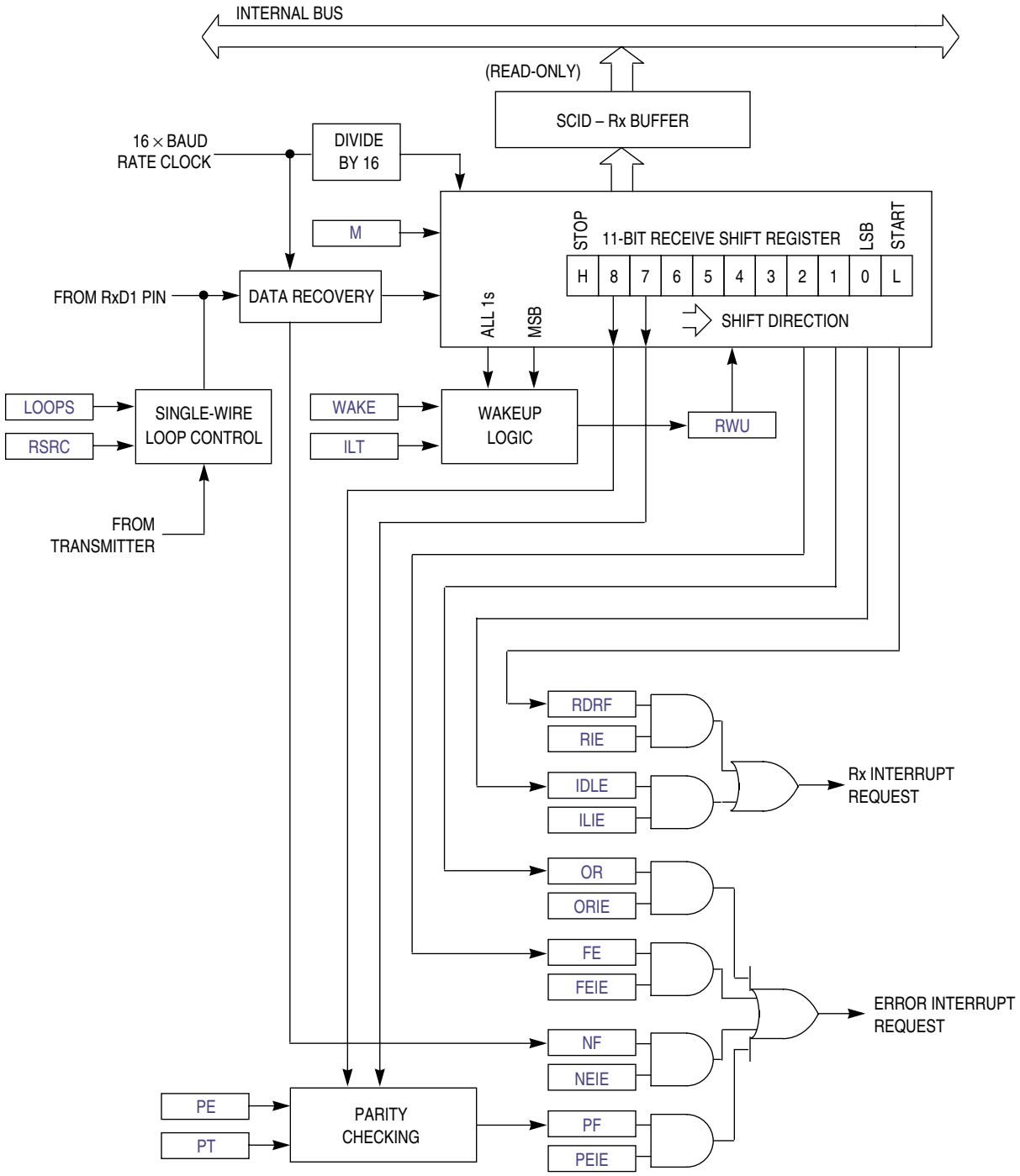


Figure 11-4. SCI Receiver Block Diagram

The receiver is enabled by setting the RE bit in SCIxC2. Character frames consist of a start bit of logic 0, eight (or nine) data bits (LSB first), and a stop bit of logic 1. For information about 9-bit data mode, refer to Section 11.8.1, "8- and 9-Bit Data Modes." For the remainder of this discussion, we assume the SCI is configured for normal 8-bit data mode.

inhibits setting of the status flags associated with the receiver, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force RWU to 0 so all receivers wake up in time to look at the first character(s) of the next message.

11.6.3.1 Idle-Line Wakeup

When WAKE = 0, the receiver is configured for idle-line wakeup. In this mode, RWU is cleared automatically when the receiver detects a full character time of the idle-line level. The M control bit selects 8-bit or 9-bit data mode that determines how many bit times of idle are needed to constitute a full character time (10 or 11 bit times because of the start and stop bits). The idle-line type (ILT) control bit selects one of two ways to detect an idle line. When ILT = 0, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full character time of idle. When ILT = 1, the idle bit counter doesn't start until after a stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

11.6.3.2 Address-Mark Wakeup

When WAKE = 1, the receiver is configured for address-mark wakeup. In this mode, RWU is cleared automatically when the receiver detects a logic 1 in the most significant bit of a received character (eighth bit in M = 0 mode and ninth bit in M = 1 mode).

11.7 Interrupts and Status Flags

The SCI system has three separate interrupt vectors to reduce the amount of software needed to isolate the cause of the interrupt. One interrupt vector is associated with the transmitter for TDRE and TC events. Another interrupt vector is associated with the receiver for RDRF and IDLE events, and a third vector is used for OR, NF, FE, and PF error conditions. Each of these eight interrupt sources can be separately masked by local interrupt enable masks. The flags can still be polled by software when the local masks are cleared to disable generation of hardware interrupt requests.

The SCI transmitter has two status flags that optionally can generate hardware interrupt requests. Transmit data register empty (TDRE) indicates when there is room in the transmit data buffer to write another transmit character to SCIxD. If the transmit interrupt enable (TIE) bit is set, a hardware interrupt will be requested whenever TDRE = 1. Transmit complete (TC) indicates that the transmitter is finished transmitting all data, preamble, and break characters and is idle with TxD1 high. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (TCIE) bit is set, a hardware interrupt will be requested whenever TC = 1. Instead of hardware interrupts, software polling may be used to monitor the TDRE and TC status flags if the corresponding TIE or TCIE local interrupt masks are 0s.

When a program detects that the receive data register is full (RDRF = 1), it gets the data from the receive data register by reading SCIxD. The RDRF flag is cleared by reading SCIxS1 while RDRF = 1 and then reading SCIxD. If the SCI is configured to operate in 9-bit mode, an additional read to the SCIxC3 register is required to clear RDRF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-5. SCI Baud Rate Register (SCIxBDH)

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
Write:								
Reset:	0	0	0	0	0	1	0	0

= Unimplemented or Reserved

Figure 11-6. SCI x Baud Rate Register (SCIxBDL)

SBR12:SBR0 — Baud Rate Modulo Divisor

These 13 bits are referred to collectively as BR, and they set the modulo divide rate for the SCI baud rate generator. When BR = 0, the SCI baud rate generator is disabled to reduce supply current. When BR = 1 to 8191, the SCI baud rate = BUSCLK/(16×BR).

11.10.2 SCI x Control Register 1 (SCIxC1)

This read/write register is used to control various optional features of the SCI system.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 11-7. SCI x Control Register 1 (SCIxC1)

LOOPS — Loop Mode Select

Selects between loop back modes and normal 2-pin full-duplex modes. When LOOPS = 1, the transmitter output is internally connected to the receiver input.

1 = Loop mode or single-wire mode where transmitter outputs are internally connected to receiver input. (See RSRC bit.) RxD1 pin is not used by SCI.

0 = Normal operation — RxD1 and TxD1 use separate pins.

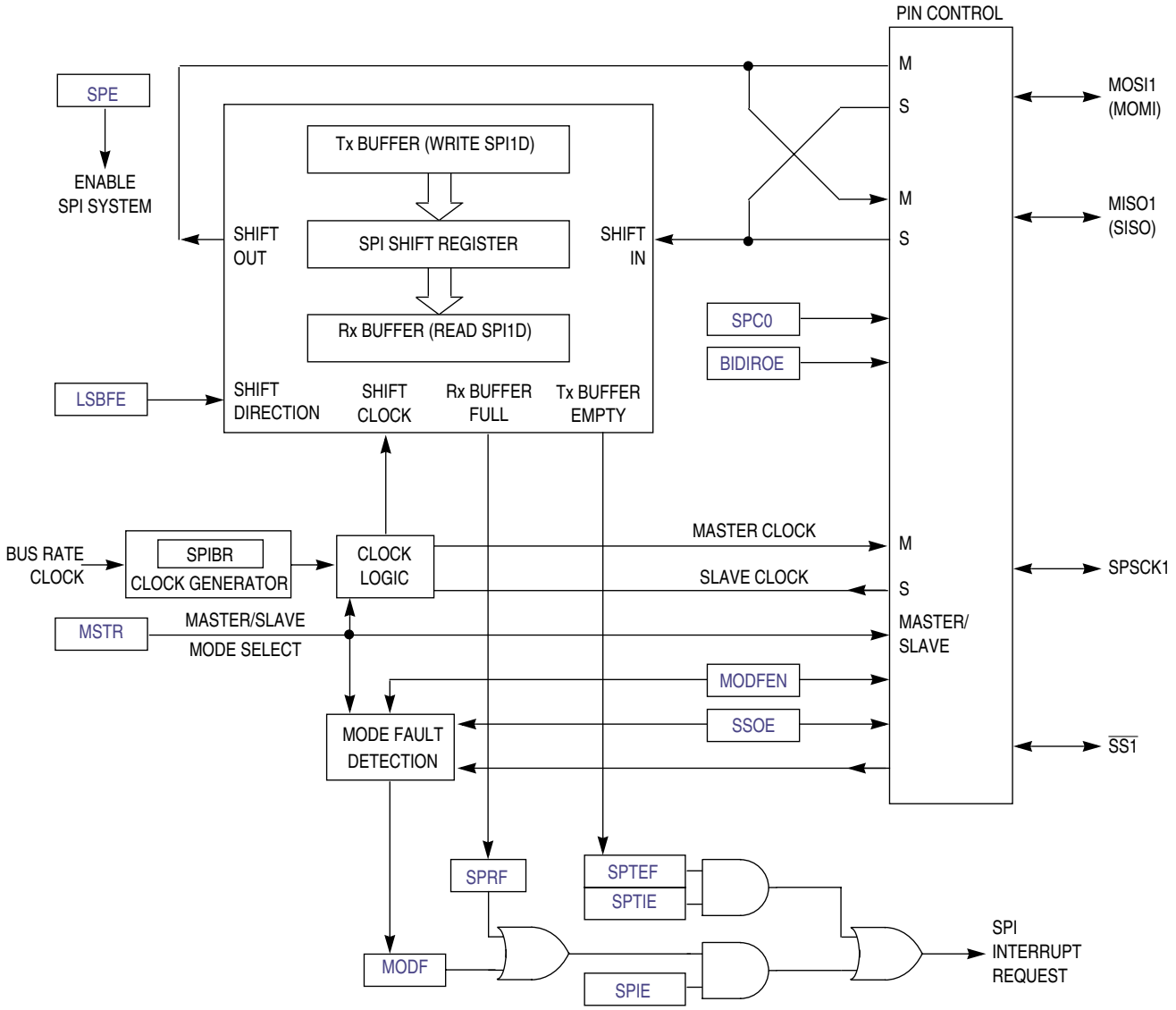


Figure 12-3. SPI Module Block Diagram

12.3.3 SPI Interrupts

There are three flag bits, two interrupt mask bits, and one interrupt vector associated with the SPI system. The SPI interrupt enable mask (SPIE) enables interrupts from the SPI receiver full flag (SPRF) and mode fault flag (MODF). The SPI transmit interrupt enable mask (SPTIE) enables interrupts from the SPI transmit buffer empty flag (SPTEF). When one of the flag bits is set, and the associated interrupt mask bit is set, a hardware interrupt request is sent to the CPU. If the interrupt mask bits are cleared, software can poll the associated flag bits instead of using interrupts. The SPI interrupt service routine (ISR) should check the flag bits to determine what event caused the interrupt. The service routine should also clear the flag bit(s) before returning from the ISR (usually near the beginning of the ISR).

12.3.4 Mode Fault Detection

A mode fault occurs and the mode fault flag (MODF) becomes set when a master SPI device detects an error on the $\overline{SS1}$ pin (provided the $\overline{SS1}$ pin is configured as the mode fault input signal). The $\overline{SS1}$ pin is configured to be the mode fault input signal when MSTR = 1, mode fault enable is set (MODFEN = 1), and slave select output enable is clear (SSOE = 0).

The mode fault detection feature can be used in a system where more than one SPI device might become a master at the same time. The error is detected when a master's $\overline{SS1}$ pin is low, indicating that some other SPI device is trying to address this master as if it were a slave. This could indicate a harmful output driver conflict, so the mode fault logic is designed to disable all SPI output drivers when such an error is detected.

When a mode fault is detected, MODF is set and MSTR is cleared to change the SPI configuration back to slave mode. The output drivers on the SPSCK1, MOSI1, and MISO1 (if not bidirectional mode) are disabled.

MODF is cleared by reading it while it is set, then writing to the SPI control register 1 (SPI1C1). User software should verify the error condition has been corrected before changing the SPI back to master mode.

12.4 SPI Registers and Control Bits

The SPI has five 8-bit registers to select SPI options, control baud rate, report SPI status, and for transmit/receive data.

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all SPI registers. This section refers to registers and control bits only by their names, and a Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

RES8 — ATD Resolution Select

This bit determines the resolution of the ATD converter, 8-bits or 10-bits. The ATD converter has the accuracy of a 10-bit converter. However, if 8-bit compatibility is required, selecting 8-bit resolution will map result data bits 9-2 onto ATD1RH bits 7-0.

The effect of the RES8 bit on the result is shown in Table 14-3.

1 = 8-bit resolution selected.
0 = 10-bit resolution selected.

SGN — Signed Result Select

This bit determines whether the result will be signed or unsigned data. Signed data is represented as 2's complement data and is achieved by complementing the MSB of the result. Signed data mode can be used only when the result is left justified (DJM = 0) and is not available for right-justified mode (DJM = 1). When a signed result is selected, the range for conversions becomes –512 ($200) to 511 ($1FF) for 10-bit resolution and –128 ($80) to 127 ($7F) for 8-bit resolution.

The effect of the SGN bit on the result is shown in Table 14-3.

1 = Left justified result data is signed.
0 = Left justified result data is unsigned.

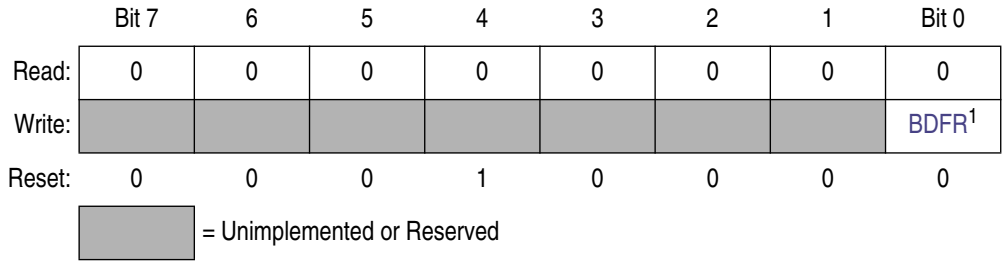
Table 14-3. Available Result Data Formats

RES8	DJM	SGN	Data Formats of Result	Analog Input $V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$ ATD1RH:ATD1RL	
				V_{DDA}	V_{SSA}
1	0	0	8-bit : left justified : unsigned	$FF:$00	$00:$00
1	0	1	8-bit : left justified : signed	$7F:$00	$80:$00
1	1	X[1]	8-bit : left justified[2] : unsigned	$FF:$00	$00:$00
0	0	0	10-bit : left justified : unsigned	$FF:$C0	$00:$00
0	0	1	10-bit : left justified : signed	$7F:$C0	$80:$00
0	1	X[1]	10-bit : right justified : unsigned	$03:$FF	$00:$00

1 The SGN bit is only effective when DJM = 0. When DJM = 1, SGN is ignored.
2 8-bit results are always in ATD1RH.

PRS — Prescaler Rate Select

This field of bits determines the prescaled factor for the ATD conversion clock. Table 14-4 illustrates the divide-by operation and the appropriate range of bus clock frequencies.



1 BDFR is writable only through serial active background mode debug commands, not from user programs.

Figure 15-6. System Background Debug Force Reset Register (SBDFR)

BDFR — Background Debug Force Reset

A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

15.5.3 DBG Registers and Control Bits

The debug module includes nine bytes of register space for three 16-bit registers and three 8-bit control and status registers. These registers are located in the high register space of the normal memory map so they are accessible to normal application programs. These registers are rarely if ever accessed by normal user application programs with the possible exception of a ROM patching mechanism that uses the breakpoint logic.

15.5.3.1 Debug Comparator A High Register (DBGCAH)

This register contains compare value bits for the high-order eight bits of comparator A. This register is forced to $00 at reset and can be read at any time or written at any time unless ARM = 1.

15.5.3.2 Debug Comparator A Low Register (DBGCAL)

This register contains compare value bits for the low-order eight bits of comparator A. This register is forced to $00 at reset and can be read at any time or written at any time unless ARM = 1.

15.5.3.3 Debug Comparator B High Register (DBGCBH)

This register contains compare value bits for the high-order eight bits of comparator B. This register is forced to $00 at reset and can be read at any time or written at any time unless ARM = 1.

15.5.3.4 Debug Comparator B Low Register (DBGCBL)

This register contains compare value bits for the low-order eight bits of comparator B. This register is forced to $00 at reset and can be read at any time or written at any time unless ARM = 1.

15.5.3.7 Debug Control Register (DBGC)

This register can be read or written at any time.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DBGEN	ARM	TAG	BRKEN	RWA	RWAEN	RWB	RWBEN
Reset:	0	0	0	0	0	0	0	0

Figure 15-7. Debug Control Register (DBGC)

DBGEN — Debug Module Enable

Used to enable the debug module. DBGEN cannot be set to 1 if the MCU is secure.
1 = DBG enabled.
0 = DBG disabled.

ARM — Arm Control

Controls whether the debugger is comparing and storing information in the FIFO. A write is used to set this bit (and the ARMF bit) and completion of a debug run automatically clears it. Any debug run can be manually stopped by writing 0 to ARM or to DBGEN.
1 = Debugger armed.
0 = Debugger not armed.

TAG — Tag/Force Select

Controls whether break requests to the CPU will be tag or force type requests. If BRKEN = 0, this bit has no meaning or effect.
1 = CPU breaks requested as tag type requests.
0 = CPU breaks requested as force type requests.

BRKEN — Break Enable

Controls whether a trigger event will generate a break request to the CPU. Trigger events can cause information to be stored in the FIFO without generating a break request to the CPU. For an end trace, CPU break requests are issued to the CPU when the comparator(s) and R/W meet the trigger requirements. For a begin trace, CPU break requests are issued when the FIFO becomes full. TRGSEL does not affect the timing of CPU break requests.
1 = Triggers cause a break request to the CPU.
0 = CPU break requests not enabled.

RWA — R/W Comparison Value for Comparator A

When RWAEN = 1, this bit determines whether a read or a write access qualifies comparator A. When RWAEN = 0, RWA and the R/W signal do not affect comparator A.
1 = Comparator A can only match on a read cycle.
0 = Comparator A can only match on a write cycle.

A.7 ATD Characteristics

Table A-6. ATD Electrical Characteristics (Operating)

Num	Characteristic	Condition	Symbol	Min	Typical	Max	Unit
1	ATD supply[1]		V_{DDAD}	1.80	—	3.6	V
2	ATD supply current	Enabled	$I_{DDADrun}$	—	0.7	1.2	mA
		Disabled (ATDPU = 0 or STOP)	$I_{DDADstop}$	—	0.02	0.6	µA
3	Differential supply voltage	V_{DD}–V_{DDAD}	$\lvert V_{DDLT}\rvert$	—	—	100	mV
4	Differential ground voltage	V_{SS}–V_{SSAD}	$\lvert V_{SDLT}\rvert$	—	—	100	mV
5	Reference potential, low		$\lvert V_{REFL}\rvert$	—	—	V_{SSAD}	V
	Reference potential, high	2.08V ≤ V_{DDAD} ≤ 3.6V	V_{REFH}	2.08	—	V_{DDAD}	V
		1.80V ≤ V_{DDAD} < 2.08V		V_{DDAD}	—	V_{DDAD}	
6	Reference supply current (V_{REFH} to V_{REFL})	Enabled	I_{REF}	—	200	300	µA
		Disabled (ATDPU = 0 or STOP)	I_{REF}	—	<0.01	0.02	
7	Analog input voltage[2]		V_{INDC}	V_{SSAD} – 0.3	—	V_{DDAD} + 0.3	V

1 V_{DDAD} must be at same potential as V_{DD}.
2 Maximum electrical operating range, not valid conversion range.