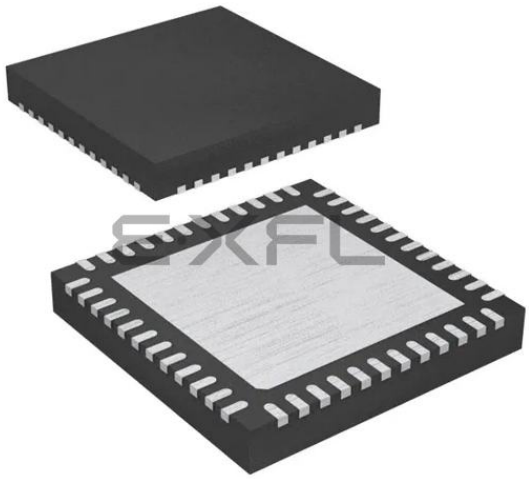

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08gt16cfder

Chapter 12
Serial Peripheral Interface (SPI) Module

- Multiple clock source options:
  - Internally generated clock with ±0.2% trimming resolution and ±0.5% deviation across voltage.
  - Crystal
  - Resonator, or
  - External clock
- Inter-integrated circuit bus module to operate up to 100 kbps (IIC)
- One 3-channel and one 5-channel 16-bit timer/pulse width modulator (TPM) modules with selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels (TPMx).
- 8-pin keyboard interrupt module (KBI)
- 16 high-current pins (limited by package dissipation)
- Software selectable pullups on ports when used as input. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullup on $\overline{\text{RESET}}$ and IRQ pin to reduce customer system cost
- Up to 56 general-purpose input/output (I/O) pins, depending on package selection
- 64-pin low-profile quad flat package (LQFP) — MC9S08GBxx
- 48-pin quad flat package, no lead (QFN) — MC9S08GTxx
- 44-pin quad flat package (QFP) — MC9S08GTxx
- 42-pin shrink dual in-line package (SDIP) — MC9S08GTxx

1.2.3 Devices in the MC9S08GB/GT Series

Table 1-1 lists the devices available in the MC9S08GB/GT series and summarizes the differences among them.

Table 1-1. Devices in the MC9S08GB/GT Series

Device	FLASH	RAM	TPM	I/O	Packages
MC9S08GB60	60K	4K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GB32	32K	2K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GT60	60K	4K	Two 2-channel, 16-bit timers	39 36 34	48 QFN[1] 44 QFP 42 SDIP
MC9S08GT32	32K	2K	Two 2-channel, 16-bit timers	39 36 34	48 QFN[(1)] 44 QFP 42 SDIP
MC9S08GT16	16K	1K	Two 2-channel, 16-bit timers	39 36 34	48 QFN[(1)] 44 QFP 42 SDIP

1 The 48-pin QFN package has one 3-channel and one 2-channel 16-bit TPM.

Chapter 5 Resets, Interrupts, and System Configuration

5.1 Introduction

This section discusses basic reset and interrupt mechanisms and the various sources of reset and interrupts in the MC9S08GB/GT. Some interrupt sources from peripheral modules are discussed in greater detail within other sections of this data manual. This section gathers basic information about all reset and interrupt sources in one place for easy reference. A few reset and interrupt sources, including the computer operating properly (COP) watchdog and real-time interrupt (RTI), are not part of on-chip peripheral systems with their own sections but are part of the system control logic.

5.2 Features

Reset and interrupt features include:

- Multiple sources of reset for flexible system configuration and reliable operation:
  - Power-on detection (POR)
  - Low voltage detection (LVD) with enable
  - External $\overline{\text{RESET}}$ pin with enable
  - COP watchdog with enable and two timeout choices
  - Illegal opcode
  - Serial command from a background debug host
- Reset status register (SRS) to indicate source of most recent reset
- Separate interrupt vectors for each module (reduces polling overhead) (see Table 5-1)

5.3 MCU Reset

Resetting the MCU provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector ($FFFE:$FFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with pullup devices disabled. The I bit in the condition code register (CCR) is set to block maskable interrupts so the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to $00FF at reset.

The MC9S08GB/GT has seven sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Computer operating properly (COP) timer
- Illegal opcode detect
- Background debug forced reset
- The reset pin ($\overline{\text{RESET}}$)
- Clock generator loss of lock and loss of clock reset

PTASEn — Slew Rate Control Enable for Port A Bit n (n = 0–7)

For port A pins that are outputs, these read/write control bits determine whether the slew rate controlled outputs are enabled. For port A pins that are configured as inputs, these bits are ignored.

1 = Slew rate control enabled.

0 = Slew rate control disabled.

PTADDn — Data Direction for Port A Bit n (n = 0–7)

These read/write bits control the direction of port A pins and what is read for PTAD reads.

1 = Output driver enabled for port A bit n and PTAD reads return the contents of PTADn.

0 = Input (output driver disabled) and reads return the pin value.

6.6.2 Port B Registers (PTBD, PTBPE, PTBSE, and PTBDD)

Port B includes eight general-purpose I/O pins that share with the ATD function. Port B pins used as general-purpose I/O pins are controlled by the port B data (PTBD), data direction (PTBDD), pullup enable (PTBPE), and slew rate control (PTBSE) registers.

If the ATD takes control of a port B pin, the corresponding PTBDD, PTBSE, and PTBPE bits are ignored. When a port B pin is being used as an ATD pin, reads of PTBD will return a 0 of the corresponding pin, provided PTBDD is 0.

PTBD

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTBD7	PTBD6	PTBD5	PTBD4	PTBD3	PTBD2	PTBD1	PTBD0
Reset:	0	0	0	0	0	0	0	0

PTBPE

Read: Write:	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
Reset:	0	0	0	0	0	0	0	0

PTBSE

Read: Write:	PTBSE7	PTBSE6	PTBSE5	PTBSE4	PTBSE3	PTBSE2	PTBSE1	PTBSE0
Reset:	0	0	0	0	0	0	0	0

PTBDD

Read: Write:	PTBDD7	PTBDD6	PTBDD5	PTBDD4	PTBDD3	PTBDD2	PTBDD1	PTBDD0
Reset:	0	0	0	0	0	0	0	0

Figure 6-10. Port B Registers

- **Frequency-locked loop** — A frequency-locked loop (FLL) stage takes either the internal or external clock source and multiplies it to a higher frequency. Status bits provide information when the circuit has achieved lock and when it falls out of lock. Additionally, this block can monitor the external reference clock and signals whether the clock is valid or not.
- **Clock select block** — The clock select block provides several switch options for connecting different clock sources to the system clock tree. ICGDCLK is the multiplied clock frequency out of the FLL, ICGERCLK is the reference clock frequency from the crystal or external clock source, and FFE (fixed frequency enable) is a control signal used to control the system fixed frequency clock (XCLK). ICGLCLK is the clock source for the background debug controller (BDC).

The module is intended to be very user friendly with many of the features occurring automatically without user intervention. To quickly configure the module, go to Section 7.4, "Initialization/Application Information," and pick an example that best suits the application needs.

7.1.1 Features

Features of the ICG and clock distribution system:

- Several options for the primary clock source allow a wide range of cost, frequency, and precision choices:
  - 32 kHz–100 kHz crystal or resonator
  - 1 MHz–16 MHz crystal or resonator
  - External clock
  - Internal reference generator
- Defaults to self-clocked mode to minimize startup delays
- Frequency-locked loop (FLL) generates 8 MHz to 40 MHz (for bus rates up to 20 MHz)
  - Uses external or internal clock as reference frequency
- Automatic lockout of non-running clock sources
- Reset or interrupt on loss of clock or loss of FLL lock
- Digitally-controlled oscillator (DCO) preserves previous frequency settings, allowing fast frequency lock when recovering from stop3 mode
- DCO will maintain operating frequency during a loss or removal of reference clock
- Post-FLL divider selects 1 of 8 bus rate divisors (/1 through /128)
- Separate self-clocked source for real-time interrupt
- Trimmable internal clock source supports SCI communications without additional external components
- Automatic FLL engagement after lock is acquired

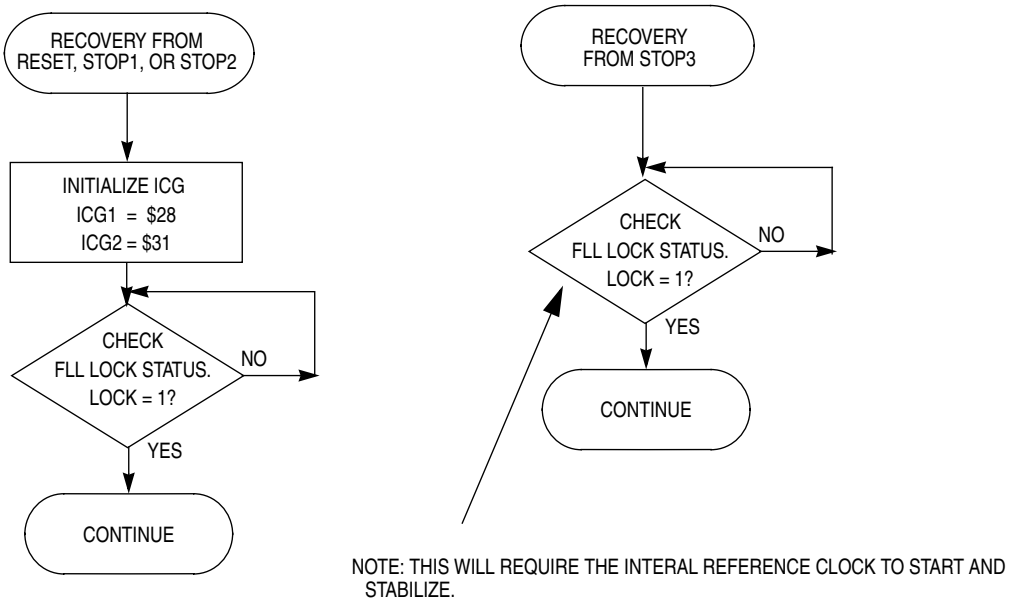


Figure 7-10. ICG Initialization and Stop Recovery for Example #3

7.4.5 Example #4: Internal Clock Generator Trim

The internally generated clock source is guaranteed to have a period ± 25% of the nominal value. In some case this may be sufficient accuracy. For other applications that require a tight frequency tolerance, a trimming procedure is provided that will allow a very accurate source. This section outlines one example of trimming the internal oscillator. Many other possible trimming procedures are valid and can be used.

Table 7-9. CLKST Clock Mode Status

CLKST[1:0]	Clock Status
00	Self-clocked
01	FLL engaged, internal reference
10	FLL bypassed, external reference
11	FLL engaged, external reference

REFST — Reference Clock Status

The REFST bit indicates which clock reference is currently selected by the Reference Select circuit.

1 = Crystal/Resonator selected.
0 = External Clock selected.

LOLS — FLL Loss of Lock Status

The LOLS bit is an indication of FLL lock status. If LOLS is set, it remains set until cleared by software or an MCU reset.

1 = FLL has unexpectedly lost lock since LOLS was last cleared, LOLRE determines action taken.
0 = FLL has not unexpectedly lost lock since LOLS was last cleared.

LOCK — FLL Lock Status

The LOCK bit indicates whether the FLL has acquired lock. The LOCK bit is cleared in off, self-clocked, and FLL bypassed modes.

1 = FLL is currently locked.
0 = FLL is currently unlocked.

LOCS — Loss Of Clock Status

The LOCS bit is an indication of ICG loss of clock status. If LOCS is set, it remains set until cleared by software on an MCU reset.

1 = ICG has lost clock since LOCS was last cleared, LOCRE determines action taken.
0 = ICG has not lost clock since LOCS was last cleared.

ERCS — External Reference Clock Status

The ERCS bit is an indication of whether or not the external reference clock (ICGERCLK) meets the minimum frequency requirement.

1 = External reference clock is stable, frequency requirement is met.
0 = External reference clock is not stable, frequency requirement is not met.

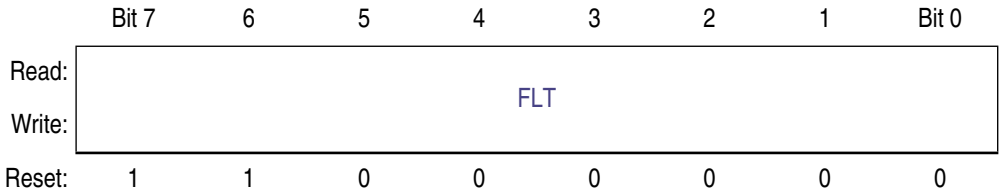


Figure 7-18. ICG Lower Filter Register (ICGFLTL)

The filter registers show the filter value (FLT).

FLT — Filter Value

The FLT bits indicate the current filter value, which controls the DCO frequency. The FLT bits are read only except when the CLKS bits are programmed to self-clocked mode (CLKS = 00). In self-clocked mode, any write to ICGFLTU updates the current 12-bit filter value. Writes to the ICGFLTU register will not affect FLT if a previous latch sequence is not complete.

7.5.6 ICG Trim Register (ICGTRM)

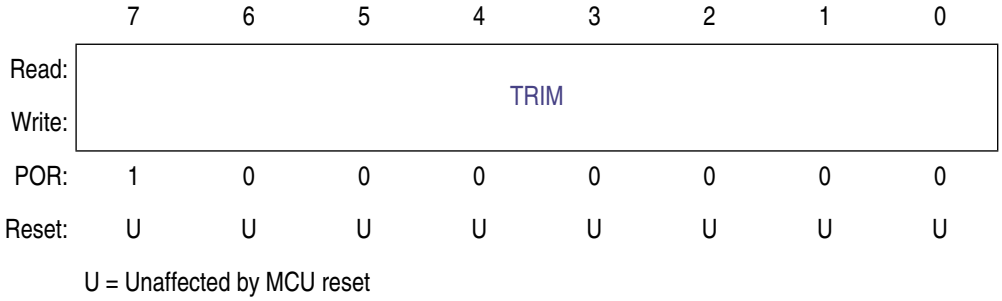


Figure 7-19. ICG Trim Register (ICGTRM)

TRIM — ICG Trim Setting

The TRIM bits control the internal reference generator frequency. They allow a ± 25% adjustment of the nominal (POR) period. The bit's effect on period is binary weighted (i.e., bit 1 will adjust twice as much as changing bit 0). Increasing the binary value in TRIM will increase the period and decreasing the value will decrease the period.

rel — Any label or expression that refers to an address that is within –128 to +127 locations from the next address after the last byte of object code for the current instruction. The assembler will calculate the 8-bit signed offset and include it in the object code for this instruction.

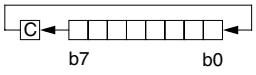
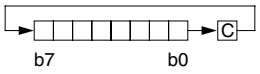
Address modes

INH = Inherent (no operands)
IMM = 8-bit or 16-bit immediate
DIR = 8-bit direct
EXT = 16-bit extended
IX = 16-bit indexed no offset
IX+ = 16-bit indexed no offset, post increment (CBEQ and MOV only)
IX1 = 16-bit indexed with 8-bit offset from H:X
IX1+ = 16-bit indexed with 8-bit offset, post increment (CBEQ only)
IX2 = 16-bit indexed with 16-bit offset from H:X
REL = 8-bit relative offset
SP1 = Stack pointer with 8-bit offset
SP2 = Stack pointer with 16-bit offset

Table 8-1. HCS08 Instruction Set Summary (Sheet 1 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles[1]
			V	H	I	N	Z	C				
ADC #*opr8i* ADC *opr8a* ADC *opr16a* ADC *oprx16*,X ADC *oprx8*,X ADC ,X ADC *oprx16*,SP ADC *oprx8*,SP	Add with Carry	A ← (A) + (M) + (C)			–				IMM DIR EXT IX2 IX1 IX SP2 SP1	A9 B9 C9 D9 E9 F9 9ED9 9EE9	ii dd hh ll ee ff ff	2 3 4 4 3 3 5 4
ADD #*opr8i* ADD *opr8a* ADD *opr16a* ADD *oprx16*,X ADD *oprx8*,X ADD ,X ADD *oprx16*,SP ADD *oprx8*,SP	Add without Carry	A ← (A) + (M)			–				IMM DIR EXT IX2 IX1 IX SP2 SP1	AB BB CB DB EB FB 9EDB 9EEB	ii dd hh ll ee ff ff	2 3 4 4 3 3 5 4
AIS #*opr8i*	Add Immediate Value (Signed) to Stack Pointer	SP ← (SP) + (M) M is sign extended to a 16-bit value	–	–	–	–	–	–	IMM	A7	ii	2
AIX #*opr8i*	Add Immediate Value (Signed) to Index Register (H:X)	H:X ← (H:X) + (M) M is sign extended to a 16-bit value	–	–	–	–	–	–	IMM	AF	ii	2
AND #*opr8i* AND *opr8a* AND *opr16a* AND *oprx16*,X AND *oprx8*,X AND ,X AND *oprx16*,SP AND *oprx8*,SP	Logical AND	A ← (A) & (M)	0	–	–			–	IMM DIR EXT IX2 IX1 IX SP2 SP1	A4 B4 C4 D4 E4 F4 9ED4 9EE4	ii dd hh ll ee ff ff	2 3 4 4 3 3 5 4

Table 8-1. HCS08 Instruction Set Summary (Sheet 6 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles[1]
			V	H	I	N	Z	C				
PULA	Pull Accumulator from Stack	SP ← (SP + $0001); Pull (A)	–	–	–	–	–	–	INH	86		3
PULH	Pull H (Index Register High) from Stack	SP ← (SP + $0001); Pull (H)	–	–	–	–	–	–	INH	8A		3
PULX	Pull X (Index Register Low) from Stack	SP ← (SP + $0001); Pull (X)	–	–	–	–	–	–	INH	88		3
ROL *oprx8*,X ROL ,X ROL *oprx8*,SP	Rotate Left through Carry			–	–				DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	5 1 1 5 4 6
ROR *oprx8*,X ROR ,X ROR *oprx8*,SP	Rotate Right through Carry			–	–				DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	5 1 1 5 4 6
RSP	Reset Stack Pointer	SP ← $FF (High Byte Not Affected)	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + $0001; Pull (CCR) SP ← (SP) + $0001; Pull (A) SP ← (SP) + $0001; Pull (X) SP ← (SP) + $0001; Pull (PCH) SP ← (SP) + $0001; Pull (PCL)							INH	80		9
RTS	Return from Subroutine	SP ← SP + $0001; Pull (PCH) SP ← SP + $0001; Pull (PCL)	–	–	–	–	–	–	INH	81		6
SBC #*opr8i* SBC *opr8a* SBC *opr16a* SBC *oprx16*,X SBC *oprx8*,X SBC ,X SBC *oprx16*,SP SBC *oprx8*,SP	Subtract with Carry	A ← (A) – (M) – (C)		–	–				IMM DIR EXT IX2 IX1 IX SP2 SP1	A2 B2 C2 D2 E2 F2 9ED2 9EE2	ii dd hh ll ee ff ff ee ff ff	2 3 4 4 3 3 5 4
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask Bit	I ← 1	–	–	1	–	–	–	INH	9B		1
STA *opr8a* STA *opr16a* STA *oprx16*,X STA *oprx8*,X STA ,X STA *oprx16*,SP STA *oprx8*,SP	Store Accumulator in Memory	M ← (A)	0	–	–			–	DIR EXT IX2 IX1 IX SP2 SP1	B7 C7 D7 E7 F7 9ED7 9EE7	dd hh ll ee ff ff ee ff ff	3 4 4 3 2 5 4
STHX *opr8a* STHX *opr16a* STHX *oprx8*,SP	Store H:X (Index Reg.)	(M:M + $0001) ← (H:X)	0	–	–			–	DIR EXT SP1	35 96 9EFF	dd hh ll ff	4 5 5
STOP	Enable Interrupts: Stop Processing Refer to MCU Documentation	I bit ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		2+
STX *opr8a* STX *opr16a* STX *oprx16*,X STX *oprx8*,X STX ,X STX *oprx16*,SP STX *oprx8*,SP	Store X (Low 8 Bits of Index Register) in Memory	M ← (X)	0	–	–			–	DIR EXT IX2 IX1 IX SP2 SP1	BF CF DF EF FF 9EDF 9EEF	dd hh ll ee ff ff ee ff ff	3 4 4 3 2 5 4

9.3 KBI Block Diagram

Figure 9-3 shows the block diagram for a KBI module.

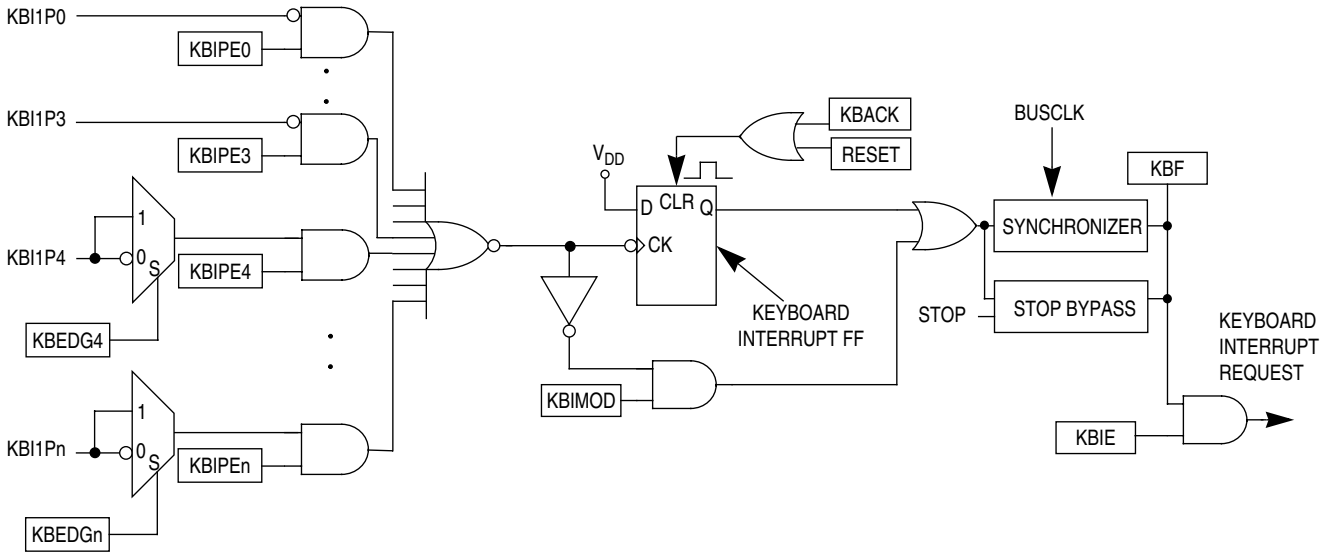


Figure 9-3. KBI Block Diagram

The KBI module allows up to eight pins to act as additional interrupt sources. Four of these pins allow falling-edge sensing while the other four can be configured for either rising-edge sensing or falling-edge sensing. The sensing mode for all eight pins can also be modified to detect edges and levels instead of only edges.

9.4 Keyboard Interrupt (KBI) Module

This on-chip peripheral module is called a keyboard interrupt (KBI) module because originally it was designed to simplify the connection and use of row-column matrices of keyboard switches. However, these inputs are also useful as extra external interrupt inputs and as an external means of waking up the MCU from stop or wait low-power modes.

9.4.1 Pin Enables

The KBIPEn control bits in the KBI1PE register allow a user to enable (KBIPEn = 1) any combination of KBI-related port pins to be connected to the KBI module. Pins corresponding to 0s in KBI1PE are general-purpose I/O pins that are not associated with the KBI module.

9.4.2 Edge and Level Sensitivity

Synchronous logic is used to detect edges. Prior to detecting an edge, enabled keyboard inputs in a KBI module must be at the deasserted logic level.

A falling edge is detected when an enabled keyboard input signal is seen as a logic 1 (the deasserted level) during one bus cycle and then a logic 0 (the asserted level) during the next cycle.

9.5.2 KBI Pin Enable Register (KBI1PE)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	KBIPE7	KBIPE6	KBIPE5	KBIPE4	KBIPE3	KBIPE2	KBIPE1	KBIPE0
Reset:	0	0	0	0	0	0	0	0

Figure 9-5. KBI Pin Enable Register (KBI1PE)

KBIPEn — Keyboard Pin Enable for KBI Port Bit n (n = 7–0)

Each of these read/write bits selects whether the associated KBI port pin is enabled as a keyboard interrupt input or functions as a general-purpose I/O pin.

1 = Bit n of KBI port enabled as a keyboard interrupt input

0 = Bit n of KBI port is a general-purpose I/O pin not associated with the KBI.

10.6.4 PWM End-of-Duty-Cycle Events

For channels that are configured for PWM operation, there are two possibilities:

- When the channel is configured for edge-aligned PWM, the channel flag is set when the timer counter matches the channel value register that marks the end of the active duty cycle period.
- When the channel is configured for center-aligned PWM, the timer count matches the channel value register twice during each PWM cycle. In this CPWM case, the channel flag is set at the start and at the end of the active duty cycle, which are the times when the timer counter matches the channel value register.

The flag is cleared by the 2-step sequence described in Section 10.6.1, "Clearing Timer Interrupt Flags."

10.7 TPM Registers and Control Bits

The TPM includes:

- An 8-bit status and control register (TPMxSC)
- A 16-bit counter (TPMxCNTH:TPMxCNTL)
- A 16-bit modulo register (TPMxMODH:TPMxMODL)

Each timer channel has:

- An 8-bit status and control register (TPMxCnSC)
- A 16-bit channel value register (TPMxCnVH:TPMxCnVL)

Refer to the direct-page register summary in the Memory chapter of this data sheet for the absolute address assignments for all TPM registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

Some MCU systems have more than one TPM, so register names include placeholder characters to identify which TPM and which channel is being referenced. For example, TPMxCnSC refers to timer (TPM) x, channel n and TPM1C2SC is the status and control register for timer 1, channel 2.

10.7.1 Timer x Status and Control Register (TPMxSC)

TPMxSC contains the overflow status flag and control bits that are used to configure the interrupt enable, TPM configuration, clock source, and prescale divisor. These controls relate to all channels within this timer module.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-5. Timer x Status and Control Register (TPMxSC)

When polling is used, this sequence is naturally satisfied in the normal course of the user program. If hardware interrupts are used, SCIxS1 must be read in the interrupt service routine (ISR). Normally, this is done in the ISR anyway to check for receive errors, so the sequence is automatically satisfied.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the RxD1 line remains idle for an extended period of time. IDLE is cleared by reading SCIxS1 while IDLE = 1 and then reading SCIxD. After IDLE has been cleared, it cannot become set again until the receiver has received at least one new character and has set RDRF.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead and the data and any associated NF, FE, or PF condition is lost.

11.8 Additional SCI Functions

The following sections describe additional SCI functions.

11.8.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCIxC1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCIxC3. For the receiver, the ninth bit is held in R8 in SCIxC3.

When transmitting 9-bit data, write to the T8 bit before writing to SCIxD for coherent writes to the transmit data buffer. If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCIxD to the shifter.

When receiving 9-bit data, clear the RDRF bit by reading both R8 and SCIxD. R8 and SCIxD can be read in either order.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wakeup so the ninth data bit can serve as the wakeup bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

11.9 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted.

In stop1 and stop2 modes, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes.

No SCI module registers are affected in stop3 mode.

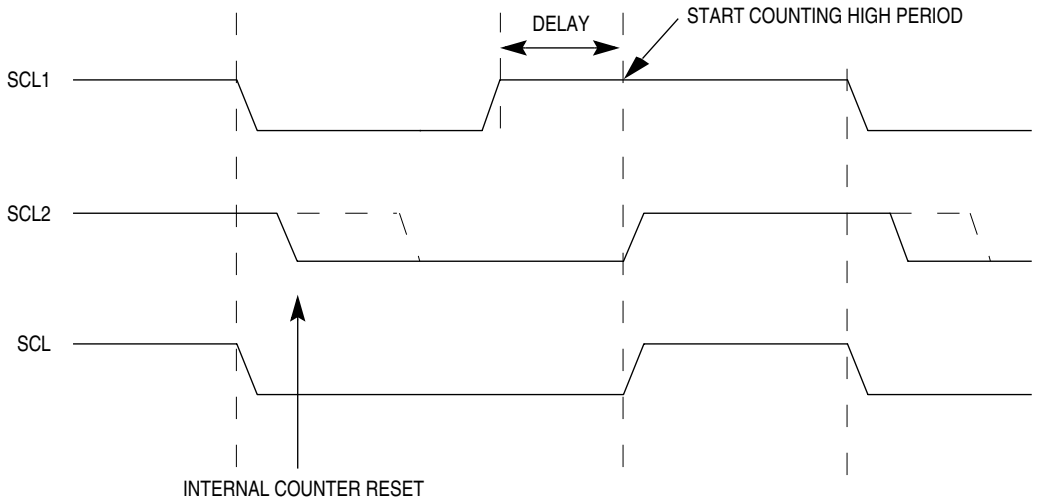


Figure 13-4. IIC Clock Synchronization

13.2.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

13.2.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

13.3 Resets

The IIC is disabled after reset. The IIC cannot cause an MCU reset.

14.3.3 Analog Input Multiplexer

The analog input multiplexer selects one of the eight external analog input channels to generate an analog sample. The analog input multiplexer includes negative stress protection circuitry which prevents cross-talk between channels when the applied input potentials are within specification. Only analog input signals within the potential range of V_{REFL} to V_{REFH} (ATD reference potentials) will result in valid ATD conversions.

14.3.4 ATD Module Accuracy Definitions

Figure 14-4 illustrates an ideal ATD transfer function. The horizontal axis represents the ATD input voltage in millivolts. The vertical axis the conversion result code. The ATD is specified with the following figures of merit:

- Number of bits (N) — The number of bits in the digitized output
- Resolution (LSB) — The resolution of the ATD is the step size of the ideal transfer function. This is also referred to as the ideal code width, or the difference between the transition voltages to a given code and to the next code. This unit, known as 1LSB, is equal to

$$1LSB = (V_{REFH} - V_{REFL}) / 2^N \qquad \textit{Eqn. 14-5}$$

- Inherent quantization error (E_Q) — This is the error caused by the division of the perfect ideal straight-line transfer function into the quantized ideal transfer function with 2^N steps. This error is ± 1/2 LSB.
- Differential non-linearity (DNL) — This is the difference between the current code width and the ideal code width (1LSB). The current code width is the difference in the transition voltages to the current code and to the next code. A negative DNL means the transfer function spends less time at the current code than ideal; a positive DNL, more. The DNL cannot be less than –1.0; a DNL of greater than 1.0 reduces the effective number of bits by 1.
- Integral non-linearity (INL) — This is the difference between the transition voltage to the current code and the transition to the corresponding code on the adjusted transfer curve. INL is a measure of how straight the line is (how far it deviates from a straight line). The adjusted ideal transition voltage is:

Eqn. 14-6

$$\text{Adjusted Ideal Trans. V} = \frac{(\text{Current Code} - 1/2)}{2^N} * ((V_{REFH} + E_{FS}) - (V_{REFL} + E_{ZS}))$$

- Zero scale error (E_{ZS}) — This is the difference between the transition voltage to the first valid code and the ideal transition to that code. Normally, it is defined as the difference between the actual and ideal transition to code $001, but in some cases the first transition may be to a higher code. The ideal transition to any code is:

Eqn. 14-7

$$\text{Ideal Transition V} = \frac{(\text{Current Code} - 1/2)}{2^N} *(V_{REFH} - V_{REFL})$$

Figure 15-3 shows the host receiving a logic 1 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target MCU. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target MCU drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host should sample the bit level about 10 cycles after it started the bit time.

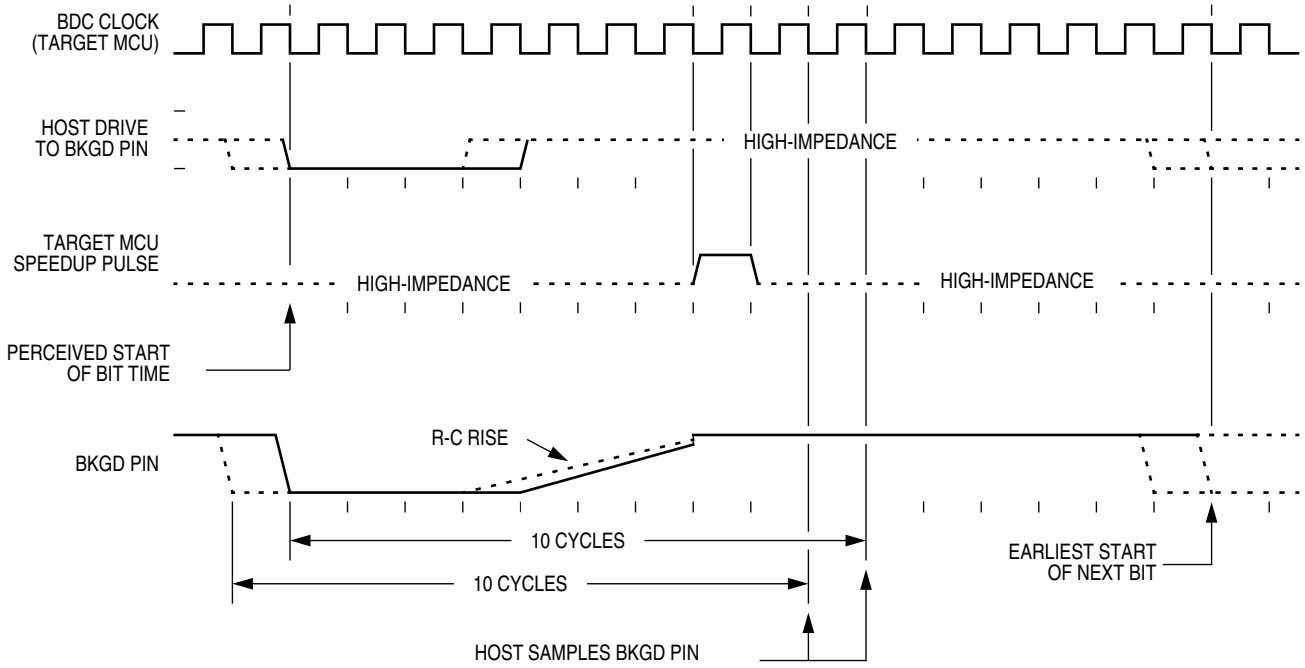


Figure 15-3. BDC Target-to-Host Serial Bit Timing (Logic 1)

TRG3:TRG2:TRG1:TRG0 — Select Trigger Mode

Selects one of nine triggering modes

Table 15-2. Trigger Mode Selection

TRG[3:0]	Triggering Mode
0000	A-only
0001	A OR B
0010	A Then B
0011	Event-only B (store data)
0100	A then event-only B (store data)
0101	A AND B data (full mode)
0110	A AND NOT B data (full mode)
0111	Inside range: A ≤ address ≤ B
1000	Outside range: address < A or address > B
1001 – 1111	No trigger

15.5.3.9 Debug Status Register (DBGS)

This is a read-only status register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AF	BF	ARMF	0	CNT3	CNT2	CNT1	CNT0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-9. Debug Status Register (DBGS)

AF — Trigger Match A Flag

AF is cleared at the start of a debug run and indicates whether a trigger match A condition was met since arming.

1 = Comparator A match.
0 = Comparator A has not matched.

BF — Trigger Match B Flag

BF is cleared at the start of a debug run and indicates whether a trigger match B condition was met since arming.

1 = Comparator B match.
0 = Comparator B has not matched.

A.7 ATD Characteristics

Table A-6. ATD Electrical Characteristics (Operating)

Num	Characteristic	Condition	Symbol	Min	Typical	Max	Unit
1	ATD supply[1]		V_{DDAD}	1.80	—	3.6	V
2	ATD supply current	Enabled	$I_{DDADrun}$	—	0.7	1.2	mA
		Disabled (ATDPU = 0 or STOP)	$I_{DDADstop}$	—	0.02	0.6	µA
3	Differential supply voltage	V_{DD}–V_{DDAD}	$\lvert V_{DDLT}\rvert$	—	—	100	mV
4	Differential ground voltage	V_{SS}–V_{SSAD}	$\lvert V_{SDLT}\rvert$	—	—	100	mV
5	Reference potential, low		$\lvert V_{REFL}\rvert$	—	—	V_{SSAD}	V
	Reference potential, high	2.08V ≤ V_{DDAD} ≤ 3.6V	V_{REFH}	2.08	—	V_{DDAD}	V
		1.80V ≤ V_{DDAD} < 2.08V		V_{DDAD}	—	V_{DDAD}	
6	Reference supply current (V_{REFH} to V_{REFL})	Enabled	I_{REF}	—	200	300	µA
		Disabled (ATDPU = 0 or STOP)	I_{REF}	—	<0.01	0.02	
7	Analog input voltage[2]		V_{INDC}	V_{SSAD} – 0.3	—	V_{DDAD} + 0.3	V

1 V_{DDAD} must be at same potential as V_{DD}.
2 Maximum electrical operating range, not valid conversion range.

Appendix B Ordering Information and Mechanical Drawings

B.1 Ordering Information

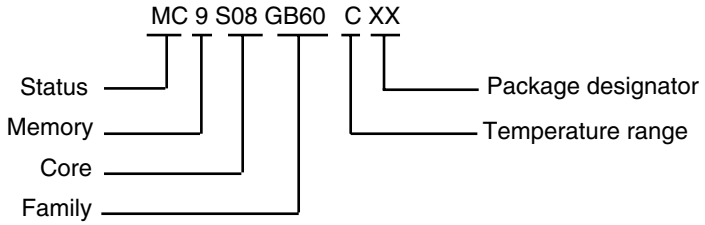
This section contains ordering numbers for MC9S08GB60, MC9S08GB32, MC9S08GT60, MC9S08GT32, and MC9S08GT16 devices. See below for an example of the device numbering system.

Table B-1. Device Numbering System

MC Order Number	FLASH Memory	RAM	TPM	Available Package Type (Part Number Suffix)
MC9S08GB60	60K	4K	One 3-channel and one 5-channel 16-bit timer	64 LQFP (FU)
MC9S08GB32	32K	2K	One 3-channel and one 5-channel 16-bit timer	64 LQFP (FU)
MC9S08GT60	60K	4K	Two 2-channel/16-bit timers	48 QFN (FD)[1] 44 QFP (FB) 42 SDIP (B)
MC9S08GT32	32K	2K	Two 2-channel/16-bit timers	48 QFN (FD)(1) 44 QFP (FB) 42 SDIP (B)
MC9S08GT16	16K	1K	Two 2-channel/16-bit timers	48 QFN (FD)(1) 44 QFP (FB) 42 SDIP (B)

[1] The 48-pin QFN package has one 3-channel and one 2-channel 16-bit TPM.

Temperature and package designators:
C = –40°C to 85°C
FU = 64-pin Low Quad Flat Package (LQFP)
FD = 48-pin Quad Flat Package, No Leads
FB = 44-pin Quad Flat Package (QFP)
B = 42-pin Skinny Dual In-Line Package (SDIP)
MC = Fully qualified



B.2 Mechanical Drawings

This appendix contains mechanical specifications for MC9S08GB/GT MCU.