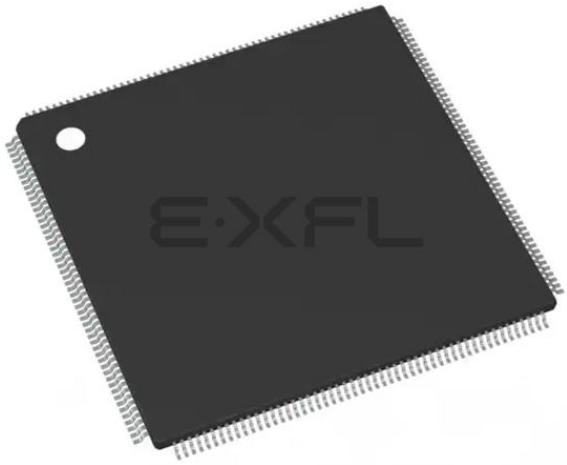

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 480MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 168 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1M x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 36x16b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-LQFP |
| Supplier Device Package | 208-LQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h753bit6 |

# 3 Functional overview

## 3.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

*Figure 1* shows the general block diagram of the STM32H753xI family.

*Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.*

## 3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory through a serial interface (USART, I2C, SPI, USB-DFU). Refer to *STM32 microcontroller System memory Boot mode* application note (AN2606) for details.

## 3.5 Power supply management

### 3.5.1 Power supply scheme

STM32H53xI power supply voltages are the following:

- $V_{DD}$ = 1.62 to 3.6 V: external power supply for I/Os, provided externally through $V_{DD}$ pins.
- $V_{DDLDO}$ = 1.62 to 3.6 V: supply voltage for the internal regulator supplying $V_{CORE}$
- $V_{DDA}$ = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP and OPAMP.
- $V_{DD33USB}$ and $V_{DD50USB}$:
  $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a $V_{DD}$ supply different from 3.3 V.
  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if $V_{DD}$ = 3.3 V.
- $V_{BAT}$ = 1.2 to 3.6 V: power supply for the $V_{SW}$ domain when $V_{DD}$ is not present.
- $V_{CAP}$: $V_{CORE}$ supply voltage, which values depend on voltage scaling (0.7 V, 0.9 V, 1.0 V, 1.1 V or 1.2 V). They are configured through VOS bits in PWR_D3CR register. The $V_{CORE}$ domain is split into the following power domains that can be independently switch off.
  - D1 domain containing some peripherals and the Cortex®-M7 core.
  - D2 domain containing a large part of the peripherals.
  - D3 domain containing some peripherals and the system control.

During power-up and power-down phases, the following power sequence requirements must be respected (see *Figure 2*):

- When $V_{DD}$ is below 1 V, other power supplies ($V_{DDA}$, $V_{DD33USB}$, $V_{DD50USB}$) must remain below $V_{DD}$ + 300 mV.
- When $V_{DD}$ is above 1 V, all power supplies are independent.

During the power-down phase, $V_{DD}$ can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

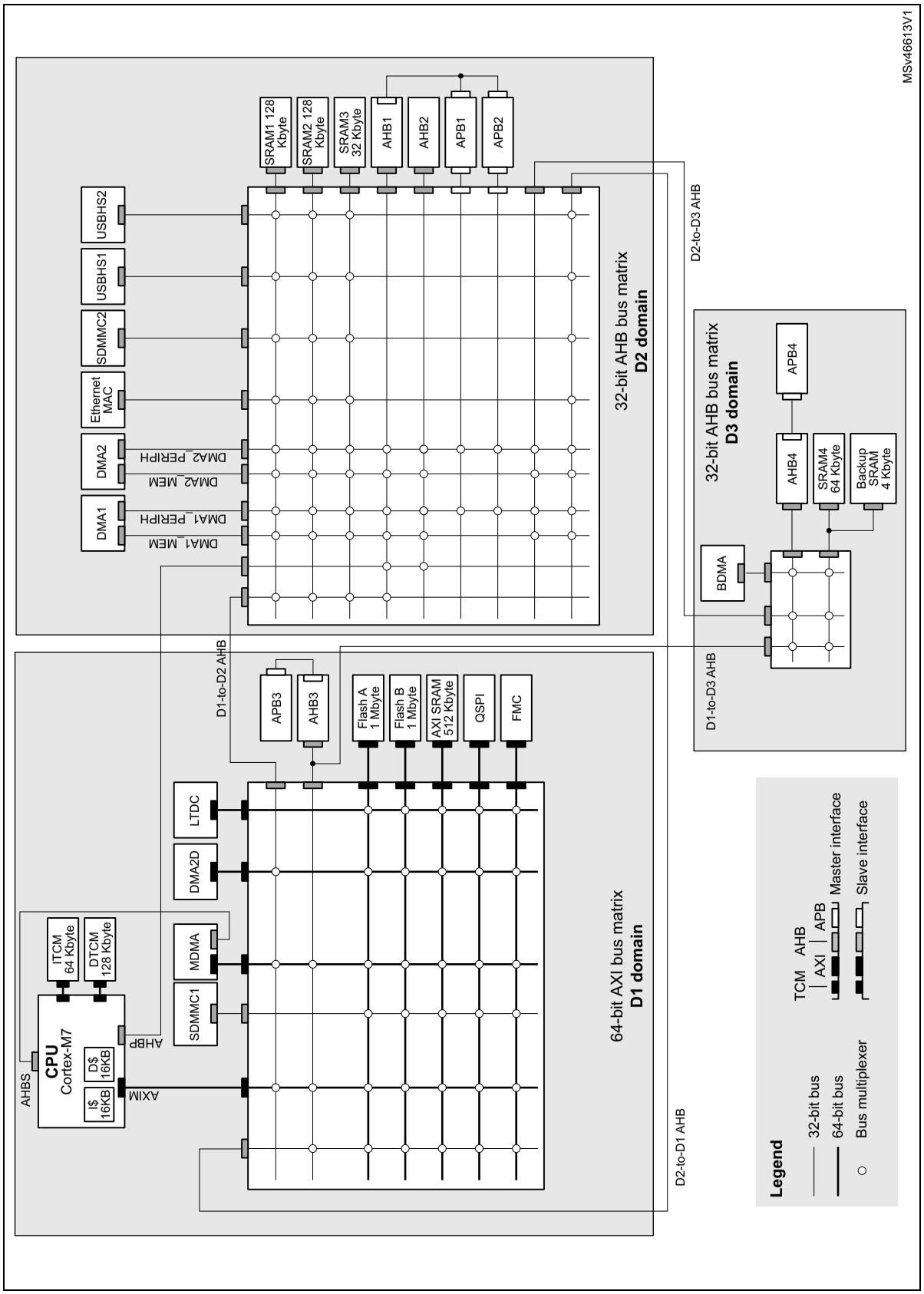



Figure 3. STM32H753xI bus matrix

## 3.31 Inter-integrated circuit interface (I2C)

STM32H753xI devices embed four $I^2C$ interfaces.

The $I^2C$ bus interface handles communications between the microcontroller and the serial $I^2C$ bus. It controls all $I^2C$ bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- $I^2C$-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

## 3.32 Universal synchronous/asynchronous receiver transmitter (USART)

STM32H753xI devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to *Table 6* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire Half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 12.5 Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

## 3.36 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

## 3.37 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- Full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

**Table 8. STM32H753xI pin/ball definition (continued)**

| Pin/ball name | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | LQFP144 | UFBGA169 | UFBGA176+25 | LQFP176 | LQFP208 | TFBGA240 +25 | | | | | | |
| 31 | K3 | 43 | J6 | R3 | 53 | 56 | R5 | PA7 | I/O | TT_a | - | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT | ADC12_INN3, ADC12_INP7, OPAMP1_VINM |
| 32 | G4 | 44 | K6 | N5 | 54 | 57 | T4 | PC4 | I/O | TT_a | - | DFSDM_CKIN2, I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT | ADC12_INP4, OPAMP1_VOUT, COMP_1_INM |
| 33 | H4 | 45 | N5 | P5 | 55 | 58 | U4 | PC5 | I/O | TT_a | - | SAI1_D3, DFSDM_DATIN2, SPDIFRX_IN3, SAI4_D3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP_1_OUT, EVENTOUT | ADC12_INN4, ADC12_INP8, OPAMP1_VINM |
| - | - | - | N4 | - | - | 59 | G13 | VDD | S | - | - | - | - |
| - | - | - | H12 | J9 | - | 60 | G16 | VSS | S | - | - | - | - |
| 34 | J4 | 46 | M5 | R5 | 56 | 61 | U5 | PB0 | I/O | FT_a | - | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT | ADC12_INN5, ADC12_INP9, OPAMP1_VINP, COMP_1_INP |
| 35 | K4 | 47 | L5 | R4 | 57 | 62 | T5 | PB1 | I/O | TT_u | - | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT | ADC12_INP5, COMP_1_INM |
| 36 | G5 | 48 | L6 | M6 | 58 | 63 | R6 | PB2 | I/O | FT_ha | - | SAI1_D1, DFSDM_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, QUADSPI_CLK, SAI4_D1, EVENTOUT | COMP_1_INP, RTC_OUT |

**Table 8. STM32H753xI pin/ball definition (continued)**

| Pin/ball name | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | LQFP144 | UFBGA169 | UFBGA176+25 | LQFP176 | LQFP208 | TFBGA240 +25 | | | | | | |
| - | - | - | - | E12 | 128 | 151 | D16 | PH13 | I/O | FT_h | - | TIM8_CH1N, UART4_TX, FDCAN1_TX, FMC_D21, LCD_G2, EVENTOUT | - |
| - | - | - | - | E13 | 129 | 152 | B17 | PH14 | I/O | FT_h | - | TIM8_CH2N, UART4_RX, FDCAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT | - |
| - | - | - | - | D13 | 130 | 153 | B16 | PH15 | I/O | FT_h | - | TIM8_CH3N, FDCAN1_TXFD_MODE, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT | - |
| - | - | - | A13 | E14 | 131 | 154 | A16 | PI0 | I/O | FT_h | - | TIM5_CH4, SPI2_NSS/I2S2_WS, FDCAN1_RXFD_MODE, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT | - |
| - | - | - | - | G9 | - | - | - | VSS | S | - | - | - | - |
| - | - | - | B13 | D14 | 132 | 155 | A15 | PI1 | I/O | FT_h | - | TIM8_BKIN2, SPI2_SCK/I2S2_CK, TIM8_BKIN2_COMP12, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT | - |
| - | - | - | A6 | C14 | 133 | 156 | B15 | PI2 | I/O | FT_h | - | TIM8_CH4, SPI2_MISO/I2S2_SDI, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT | - |
| - | - | - | B7 | C13 | 134 | 157 | C14 | PI3 | I/O | FT_h | - | TIM8_ETR, SPI2_MOSI/I2S2_SDO, FMC_D27, DCMI_D10, EVENTOUT | - |
| - | - | - | - | D9 | 135 | - | - | VSS | S | - | - | - | - |
| - | - | - | - | C9 | 136 | 158 | - | VDD | S | - | - | - | - |
| 76 | A9 | 109 | B12 | A14 | 137 | 159 | B14 | PA14 (JTCK/SWCLK) | I/O | FT | - | JTCK-SWCLK, EVENTOUT | - |
| 77 | A8 | 110 | C11 | A13 | 138 | 160 | A14 | PA15 (JTDI) | I/O | FT | - | JTDI, TIM2_CH1/TIM2_ETR, HRTIM_FLT1, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, UART7_TX, EVENTOUT | - |

## Table 11. Port C alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/12/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX | SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/COMP | UART5/LCD | SYS |
| Port C | PC0 | - | - | - | DFSDM_CKIN0 | - | - | DFSDM_DATIN4 | - | SAI2_FS_B | - | OTG_HS_ULPI_STP | - | FMC_SDNWE | - | LCD_R5 | EVENT-OUT |
| | PC1 | TRACED0 | - | SAI1_D1 | DFSDM_DATIN0 | DFSDM_CKIN4 | SPI2_MOSI/I2S2_SDO | SAI1_SD_A | - | SAI4_SD_A | SDMMC2_CK | SAI4_D1 | ETH_MDC | MDIOS_MDC | - | - | EVENT-OUT |
| | PC2 | - | - | - | DFSDM_CKIN1 | - | SPI2_MISO/I2S2_SDI | DFSDM_CKOUT | - | - | - | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | FMC_SDNE0 | - | - | EVENT-OUT |
| | PC3 | - | - | - | DFSDM_DATIN1 | - | SPI2_MOSI/I2S2_SDO | - | - | - | - | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK | FMC_SDCKE0 | - | - | EVENT-OUT |
| | PC4 | - | - | - | DFSDM_CKIN2 | - | I2S1_MCK | - | - | - | SPDIFRX_IN2 | - | ETH_MII_RXD0/ETH_RMII_RXD0 | FMC_SDNE0 | - | - | EVENT-OUT |
| | PC5 | - | - | SAI1_D3 | DFSDM_DATIN2 | - | - | - | - | | SPDIFRX_IN3 | SAI4_D3 | ETH_MII_RXD1/ETH_RMII_RXD1 | FMC_SDCKE0 | COMP_1_OUT | - | EVENT-OUT |
| | PC6 | - | HRTIM_CHA1 | TIM3_CH1 | TIM8_CH1 | DFSDM_CKIN3 | I2S2_MCK | - | USART6_TX | SDMMC1_D0DIR | FMC_NWAIT | SDMMC2_D6 | - | SDMMC1_D6 | DCMI_D0 | LCD_HSYNC | EVENT-OUT |
| | PC7 | TRGIO | HRTIM_CHA2 | TIM3_CH2 | TIM8_CH2 | DFSDM_DATIN3 | - | I2S3_MCK | USART6_RX | SDMMC1_D123DIR | FMC_NE1 | SDMMC2_D7 | SWPMI_TX | SDMMC1_D7 | DCMI_D1 | LCD_G6 | EVENT-OUT |
| | PC8 | TRACED1 | HRTIM_CHB1 | TIM3_CH3 | TIM8_CH3 | - | - | - | USART6_CK | UART5_RTS | FMC_NE2/FMC_NCE | - | SWPMI_RX | SDMMC1_D0 | DCMI_D2 | - | EVENT-OUT |
| | PC9 | MCO2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S_CKIN | - | - | UART5_CTS | QUADSPI_BK1_IO0 | LCD_G3 | SWPMI_SUSPEND | SDMMC1_D1 | DCMI_D3 | LCD_B2 | EVENT-OUT |
| | PC10 | - | - | HRTIM_EEV1 | DFSDM_CKIN5 | - | - | SPI3_SCK/I2S3_CK | USART3_TX | UART4_TX | QUADSPI_BK1_IO1 | - | - | SDMMC1_D2 | DCMI_D8 | LCD_R2 | EVENT-OUT |
| | PC11 | - | - | HRTIM_FLT2 | DFSDM_DATIN5 | - | - | SPI3_MISO/I2S3_SDI | USART3_RX | UART4_RX | QUADSPI_BK2_NCS | - | - | SDMMC1_D3 | DCMI_D4 | - | EVENT-OUT |
| | PC12 | TRACED3 | - | HRTIM_EEV2 | - | - | - | SPI3_MOSI/I2S3_SDO | USART3_CK | UART5_TX | - | - | - | SDMMC1_CK | DCMI_D9 | - | EVENT-OUT |
| | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT-OUT |

**Table 11. Port C alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/ HRTIM1 | SAI1/TIM3/4/5/12/ HRTIM1 | LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM | I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM | SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/ SDMMC1/ SPDIFRX | SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX | SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD | I2C4/ UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ ETH | TIM1/8/FMC/SDMMC1/ MDIOS/ OTG1_FS/ LCD | TIM1/DCMI/LCD/ COMP | UART5/ LCD | SYS |
| Port C | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT-OUT |
| | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT-OUT |

## Table 13. Port E alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/12/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX | SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/COMP | UART5/LCD | SYS |
| Port E | PE0 | - | LPTIM1_ETR | TIM4_ETR | HRTIM_SCIN | LPTIM2_ETR | - | - | - | UART8_RX | FDCAN1_RXFD_MODE | SAI2_MCK_A | - | FMC_NBL0 | DCMI_D2 | - | EVENT-OUT |
| | PE1 | - | LPTIM1_IN2 | - | HRTIM_SCOUT | - | - | - | - | UART8_TX | FDCAN1_TXFD_MODE | - | - | FMC_NBL1 | DCMI_D3 | - | EVENT-OUT |
| | PE2 | TRACECLK | - | SAI1_CK1 | - | - | SPI4_SCK | SAI1_MCLK_A | - | SAI4_MCLK_A | QUADSPI_BK1_IO2 | SAI4_CK1 | ETH_MII_TXD3 | FMC_A23 | - | - | EVENT-OUT |
| | PE3 | TRACED0 | - | - | - | TIM15_BKIN | - | SAI1_SD_B | - | SAI4_SD_B | - | - | - | FMC_A19 | - | - | EVENT-OUT |
| | PE4 | TRACED1 | - | SAI1_D2 | DFSDM_DATIN3 | TIM15_CH1N | SPI4_NSS | SAI1_FS_A | - | SAI4_FS_A | - | SAI4_D2 | - | FMC_A20 | DCMI_D4 | LCD_B0 | EVENT-OUT |
| | PE5 | TRACED2 | - | SAI1_CK2 | DFSDM_CKIN3 | TIM15_CH1 | SPI4_MISO | SAI1_SCK_A | - | SAI4_SCK_A | - | SAI4_CK2 | - | FMC_A21 | DCMI_D6 | LCD_G0 | EVENT-OUT |
| | PE6 | TRACED3 | TIM1_BKIN2 | SAI1_D1 | - | TIM15_CH2 | SPI4_MOSI | SAI1_SD_A | - | SAI4_SD_A | SAI4_D1 | SAI2_MCK_B | TIM1_BKIN2_COMP12 | FMC_A22 | DCMI_D7 | LCD_G1 | EVENT-OUT |
| | PE7 | - | TIM1_ETR | - | DFSDM_DATIN2 | - | - | - | UART7_RX | - | - | QUADSPI_BK2_IO0 | - | FMC_D4/FMC_DA4 | - | - | EVENT-OUT |
| | PE8 | - | TIM1_CH1N | - | DFSDM_CKIN2 | - | - | - | UART7_TX | - | - | QUADSPI_BK2_IO1 | - | FMC_D5/FMC_DA5 | COMP_2_OUT | - | EVENT-OUT |
| | PE9 | - | TIM1_CH1 | - | DFSDM_CKOUT | - | - | - | UART7_RTS | - | - | QUADSPI_BK2_IO2 | - | FMC_D6/FMC_DA6 | - | - | EVENT-OUT |
| | PE10 | - | TIM1_CH2N | - | DFSDM_DATIN4 | - | - | - | UART7_CTS | - | - | QUADSPI_BK2_IO3 | - | FMC_D7/FMC_DA7 | - | - | EVENT-OUT |
| | PE11 | - | TIM1_CH2 | - | DFSDM_CKIN4 | - | SPI4_NSS | - | - | - | - | SAI2_SD_B | - | FMC_D8/FMC_DA8 | - | LCD_G3 | EVENT-OUT |
| | PE12 | - | TIM1_CH3N | - | DFSDM_DATIN5 | - | SPI4_SCK | - | - | - | - | SAI2_SCK_B | - | FMC_D9/FMC_DA9 | COMP_1_OUT | LCD_B4 | EVENT-OUT |
| | PE13 | - | TIM1_CH3 | - | DFSDM_CKIN5 | - | SPI4_MISO | - | - | - | - | SAI2_FS_B | - | FMC_D10/FMC_DA10 | COMP_2_OUT | LCD_DE | EVENT-OUT |
| | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCK_B | - | FMC_D11/FMC_DA11 | - | LCD_CLK | EVENT-OUT |
| | PE15 | - | TIM1_BKIN | - | - | - | HDMI__TIM1_BKIN | - | - | - | - | | - | FMC_D12/FMC_DA12 | TIM1_BKIN_COMP12 | LCD_R7 | EVENT-OUT |

**Table 27. Embedded reference voltage (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\_DIV1}$ | 1/4 reference voltage | - | - | 25 | - | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$ | 1/2 reference voltage | - | - | 50 | - | |
| $V_{REFINT\_DIV3}$ | 3/4 reference voltage | - | - | 75 | - | |

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

**Table 28. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN\_CAL}$ | Raw data acquired at temperature of 30 °C, $V_{DDA}$ = 3.3 V | 1FF1E860 - 1FF1E861 |

### 6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 15: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the $f_{ACLK}$ frequency (refer to the table “Number of wait states according to CPU clock ($f_{rcc\_c\_ck}$) frequency and $V_{CORE}$ range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in *Table 29* to *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

**Table 35. Typical and maximum current consumption in Stop mode, regulator ON**

| Symbol | Parameter | Conditions | | Typ | Max(1) | | | | unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $T_J$ = 25°C | $T_J$ = 85°C | $T_J$ = 105°C | $T_J$ = 125°C | |
| $I_{DD(Stop)}$ | D1Stop, D2Stop, D3Stop | Flash memory in low-power mode, no IWDG | SVOS5 | 1.4 | 7.2(2) | 49 | 75(2) | 140 | mA |
| | | | SVOS4 | 1.95 | 11 | 66 | 110 | 200 | |
| | | | SVOS3 | 2.85 | 16(2) | 91 | 150(2) | 240 | |
| | | Flash memory ON, no IWDG | SVOS5 | 1.65 | 7.2 | 49 | 75 | 140 | |
| | | | SVOS4 | 2.2 | 11 | 66 | 110 | 180 | |
| | | | SVOS3 | 3.15 | 16 | 91 | 150 | 300 | |
| | D1Stop, D2Standby, D3Stop | Flash memory OFF, no IWDG | SVOS5 | 0.99 | 5.1 | 35 | 60 | 97 | |
| | | | SVOS4 | 1.4 | 7.5 | 47 | 79 | 130 | |
| | | | SVOS3 | 2.05 | 12 | 64 | 110 | 170 | |
| | | Flash memory ON, no IWDG | SVOS5 | 1.25 | 5.5 | 35 | 61 | 98 | |
| | | | SVOS4 | 1.65 | 7.8 | 47 | 80 | 130 | |
| | | | SVOS3 | 2.3 | 12 | 65 | 110 | 170 | |
| | D1Standby, D2Stop, D3Stop | Flash OFF, no IWDG | SVOS5 | 0.57 | 3 | 21 | 36 | 57 | |
| | | | SVOS4 | 0.805 | 4.5 | 27 | 47 | 74 | |
| | | | SVOS3 | 1.2 | 6.7 | 37 | 63 | 99 | |
| | D1Standby, D2Standby, D3Stop | | SVOS5 | 0.17 | 1.1(2) | 8 | 13(2) | 20 | |
| | | | SVOS4 | 0.245 | 1.5 | 11 | 17 | 26 | |
| | | | SVOS3 | 0.405 | 2.4(2) | 15 | 23(2) | 35 | |

1. Guaranteed by characterization results.
2. Guaranteed by test in production.

**Table 36. Typical and maximum current consumption in Standby mode**

| Symbol | Parameter | Conditions | | Typ(3) | | | | Max (3 V)(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Backup SRAM | RTC & LSE | 1.62 V | 2.4 V | 3 V | 3.3 V | $T_J$ = 25°C | $T_J$ = 85°C | $T_J$ = 105°C | $T_J$ = 125°C | |
| $I_{DD}$ (Standby) | Supply current in Standby mode | OFF | OFF | 1.8 | 1.9 | 1.95 | 2.05 | 4(2) | 18(3) | 40(2) | 90(3) | µA |
| | | ON | OFF | 3.4 | 3.4 | 3.5 | 3.7 | 8.2(3) | 47(3) | 83(3) | 141(3) | |
| | | OFF | ON | 2.4 | 3.5 | 3.86 | 4.12 | - | - | - | - | |
| | | ON | ON | 3.95 | 5.1 | 5.46 | 5.97 | - | - | - | - | |

1. The maximum current consumption values are given for PDR OFF (internal reset OFF). When the PDR is OFF (internal reset OFF), the current consumption is reduced by 1.2 µA compared to PDR ON.
2. Guaranteed by test in production.
3. Guaranteed by characterization results.

### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

**Table 57. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latchup class | $T_A$ = +25 °C conforming to JESD78 | II level A |

## 6.3.14 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

**Table 58. I/O current injection susceptibility(1)**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | PA7, PC5, PG1, PB14, PJ7, PA11, PA12, PA13, PA14, PA15, PJ12, PB4 | 5 | 0 | mA |
| | PA2, PH2, PH3, PE8, PA6, PA7, PC4, PE7, PE10, PE11 | 0 | NA | |
| | PA0, PA_C, PA1, PA1_C, PC2, PC2_C, PC3, PC3_C, PA4, PA5, PH4, PH5, BOOT0 | 0 | 0 | |
| | All other I/Os | 5 | NA | |

1. Guaranteed by characterization.

**Table 61. Output timing characteristics (HSLV OFF)(1) (continued)**

| Speed | Symbol | Parameter | conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 10 | $F_{max}$(2) | Maximum frequency | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 85 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 35 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 110 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 40 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 166 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 100 | |
| | $t_r/t_f$(3) | Output high to low level fall time and output low to high level rise time | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 3.8 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 6.9 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 2.8 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 5.2 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 1.8 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 3.3 | |
| 11 | $F_{max}$(2) | Maximum frequency | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 100 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 50 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 133 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 66 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 220 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 85 | |
| | $t_r/t_f$(3) | Output high to low level fall time and output low to high level rise time | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 3.3 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 6.6 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 2.4 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 4.5 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(4) | - | 1.5 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 2.7 | |

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   ($t_r$+$t_f$) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

### 6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 59: I/O static characteristics*).

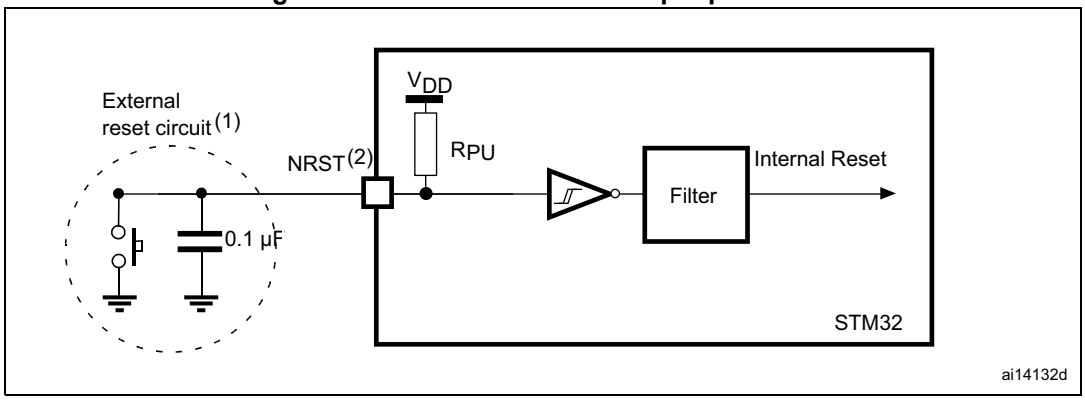
Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23: General operating conditions*.

**Table 63. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$(2) | Weak pull-up equivalent resistor(1) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(2) | NRST Input filtered pulse | 1.71 V < $V_{DD}$ < 3.6 V | - | - | 50 | ns |
| $V_{NF(NRST)}$(2) | NRST Input not filtered pulse | 1.71 V < $V_{DD}$ < 3.6 V | 300 | - | - | |
| | | 1.62 V < $V_{DD}$ < 3.6 V | 1000 | - | - | |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

**Figure 22. Recommended NRST pin protection**



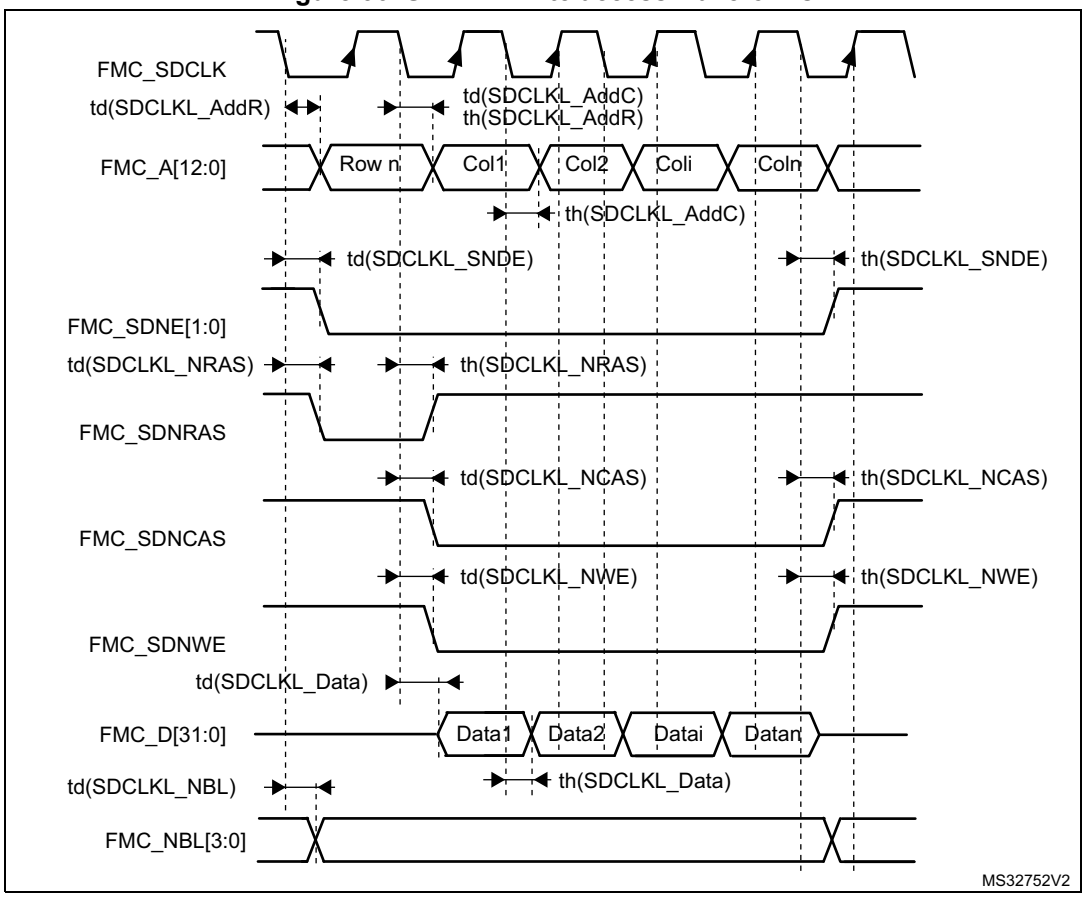

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 63*. Otherwise the reset is not taken into account by the device.

**Table 79. LPSDR SDRAM read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | $2T_{fmc\_ker\_ck} - 1$ | $2T_{fmc\_ker\_ck} + 0.5$ | ns |
| $t_{su(SDCLKH\_Data)}$ | Data input setup time | 2 | - | |
| $t_{h(SDCLKH\_Data)}$ | Data input hold time | 1.5 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 2.5 | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip select valid time | - | 2.5 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNRAS}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

**Figure 36. SDRAM write access waveforms**



### 6.3.26 Comparator characteristics

**Table 95. COMP characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.62 | 3.3 | 3.6 | V |
| $V_{IN}$ | Comparator input voltage range | - | | 0 | - | $V_{DDA}$ | |
| $V_{BG}$(2) | Scaler input voltage | - | | Refer to $V_{REFINT}$ | | | |
| $V_{SC}$ | Scaler offset voltage | - | | - | ±5 | ±10 | mV |
| $I_{DDA(SCALER)}$ | Scaler static consumption from $V_{DDA}$ | BRG_EN=0 (bridge disable) | | - | 0.2 | 0.3 | µA |
| | | BRG_EN=1 (bridge enable) | | - | 0.8 | 1 | |
| $t_{START\_SCALER}$ | Scaler startup time | - | | - | 140 | 250 | µs |
| $t_{START}$ | Comparator startup time to reach propagation delay specification | High-speed mode | | - | 2 | 5 | µs |
| | | Medium mode | | - | 5 | 20 | |
| | | Ultra-low-power mode | | - | 15 | 80 | |
| $t_D$ | Propagation delay for 200 mV step with 100 mV overdrive | High-speed mode | | - | 50 | 80 | ns |
| | | Medium mode | | - | 0.5 | 1.2 | µs |
| | | Ultra-low-power mode | | - | 2.5 | 7 | |
| | Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs | High-speed mode | | - | 50 | 120 | ns |
| | | Medium mode | | - | 0.5 | 1.2 | µs |
| | | Ultra-low-power mode | | - | 2.5 | 7 | |
| $V_{offset}$ | Comparator offset error | Full common mode range | | - | ±5 | ±20 | mV |
| $V_{hys}$ | Comparator hysteresis | No hysteresis | | - | 0 | - | mV |
| | | Low hysteresis | | - | 10 | - | |
| | | Medium hysteresis | | - | 20 | - | |
| | | High hysteresis | | - | 30 | - | |
| $I_{DDA(COMP)}$ | Comparator consumption from $V_{DDA}$ | Ultra-low-power mode | Static | - | 400 | 600 | nA |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 800 | - | |
| | | Medium mode | Static | - | 5 | 7 | µA |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 6 | - | |
| | | High-speed mode | Static | - | 70 | 100 | |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 75 | - | |

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 27: Embedded reference voltage*.

### 6.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 99* for LCD-TFT are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and $V_{DD}$ supply voltage summarized in *Table 23: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled

**Table 99. LTDC characteristics (1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLK}$ | LTDC clock output frequency | 2.7 V < $V_{DD}$ < 3.6 V, 20 pF | - | 150 | MHz |
| | | 2.7 V < $V_{DD}$ < 3.6 V | - | 133 | |
| | | 1.62 V < $V_{DD}$ < 3.6 V | - | 90 | |
| $D_{CLK}$ | LTDC clock output duty cycle | - | 45 | 55 | % |
| $t_{w(CLKH)}$, $t_{w(CLKL)}$ | Clock High time, low time | | $t_{w(CLK)}/2-0.5$ | $t_{w(CLK)}/2+0.5$ | ns |
| $t_{v(DATA)}$ | Data output valid time | | - | 0.5 | |
| $t_{h(DATA)}$ | Data output hold time | | 0 | - | |
| $t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$ | HSYNC/VSYNC/DE output valid time | | - | 0.5 | |
| $t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$ | HSYNC/VSYNC/DE output hold time | | 0.5 | - | |

1. Guaranteed by characterization results.

**Figure 53. SAI master timing waveforms**

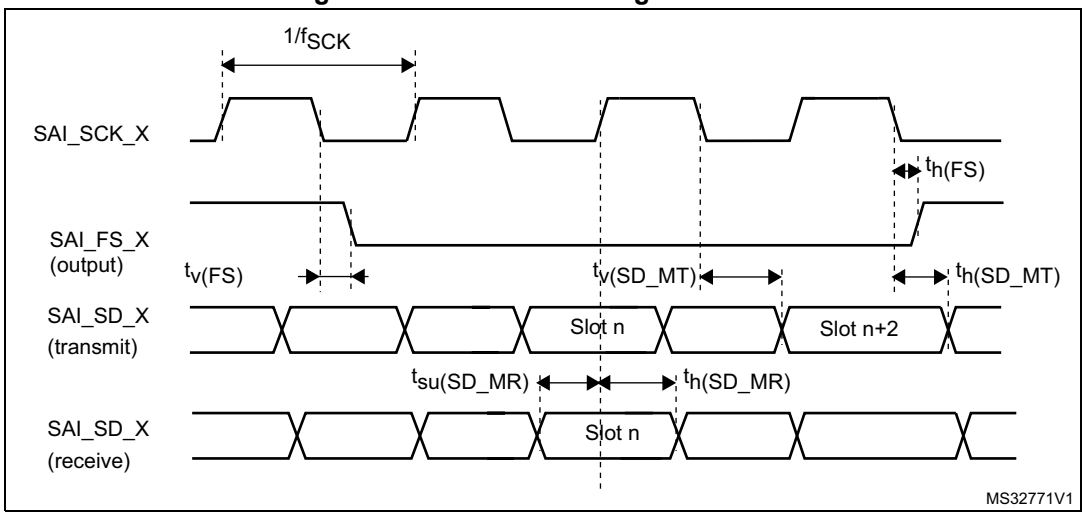
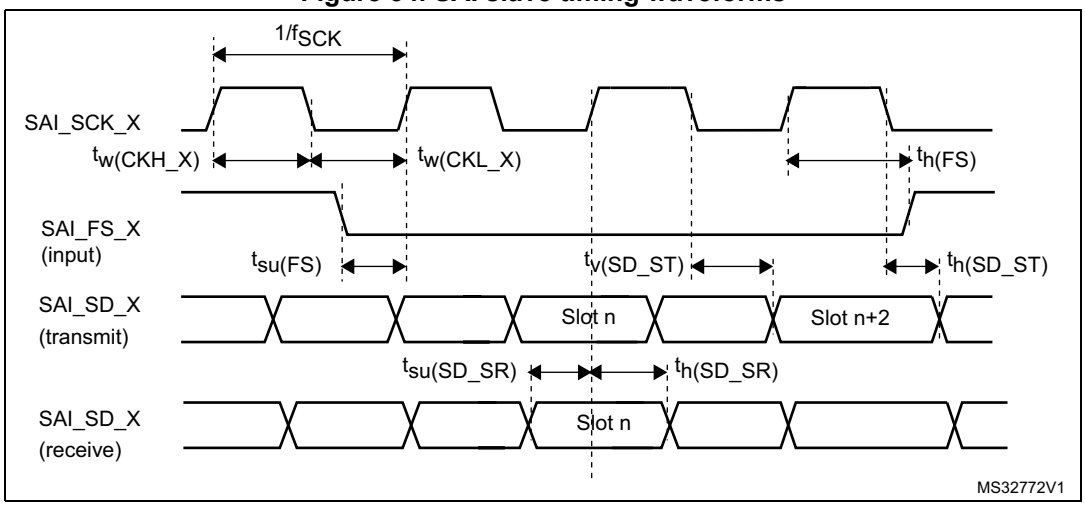



**Figure 54. SAI slave timing waveforms**




## MDIO characteristics

**Table 106. MDIO Slave timing parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{sDC}$ | Management data clock | - | - | 40 | MHz |
| $t_{d(MDIO)}$ | Management data input/output **output valid time** | 7 | 8 | 20 | ns |
| $t_{su(MDIO)}$ | Management data input/output **setup time** | 4 | - | - | |
| $t_{h(MDIO)}$ | Management data input/output **hold time** | 1 | - | - | |

The MDIO controller is mapped on APB2 domain. The frequency of the APB bus should at least 1.5 times the MDC frequency: $F_{PCLK2} \geq 1.5 * F_{MDC}$.

**Table 116. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.000 | - | - | 0.4724 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.